

Annex AD - Raw Card AD

DDR3 Registered DIMM Design File

Specification Revision	Applicable Design File	Applicable BOM
1.00	PC3-RDIMM_V100_RC_AD0_20111103.brd	PC3-RDIMM_V100_RC_AD0_20120717_BOM.TXT

Note 1 “Reference” design file updates will be released as needed. This Registered DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated.

Module Configuration

DIMM		SDRAM die ²		# of SDRAM die	# of Physical Ranks	# of Address bits row/col/Bank	MO-269 variation ¹
Capacity	Organization	Density	Organization				
4GB	128M x 72	512Mbit	128M x 4	72	4	13/11/3	GB
8GB	256M x 72	1Gbit	256M x 4	72	4	14/11/3	GB
16GB	512M x 72	2Gbit	512M x 4	72	4	15/11/3	GB
32GB	1G x 72	4Gbit	1G x 4	72	4	16/11/3	GB
64GB	2G x 72	8Gbit	2G x 4	72	4	16/12/3	GB

Note 1 Note: Some heat spreaders may not be covered within these variations.

Note 2 These are 3DS components. These are 2 die per package. Each die has its own CS_n pin.

SDRAM Configuration

Raw Card	Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM	SDRAM Package Type	SDRAM Organization	MO-207 variation	Notes
AD0	10.5 mm x 12.0 mm	8	78 Ball FBGA	x4, 3DS, 2 die, two row	DT-z	

Supported Speeds

Raw Card	Config	PC3-6400	PC3-8500	PC3-10600	PC3-12800	PC3-14900	Notes
AD0	DDR3	X	X	X	X		1
	DDR3L	X	X	X	X		1

Note 1 “X” reflects speed grades approved from previous ballots. “P” reflects speed grades for this ballot. JEDEC office to replace “P” with “X” before publication.

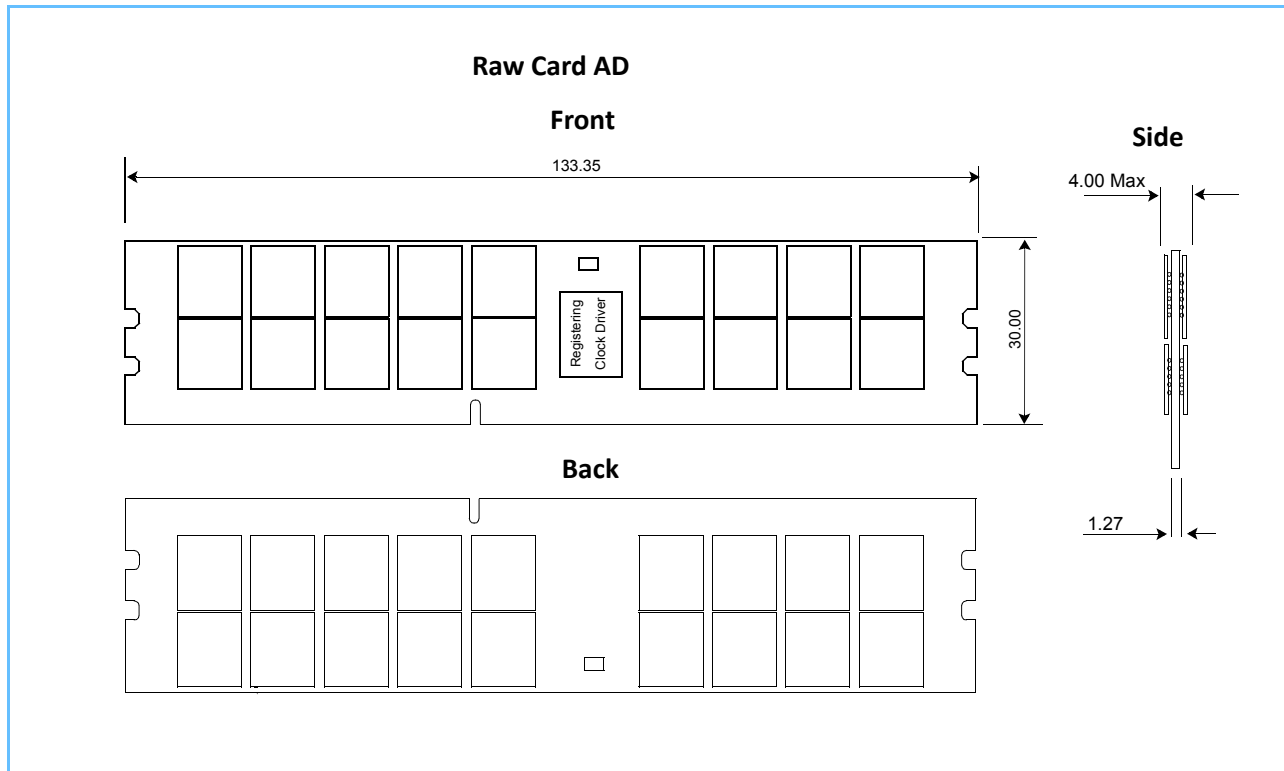
Design Rules and Deviations

Note 1 Design uses 0.075 mm trace width on outer layers. This implies outer layer copper thickness should be limited to 0.037 mm or less.

Note 2 Post register clocks are terminated with a single resistor.

General Layout

x72 DIMM, populated as four physical rank of x4 DDR3 SDRAMs



Note 1 All dimensions are typical unless otherwise stated. (Millimeters)

Note 2 Serial PD with thermal sensor is within the thermal sensor placement area as defined in MO-269.

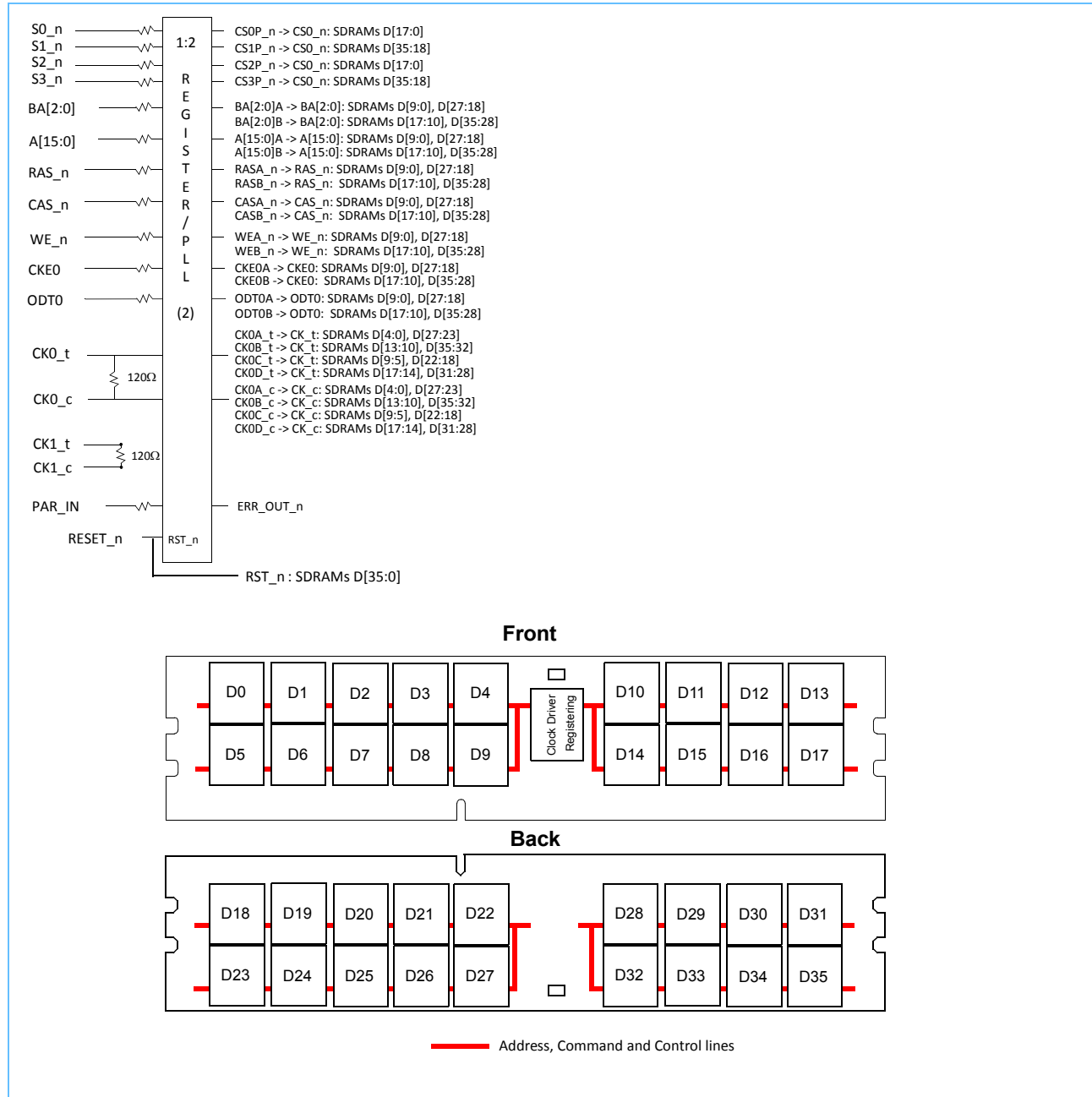
Note 3 Registering clock driver is placed within the Register Placement Area as defined in MO-269 although compliance is not mandated as monolithic DRAMs are used in this assembly.

Note 4 Implementation and dimensions are without heat spreader.

Note 5 In the event that a heat spreader is added to this module, module thickness would increase. Please refer to MO-269 for dimensions of specific variations with heat spreader fitted.

Block Diagram

x72 DIMM, populated as four physical rank of x4 DDR3 3DS SDRAMs (part 1 of 3)

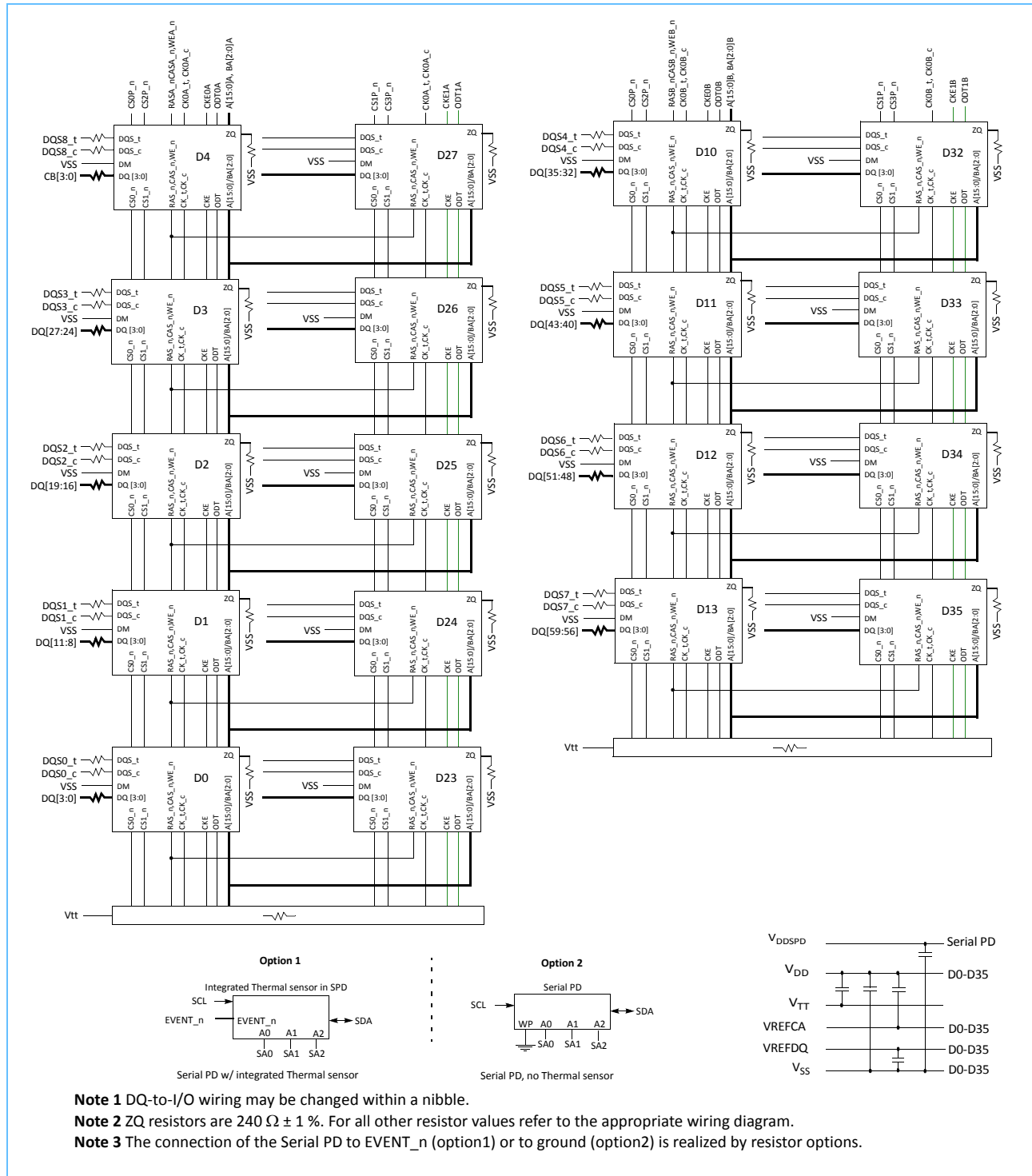


Note 1 CK0_t and CK0_c are differentially terminated with a single 120 Ω ± 5 % resistor.

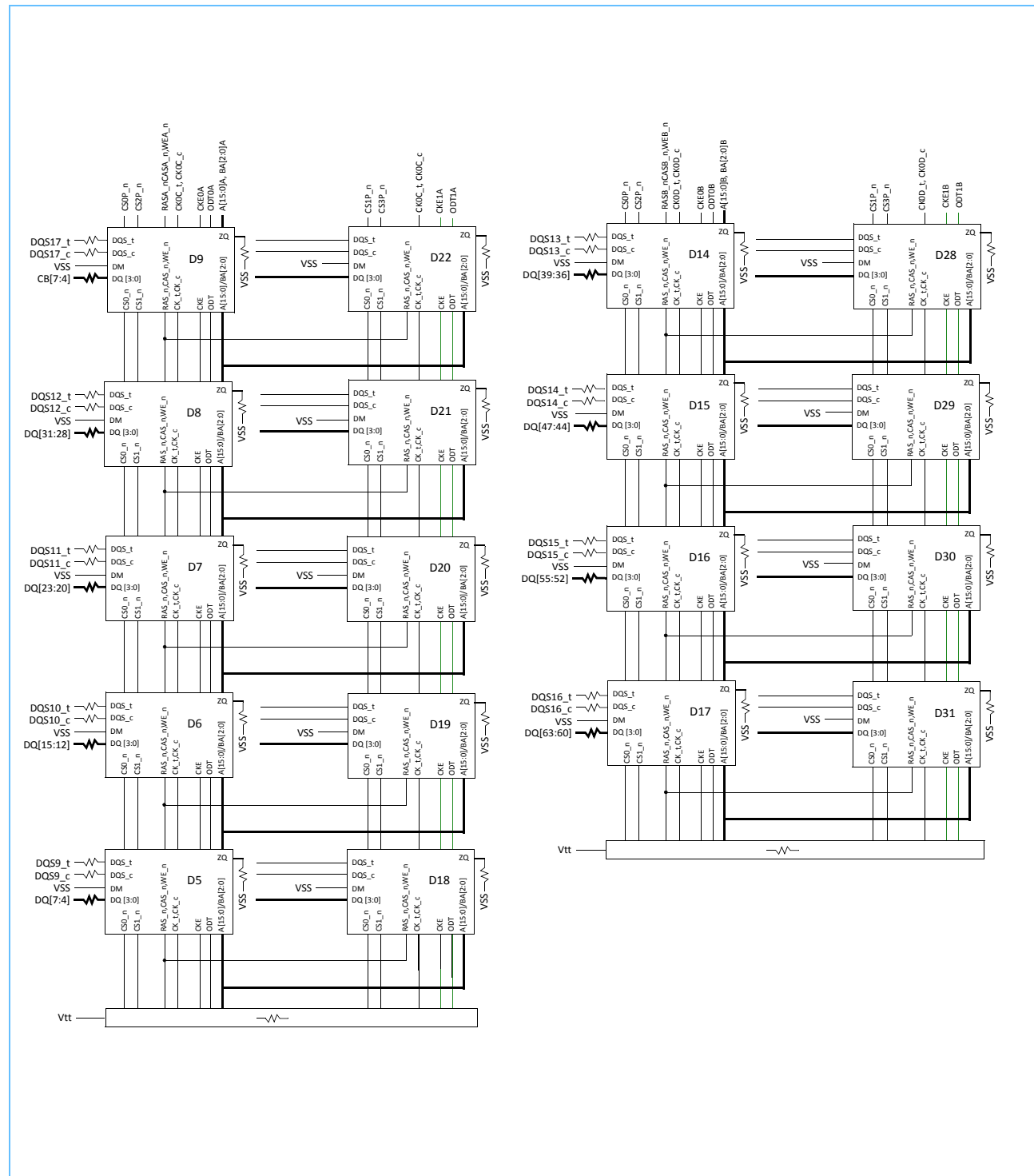
Note 2 CK1_t and CK1_c are differentially terminated with a single 120 Ω ± 5 % resistor, but are not used.

Block Diagram

x72 DIMM, populated as four physical rank of x4 DDR3 3DS SDRAMs (part 2 of 3)



x72 DIMM, populated as four physical rank of x4 DDR3 3DS SDRAMs (part 3 of 3)



Registering Clock Driver

Refer to the register vendor data sheets for all technical specifications and requirements.

Component Specifications

Register Type	Register Speed Grade PC3-6400	Register Speed Grade PC3-8500	Register Speed Grade PC3-10600	Register Speed Grade PC3-12800	Register Speed Grade PC3-14900	Quantity
1:2 28-bit 1.5V, 1.35V	SSTE32882	SSTE32882	SSTE32882	SSTE32882	SSTE32882	1

Register Control Bit Settings

Types of Control Bits:

1. Reserved for future use (RFU):

These control register bits must be programmed to zero for all raw cards that have been developed/manufactured before this “future use” was defined.

2. Test bits (Test):

These control register bits are used by Register, DIMM or System vendors for test and characterization purposes only. They must be programmed to zero for normal operation.

3. Card type specific (Card):

These values were used during validation of this reference design. It is recommended that systems program these register bits as defined here to ensure operation as validated. Any change from these values to match module implementation must be verified in simulation and testing.

4. Application specific bits (A/S):

These control register bits are freely programmable by the user based on the actual system configuration in which this DIMM is used.