

4.20.24 - 240-Pin, 72 bit-wide, PC3(L)-6400/PC3(L)-8500/PC3(L)-10600/PC3(L)-12800/PC3(L)-14900/PC3(L)-17000 DDR3 SDRAM Load Reduced DIMM Design Specification

DDR3 SDRAM Load Reduced DIMM Design Specification

Revision 0.35

April 2014

Contents

1.0 Product Description.....	4
Table 1 – Product Family Attributes	5
Table 2 – Environmental Parameters.....	5
2.0 Pinout and Description.....	6
Table 3 – Pin Description	6
Table 4 – Load Reduced DIMM Input/Output Functional Description.....	7
Table 5 – DDR3 240-pin LRDIMM, RDIMM and UDIMM Pinout.....	9
Table 6 – Pinout Comparison Between UDIMM Type and LRDIMM Type	10
Table 7 – Pinout Comparison Between RDIMM Type and LRDIMM Type	11
3.0 Component Details	12
Table 8 – Supported SDRAM Components Maximum size for 1Gb to 4Gb	12
4.0 Pin Assignments for 1Gb to 4Gb; DDR3 SDRAM	13
Table 9 – x4 Ballout of DDR3 SDRAMs (Top view)	13
Table 10 – x8 Ballout of DDR3 SDRAMs (Top view)	14
Table 11 – x4 Ballout of DDR3 SDRAMs for DDP Stacked DIMM (Top view).....	15
Table 12 – x8 Ballout of DDR3 SDRAMs for Stacked DDP DIMM (Top view).....	16
Table 13 – x4 Ballout of DDR3 SDRAMs for Stacked QDP DIMM (Top view)	17
Table 14 – x8 Ballout of DDR3 SDRAMs for Stacked QDP DIMM (Top view)	18
5.0 PCB Pad Array Options for SDRAM Placements	19
Figure 1 – x4 SDRAM Pad Array (Top view)	20
Figure 2 – x8 SDRAM Pad Array (Top view)	21
Figure 3 – x4 SDRAM Pad Array DDP Stacked (Top View).....	22
Figure 4 – x8 SDRAM Pad Array DDP Stacked (Top View).....	23
Figure 5 – x4 SDRAM Pad Array QDP Stacked (Top view)	24
Figure 6 – x8 SDRAM Pad Array QDP Stacked (Top view)	25
6.0 Pin Assignments for Memory Buffer.....	26
Table 15 – Left Side (1 of 3).....	26
Table 16 – Left Side (2 of 3).....	27
Table 17 – Right Side (3 of 3)	28
7.0 Pin Assignments for Serial Presence Detect	29
Table 18 – SPD Pinout (Top view).....	29
8.0 DDR3 Load Reduced DIMM Wiring Details.....	30
Table 19 – Signal Groups	30
9.0 Net Structures	31
9.1 Explanation of Net Structure Diagrams.....	31
9.2 Net Structure Example.....	31
Figure 7 – 4 GB double-sided x72 DIMM using 1 Gbit, 128Mx8 SDRAM devices	31

9.3 General Net Structure Routing Guidelines	32
Table 20 – Signal referencing information	32
9.4 Test Points.....	33
Figure 8 – Test Point Location	33
9.5 Differential Clock Net Structures.....	33
10.0 Timing	34
10.1 DIMM Timing Requirements	34
Table 21 – LRDIMM Command Separation for Different Ranks	34
Table 22 – LRDIMM Command Separation for Different Ranks	34
Figure 9 – Write Followed by Write to a Different Physical Rank at MB Host Interface.....	35
Figure 10 – Read Followed by Read to a Different Physical Rank at MB Host Interface ..	35
Figure 11 – Write Followed by Read to a Different Physical Rank at MB DRAM Interface	35
10.2 Command and DQ Delay Path Calculation	36
10.3 Example Address Timing Budget	36
11.0 DIMM Wiring Requirements	37
11.1 ZQ Requirements	37
11.2 DQ Requirements	37
Table 23 – Gold Finger to Memory Buffer Mapping	37
11.3 VREF Requirements	38
11.4 Signals not used on JEDEC Standard DIMMs	38
11.5 Wiring for SMBus.....	39
Figure 12 – Schematic of SPD/Thermal Sensor and MB	39
Figure 13 – The following schematic defines the required wiring for AVDD.....	40
12.0 Control Wiring.....	41
Table 24 – QCSx_n to Physical Rank Mapping	41
Figure 14 – 2 rank x4 Module Configuration Wiring	41
Figure 15 – 4 rank x4 Module Configuration Wiring	42
Figure 16 – 4 rank x8 Module Configuration Wiring	42
Figure 17 – 8 rank x4 Module Configuration Wiring	43
Figure 18 – 8 Rank x8 Module Configuration Wiring	43
13.0 Serial Presence Detect Definition.....	44
14.0 DDR3 DIMM Label Format	45
15.0 DIMM Mechanical Specifications.....	47
Table 25 – Maximum LRDIMM Thickness	47
16.0 Design File Naming Convention.....	48
Annex A - Raw Card A.....	A1
Annex C - Raw Card C.....	C1
Annex K - Raw Card K.....	K1

1.0 Product Description

This specification defines the electrical and mechanical requirements for 240-pin, 72 bit-wide, Load Reduced Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR3 SDRAM DIMMs). These SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations.

PC3 refers to DIMMs designed to operate at 1.5V nominal. PC3L refers to DIMMs with components that can support 1.35V nominal.

PC3(L)-6400, PC3(L)-8500, PC3(L)-10600, PC3(L)-12800, PC3-14900, PC3-17000 refers to the JEDEC standard DIMM naming convention in which PC3(L)-6400, PC3(L)-8500, PC3(L)-10600, PC(L)-12800, PC3-14900 and PC3-17000 indicates a DIMM running at 400, 533, 667, 800, 931 and 1063 MHz clock speed and offering 6400, 8500, 10600, 12800, 14900 and 17000 MB/s bandwidth.

Reference design examples are included which provide an initial basis for Registered DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC3(L)-6400, PC3(L)-8500, PC3(L)-10600, PC3(L)-12800, PC3-14900 and PC3-17000 support. All Load Reduced DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design. DDR3 and DDR3L (PC3 and PC3L) have different requirements. Speed grades and voltages for each reference design are defined in each appendix. DDR3 refers to 1.5V operation only. For the design to be 1.35V capable the appendix must specifically include DDR3L.

The LRDIMM differs from RDIMMs in that the SDRAMs do not connect directly to the edge connector with the exception of VDD and VSS (ground). The Memory Buffer (MB) buffers both address and data. Increased performance is achieved based on the LRDIMM presenting only one load to the system. Increased capacity is achieved since the MB drives only the SDRAMs on the module and therefore a well defined topology and load. The maximum number of SDRAM die is 144. The LRDIMM is intended to function in all RDIMM platforms with appropriate BIOS changes. Systems designed to function with LRDIMMs will be better able to take advantage of LRDIMM features.

While four chip selects are possible at the edge connector the MB provides a “address multiplication” feature. The MB uses one or two of the address lines not directly usable by the SDRAM to generate additional chips selects to the SDRAM. This feature is completely configurable in the MB. There are 2 additional address lines (A16 and A17) defined that will typically only be used with the address multiplication feature. With address multiplication refresh and mode register access become more difficult. This is because the system sees the LRDIMM as fewer logical ranks than the true physical ranks. Rank based commands like refresh and mode register access must accommodate this in some fashion. The MB provides several methods. See the MB Design Specification for more information on the MB features and programming.

The LRDIMM has the option of using ODT0 only or both ODT0 and ODT1.

The VREF_DQ and VREF_CA pins on the edge connector provide the reference for the MB. The MB has additional VREF generators that may be used for the SDRAM reference and as the reference for the MB interfaces.

LRDIMMs can use an address mirroring feature. This is exactly as defined in the UDIMM Design Specification with the exception that all odd ranks are mirrored when this feature is used. There is an SPD bit that provides the information to the system on whether the specific LRDIMM requires the use of address mirroring. Since the wiring on the LRDIMM is different to support this feature it must be used when the LRDIMM is wired to use address mirroring. As defined the controller must have the capability to do address mirroring.

The LRDIMMs are defined to require an integrated thermal sensor with the SPD. Additionally the MB is defined to have an internal thermal sensor.

Table 1 – Product Family Attributes

DIMM organization	x72 ECC
DIMM dimensions: height (nom.) x width (nom.) x thickness (max.) / MO-number, Variation	30.35 mm x 133.35 mm x 4.00 mm / MO-269, Variation TBD 30.35 mm x 133.35 mm x 6.75 mm / MO-269, Variation TBD 30.35 mm x 133.35 mm x 7.55 mm / MO-269, Variation TBD 18.75 mm x 133.35 mm x 4.00 mm / MO-269, Variation DB 18.75 mm x 133.35 mm x 6.75 mm / MO-269, Variation EB 18.75 mm x 133.35 mm x 7.55 mm / MO-269, Variation FB
Pin count	240
SDRAMs supported	1 Gb, 2 Gb, 4 Gb
Capacity	4 GB, 8 GB, 16 GB, 32 GB, 64 GB
Serial PD	Consistent with JC 45
Voltage options	1.35 and 1.5 volt (V_{DD}), 3.3 volt (V_{DDSPD})
Interface	1.35 and 1.5 volt signal switching based on reference voltage at $V_{DD}/2$. See DRAM specification for more detail.

Table 2 – Environmental Parameters

DR3 SDRAM Load Reduced DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating temperature	See Note		3
H_{OPR}	Operating humidity (relative)	10 to 90	%	1
T_{STG}	Storage temperature	-50 to +100	°C	1
H_{STG}	Storage humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric pressure (operating & storage)	105 to 69	K Pascal	1, 2
Note 1 Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Note 2 Up to 9850 ft. Note 3 The designer must meet the case temperature specifications for individual module components.				

2.0 Pinout and Description

Table 3 – Pin Description

Pin Name	Description	Number	Pin Name	Description	Number
CK0_t	Clock Input, positive line	1	Par_In	Parity bit for the Address and Control bus	1
CK0_c	Clock Input, negative line	1	ErrOut_n	Parity error found on the Address and Control bus	1
CK1_t	Clock Input, positive line	1	ODT[0]	On Die Termination Input	1
CK1_c	Clock Input, negative line	1	DQ[63:0]	Data Input/Output	64
CKE[1:0]	Clock Enables	2	CB[7:0]	Data check bits Input/Output	8
CKE[3:2], ODT[1], TEST	Clock Enables On Die Termination Memory bus tool (Not Connected and Not Usable on DIMMs)	2	DQS[8:0]_t	Data strobes	9
RAS_n	Row Address Strobe	1	DQS[8:0]_c	Data strobes, negative line	9
CAS_n	Column Address Strobe	1	DM[8:0]/ DQS[17:9]_t, TDQS[17:9]_t	Data Masks / Data strobes, Termination data strobes	9
WE_n	Write Enable	1	DQS[17:9]_c TDQS[17:9]_c	Data strobes, negative line, Termination data strobes	9
S[1:0]_n	Chip Selects	2	EVENT_n	Reserved for optional hardware temperature sensing	1
S[3:2]_n, A17, A16	Chip Selects Address Inputs	2	TEST	Memory bus test tool (Not Connected and Not Usable on DIMMs)	1
A[9:0],A11, A[15:13]	Address Inputs	14	RESET_n	Register and SDRAM control pin	1
A10/AP	Address Input/Autoprecharge	1	V _{DD}	Power Supply	22
A12/BC_n	Address Input/Burst chop	1	V _{SS}	Ground	59
BA[2:0]	SDRAM Bank Addresses	3	V _{REFDQ}	Reference Voltage for DQ	1
SCL	Serial Presence Detect (SPD) Clock Input	1	V _{REFCA}	Reference Voltage for CA	1
SDA	SPD Data Input/Output	1	V _{TT}	Termination Voltage	4
SA[2:0]	SPD Address Inputs	3	V _{DDSPD}	SPD Power	1

Table 4 – Load Reduced DIMM Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0_t	IN	Positive Line	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM Clock Driver.
CK0_c	IN	Negative Line	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM Clock Driver.
CK1_t	IN	Positive Line	Terminated but not used on RDIMMs.
CK1_c	IN	Negative Line	Terminated but not used on RDIMMs.
CKE[3:0]	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
S[3:0]_n	IN	Active Low	Enables the command decoders for the associated rank of SDRAM when low and disables decoders when high. When decoders are disabled, new commands are ignored and previous operations continue. Other combinations of these input signals perform unique functions, including disabling all outputs (except CKE and ODT) of the register(s) on the DIMM or accessing internal control words in the register device(s). For modules with two registers, S[3:2]_n operate similarly to S[1:0]_n for the second set of register outputs or register control words.
ODT[1:0]	IN	Active High	On-Die Termination control signals
RAS_n, CAS_n, WE_n	IN	Active Low	When sampled at the positive rising edge of the clock, CAS_n, RAS_n, and WE_n define the operation to be executed by the SDRAM.
V _{REFDQ}	Supply		Reference voltage for DQ0-DQ63 and CB0-CB7.
V _{REFCA}	Supply		Reference voltage for A0-A17, BA0-BA2, RAS_n, CAS_n, WE_n, S0_n, S1_n, S2_n, S3_n, CKE0, CKE1, CKE2, CKE3, Par_In, ODT0 and ODT1.
BA[2:0]	IN	—	Selects which SDRAM bank of eight is activated. BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines mode register is to be accessed during an MRS cycle.
A[17:13, 12/BC_n, 11, 10/AP, [9:0]	IN	—	Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also utilized for BL 4/8 identification for “BL on the fly” during CAS_n command. The address inputs also provide the op-code during Mode Register Set commands.
DQ[63:0], CB[7:0]	I/O	—	Data and Check Bit Input/Output pins
DM[8:0]	IN	Active High	Masks write data when high, issued concurrently with input data.
V _{DD} , V _{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic.
V _{TT}	Supply		Termination Voltage for Address/Command/Control/Clock nets.
DQS[17:0]_t	I/O	Positive Edge	Positive line of the differential data strobe for input and output data.
DQS[17:0]_c	I/O	Negative Edge	Negative line of the differential data strobe for input and output data.

Table 4 – Load Reduced DIMM Input/Output Functional Description (Continued)

Symbol	Type	Polarity	Function
TDQS[17:9]_t TDQS[17:9]_c	OUT		TDQS_t/TDQS_c is applicable for X8 DRAMs only. When enabled via Mode Register A11=1 in MR1, DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11=0 in MR1, DM/TDQS_t will provide the data mask function and TDQS_c is not used. X4/X16 DRAMs must disable the TDQS function via mode register A11=0 in MR1
SA[2:0]	IN	—	These signals are tied at the system planar to either V _{SS} or V _{DDSPD} to configure the serial SPD EEPROM address range.
SDA	I/O	—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V _{DDSPD} on the system planar to act as a pullup.
SCL	IN	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus line to V _{DDSPD} on the system planar to act as a pullup.
EVENT_n	OUT (open drain)	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the EVENT_n pin on TS/SPD part. No pull-up resistor is provided on DIMM.
V _{DDSPD}	Supply		Serial EEPROM positive power supply wired to a separate power pin at the connector which supports from 3.0 Volt to 3.6 Volt (nominal 3.3V) operation.
RESET_n	IN	Active Low	The RESET_n pin is connected to the RESET_n pin on the register and to the RESET_n pin on the DRAM.
Par_In	IN		Parity bit for the Address and Command bus. ("1": Odd, "0": Even)
ErrOut_n	OUT (open drain)		Parity error detected on the Address and Command bus. A resistor may be connected from ErrOut_n bus line to V _{DD} on the system planar to act as a pull up.
TEST			Used by memory bus analysis tools (unused (NC) on memory DIMMs)

Table 5 – DDR3 240-pin LRDIMM, RDIMM and UDIMM Pinout

Pin#	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin#	Front Side	Pin#	Back Side
1	V _{REFDQ}	121	V _{SS}	31	DQ25	151	V _{SS}	61	A2	181	A1	91	DQ41	211	V _{SS}
2	V _{SS}	122	DQ4	32	V _{SS}	152	DM3, DQS12_t, TDQS12_t	62	V _{DD}	182	V _{DD}	92	V _{SS}	212	DM5, DQS14_t, TDQS14_t
3	DQ0	123	DQ5	33	DQS3_c	153	NC,DQS12_c, TDQS12_c	63	NC, CK1_t	183	V _{DD}	93	DQS5_c	213	NC, DQS14_c, TDQS14_c
4	DQ1	124	V _{SS}	34	DQS3_t	154	V _{SS}	64	NC, CK1_c	184	CK0_t	94	DQS5_t	214	V _{SS}
5	V _{SS}	125	DM0,DQS9_t, TDQS9_t	35	V _{SS}	155	DQ30	65	V _{DD}	185	CK0_c	95	V _{SS}	215	DQ46
6	DQS0_c	126	NC,DQS9_c, TDQS9_c	36	DQ26	156	DQ31	66	V _{DD}	186	V _{DD}	96	DQ42	216	DQ47
7	DQS0_t	127	V _{SS}	37	DQ27	157	V _{SS}	67	V _{REFCA}	187	EVENT_n, NC	97	DQ43	217	V _{SS}
8	V _{SS}	128	DQ6	38	V _{SS}	158	CB4,NC	68	Par_In, NC	188	A0	98	V _{SS}	218	DQ52
9	DQ2	129	DQ7	39	CB0,NC	159	CB5,NC	69	V _{DD}	189	V _{DD}	99	DQ48	219	DQ53
10	DQ3	130	V _{SS}	40	CB1,NC	160	V _{SS}	70	A10 / AP	190	BA1	100	DQ49	220	V _{SS}
11	V _{SS}	131	DQ12	41	V _{SS}	161	NC, DM8, DQS17_t, TDQS17_t	71	BA0	191	V _{DD}	101	V _{SS}	221	DM6, DQS15_t, TDQS15_t
12	DQ8	132	DQ13	42	DQS8_c	162	NC,DQS17_c, TDQS17_c	72	V _{DD}	192	RAS_n	102	DQS6_c	222	NC, DQS15_c, TDQS15_c
13	DQ9	133	V _{SS}	43	DQS8_t	163	V _{SS}	73	WE_n	193	S0_n	103	DQS6_t	223	V _{SS}
14	V _{SS}	134	DM1, DQS10_t, TDQS10_t	44	V _{SS}	164	CB6,NC	74	CAS_n	194	V _{DD}	104	V _{SS}	224	DQ54
15	DQS1_c	135	NC, DQS10_c, TDQS10_c	45	CB2,NC	165	CB7,NC	75	V _{DD}	195	ODT0	105	DQ50	225	DQ55
16	DQS1_t	136	V _{SS}	46	CB3,NC	166	V _{SS}	76	S1_n, NC	196	A13	106	DQ51	226	V _{SS}
17	V _{SS}	137	DQ14	47	V _{SS}	167	NC(TEST), CKE2	77	ODT1, CKE3, NC	197	V _{DD}	107	V _{SS}	227	DQ60
18	DQ10	138	DQ15	48	VTT, NC	168	RESET_n	78	V _{DD}	198	S3_n, A17, NC	108	DQ56	228	DQ61
19	DQ11	139	V _{SS}	KEY				79	S2_n, A16, NC	199	V _{SS}	109	DQ57	229	V _{SS}
20	V _{SS}	140	DQ20	49	VTT, NC	169	CKE1, NC	80	V _{SS}	200	DQ36	110	V _{SS}	230	DM7, DQS16_t, TDQS16_t
21	DQ16	141	DQ21	50	CKE0	170	V _{DD}	81	DQ32	201	DQ37	111	DQS7_c	231	NC, DQS16_c, TDQS16_c
22	DQ17	142	V _{SS}	51	V _{DD}	171	A15	82	DQ33	202	V _{SS}	112	DQS7_t	232	V _{SS}
23	V _{SS}	143	DM2, DQS11_t, TDQS11_t	52	BA2	172	A14	83	V _{SS}	203	DM4, DQS13_t, TDQS13_t	113	V _{SS}	233	DQ62
24	DQS2_c	144	NC, DQS11_c, TDQS11_c	53	ErrOut_n NC	173	V _{DD}	84	DQS4_c	204	NC, DQS13_c, TDQS13_c	114	DQ58	234	DQ63
25	DQS2_t	145	V _{SS}	54	V _{DD}	174	A12 / BC_n	85	DQS4_t	205	V _{SS}	115	DQ59	235	V _{SS}
26	V _{SS}	146	DQ22	55	A11	175	A9	86	V _{SS}	206	DQ38	116	V _{SS}	236	VDDSPD
27	DQ18	147	DQ23	56	A7	176	V _{DD}	87	DQ34	207	DQ39	117	SA0	237	SA1
28	DQ19	148	V _{SS}	57	V _{DD}	177	A8	88	DQ35	208	V _{SS}	118	SCL	238	SDA
29	V _{SS}	149	DQ28	58	A5	178	A6	89	V _{SS}	209	DQ44	119	SA2	239	V _{SS}
30	DQ24	150	DQ29	59	A4	179	VDD	90	DQ40	210	DQ45	120	V _{TT}	240	V _{TT}
				60	V _{DD}	180	A3								

See Notes on following page for differences of RDIMMs and UDIMMs and LRDIMMs

Table 6 – Pinout Comparison Between UDIMM Type and LRDIMM Type

Pin #	UDIMM		LRDIMM	
	Signal	Notes	Signal	Notes
48, 49	NC	Not used on UDIMMs	VTT	Termination Voltage for Address/Command/Control/Clock nets.
120, 240	VTT	Termination Voltage for Address/Command/Control/Clock nets.	VTT	Termination Voltage for Address/Command/Control/Clock nets.
53	NC	Not used on UDIMMs	ERROut_n	Parity error output of Memory Buffer
63	CK1_t	Used for 2 rank UDIMMs, not used on single-rank UDIMMs, but terminated	CK1_t	Terminated but not used
64	CK1_c		CK1_c	
68	NC	Not used on UDIMMs	Par_In	Parity input to Memory Buffer (MB). This signal is required for MB functionality.
76	S1_n	Used for dual-rank UDIMMs, not connected on single-rank UDIMMs	S1_n	Chip select for the second logical rank. Required for programming the Memory Buffer. SMBus can be used for programming the MB.
77	ODT1, NC	Used for dual-rank UDIMMs, not connected on single-rank UDIMMs	ODT1, CKE3	Provides 4th CKE signal. Not used on JEDEC standard LRDIMMs but may be used on custom LRDIMMs. Connected to MB.
79	NC	Not used on UDIMMs	S2_n, A16	May be used as third chip select or address A16. Use is system dependent. MB can be programmed to use it as chip select 2 or address A16.
167	NC	TEST input used only on bus analysis probes	CKE2	Not used on JEDEC standard LRDIMMs but may be used on custom LRDIMMs.
169	CKE1, NC	Used for dual-rank UDIMMs, not connected on single-rank UDIMMs	CKE1	2nd CKE.
171	A15, NC	Depending on device density, may not be connected to SDRAMs on UDIMMs. However, these signals are terminated on UDIMMs. A15 not routed on some RCs	A15	Always used on LRDIMMs
172	A14		A14	
196	A13		A13	
198	NC	Not used on UDIMMs	S3_n, A17	May be used as either a 4th chip select or address A17. Use is system dependent. MB can be programmed to use it as chip select 3 or address A17.
39, 40, 45, 46, 158, 159, 164, 165	NC, CBn	Used on x72 UDIMMs, (n = 0...7); not used on x64 UDIMMs	CBn	ECC byte. Always used on LRDIMM.
125, 134, 143, 152, 161, 203, 212, 221, 230	DMn	Connected to DM on x8 DRAMs, UDM or LDM on x16 DRAMs on UDIMMs; (n = 0...8)	DQS [9:17]_t	Always connected to MB. Typically used for LRDIMMs with x4 SDRAMs. Not used for LRDIMMs with x8 SDRAMs.
126, 135, 144, 153, 162, 204, 213, 222, 231	NC	Not used on UDIMMs	DQS [9:17]_c	Always connected to MB. Typically used for LRDIMMs with x4 SDRAMs. Not used for LRDIMMs with x8 SDRAMs.
187	EVENT_n NC	Connected to the thermal sensing component on ECC DIMMs. No connection on non-ECC DIMMs.	EVENT_n	Connected to the thermal sensing component and MB.
NC = no internal connection				

Table 7 – Pinout Comparison Between RDIMM Type and LRDIMM Type

Pin #	RDIMM		LRDIMM	
	Signal	Notes	Signal	Notes
77	ODT1, NC	ODT1 is connected to the register on dual- and quad- rank RDIMMs; NC on single-rank RDIMMs, CKE3 is not available for RDIMMs	ODT1, NC, CKE3	ODT1, CKE3 is connected to the Memory Buffer. It has no defined functionality in normal use but is available for custom applications.
79	S2_n, NC	S2_n is connected to the register on quad-rank RDIMMs, not connected on single or dual rank RDIMMs. A16 is not available for RDIMMs	S2_n, NC, A16	S2_n, A16 is connected to the Memory Buffer. Based on system configuration it may be used as an additional chip select or an addition address input.
167	NC	TEST input used only on bus analysis probes. CKE2 is not available for RDIMMs	NC, CKE2	TEST input used only on bus analysis probes. The CKE2 function is only available on custom modules.
198	S3_n, NC	Connected to the register on quad-rank RDIMMs, not connected on single-or dual-rank RDIMMs	S3_n, NC, A17	S3_n, A17 is connected to the Memory Buffer. Based on system configuration it may be used as an additional chip select or an addition address input.
NC = no internal connection				

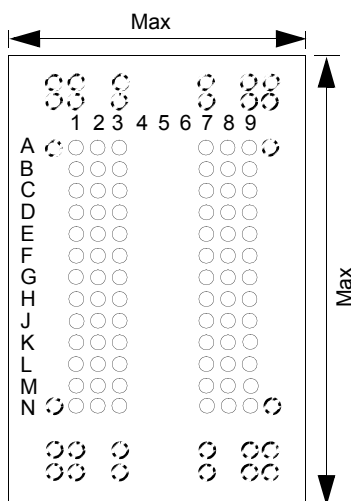
3.0 Component Details

Table 8 – Supported SDRAM Components Maximum size for 1Gb to 4Gb

This table is for reference only. Please see appropriate raw card appendix for more information.

Raw Card	Supported DRAM Outline (Width x Length) max.	Configuration	SDRAM Placement	Package Type	Module Height (mm)	MO-207 variation	# of SDRAM balls supported
A	11.0 mm x 12.0 mm	2 rank x4	2 row vertical	Planar	30.35	DW-z	82
B	11.0 mm x 12.0 mm	4 rank x8	2 row vertical	Planar	30.35	DW-z	82
C	11.0 mm x 12.0 mm	4 rank x4	2 row vertical	DDP	30.35	DW-z	82
D	11.0 mm x 12.0 mm	8 rank x8	2 row vertical	DDP	30.35	DW-z	82
E	11.0 mm x 12.0 mm	8 rank x4	2 row vertical	QDP	30.35	DW-z	82
F	11.0 mm x 12.0 mm	2 rank x4	1 row vertical	DDP	18.75	DW-z	82
G	11.0 mm x 12.0 mm	4 rank x8	1 row vertical	DDP	18.75	DW-z	82
H	11.0 mm x 12.0 mm	4 rank x4	1 row vertical	QDP	18.75	DW-z	82
J	11.0 mm x 12.0 mm	8 rank x8	1 row vertical	QDP	18.75	DW-z	82
K	10.0 mm x 13.0 mm	4 rank x4	2 row flower	DDP	30.35	DW-z	82
	11.0 mm x 12.0 mm						

Note 1 DDP refers to a 2 die stack. QDP refers to a 4 die stack.



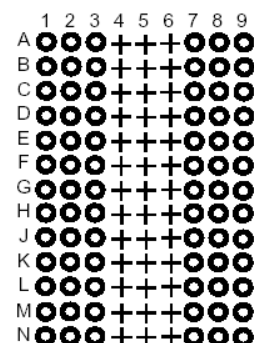
4.0 Pin Assignments for 1Gb to 4Gb; DDR3 SDRAM

Table 9 – x4 Ballout of DDR3 SDRAMs (Top view)

(MO-207 Variation DT-z/DW-z, FBGA 0.8mm x 0.8 mm pitch)

	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NC	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	NC	DQS_c	VDD	VSS	VSSQ		D
K		V _{REFDQ}	VDDQ	NC	NC	NC	VDDQ		E
L		NC	VSS	RAS_n	CK_t	VSS	NC		F
M		ODT	VDD	CAS_n	CK_c	VDD	CKE		G
N		NC	CS	WE_n	A10/AP	ZQ	NC		H
P		VSS	BA0	BA2	A15	V _{REFCA}	VSS		J
R		VDD	A3	A0	A12/BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

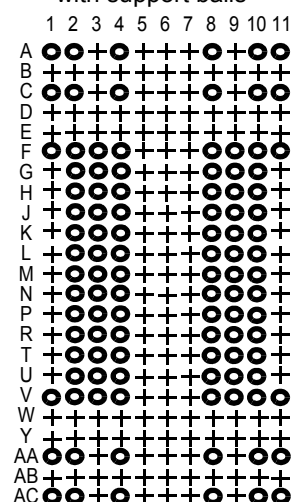
MO-207 Variation DT-z



● Populated ball

+ Ball not populated

MO-207 Variation DW-z
with support balls



Note 1 Above coordinates of ball out corresponds to footprint on PCB (Figure 1 on page 20).

Note 2 "NC" means that the ball is present and is not connected to any signal in the SDRAM package.

Note 3 NC balls may be mated with any solder pad on PCB.

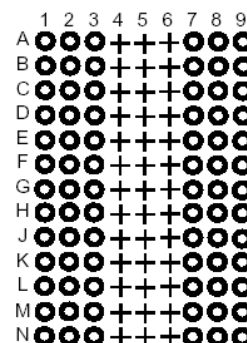
Note 4 This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions

Table 10 – x8 Ballout of DDR3 SDRAMs (Top view)

(MO-207 Variation DT-z/DW-z, FBGA 0.8 mm x 0.8 mm pitch)

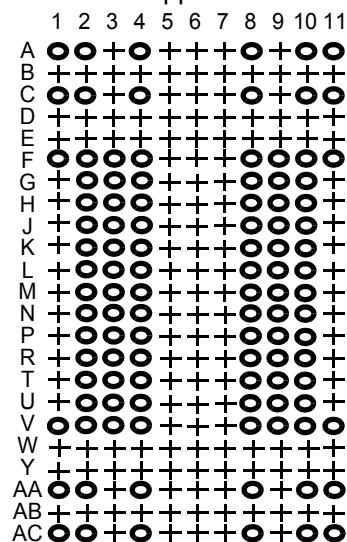
	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NU/ TDQS_c	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM/ TDQS_t	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ		D
K		V _{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ		E
L		NC	VSS	RAS_n	CK_t	VSS	NC		F
M		ODT	VDD	CAS_n	CK_c	VDD	CKE		G
N		NC	CS#	WE_n	A10/AP	ZQ	NC		H
P		VSS	BA0	BA2	A15	V _{REFCA}	VSS		J
R		VDD	A3	A0	A12/ BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z



● Populated ball
+ Ball not populated

MO-207 Variation DW-z
with support balls



Note 1 Above coordinates of ball out corresponds to footprint on PCB (Figure 2 on page 21).

Note 2 "NC" means that the ball is present and is not connected to any signal in the SDRAM package.

Note 3 NC balls may be mated with any solder pad on PCB.

Note 4 "NU" means that the ball is present and may or may not be electrically connected a an active signal in the SDRAM package.

Note 5 NU balls may only be mated with NC solder pads on PCB.

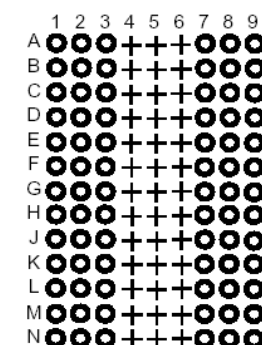
Note 6 This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions.

Table 11 – x4 Ballout of DDR3 SDRAMs for DDP Stacked DIMM (Top view)

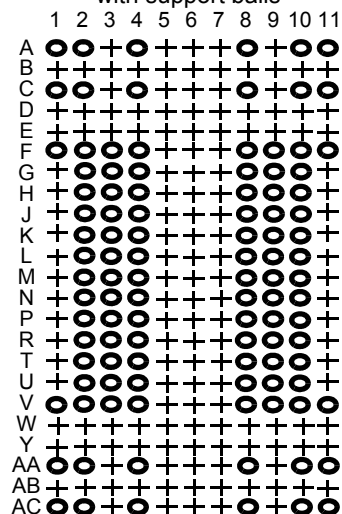
MO-207 Variation DW-z, FBGA 0.8 mm x 0.8 mm pitch)

	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NC	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	NC	DQS_c	VDD	VSS	VSSQ		D
K		V _{REFDQ}	VDDQ	NC	NC	NC	VDDQ		E
L		ODT1	VSS	RAS_n	CK_t	VSS	CKE1		F
M		ODT0	VDD	CAS_n	CK_c	VDD	CKE0		G
N		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1		H
P		VSS	BA0	BA2	A15	V _{REFCA}	VSS		J
R		VDD	A3	A0	A12/BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z



○ Populated ball
 + Ball not populated

MO-207 Variation DW-z
with support balls

Note 1 Above coordinates of ball out corresponds to footprint on PCB (Figure 3 on page 22).

Note 2 “NC” means that the ball is present and is not connected to any signal in the SDRAM package.

Note 3 NC balls may be mated with any solder pad on PCB.

Note 4 This figure is valid for SDRAM specification as defined by JESD79-3. Refer to that specification for any later revisions.