

Annex K - Raw Card K

DDR3 Registered DIMM Design File

Applicable Design File	Applicable BOM
PC3-LRDIMM_V040_RC_K0_20100422.brd	PC3-LRDIMM_V040_RC_K0_20100422_bom.pdf
Note "Reference" design file updates will be released as needed. This LRDIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated.	

Module Configuration

DIMM		SDRAM		# of SDRAMs	# of Physical Ranks	# of Address bits row/col/Bank	MO-269 variation
Capacity	Organization	Density	Organization				
8GB	1Gx72	1Gbit	256M x 4	72	4	14/11/3	AB
16GB	2Gx72	2Gbit	512M x 4	72	4	15/11/3	AB
32GB	4Gx72	4Gbit	1G x 4	72	4	16/11/3	AB

SDRAM Configuration

Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM	SDRAM Package Type	Package Type ²	MO-207 variation
9.5 x 12.5 / 10.0 x 13.0 ¹	8	78 Ball stacked FBGA	DDP	DW-z
10.5 x 11.5 / 11.0 x 12.0 ¹	8	78 Ball stacked FBGA	DDP	DW-z
Note 1 In case that DRAM to passive spacing (min) is 0.275 mm, DRAM to DRAM spacing (min) is 0.30 mm. Note 2 DDP is a dual die package				

Supported Speeds

Speed	PC3-6400	PC3-8500	PC3-10600	PC3-12800	PC3-14900	PC3-17000	Notes
DDR3	X	X	X	P			
DDR3L	X	X	X	P			

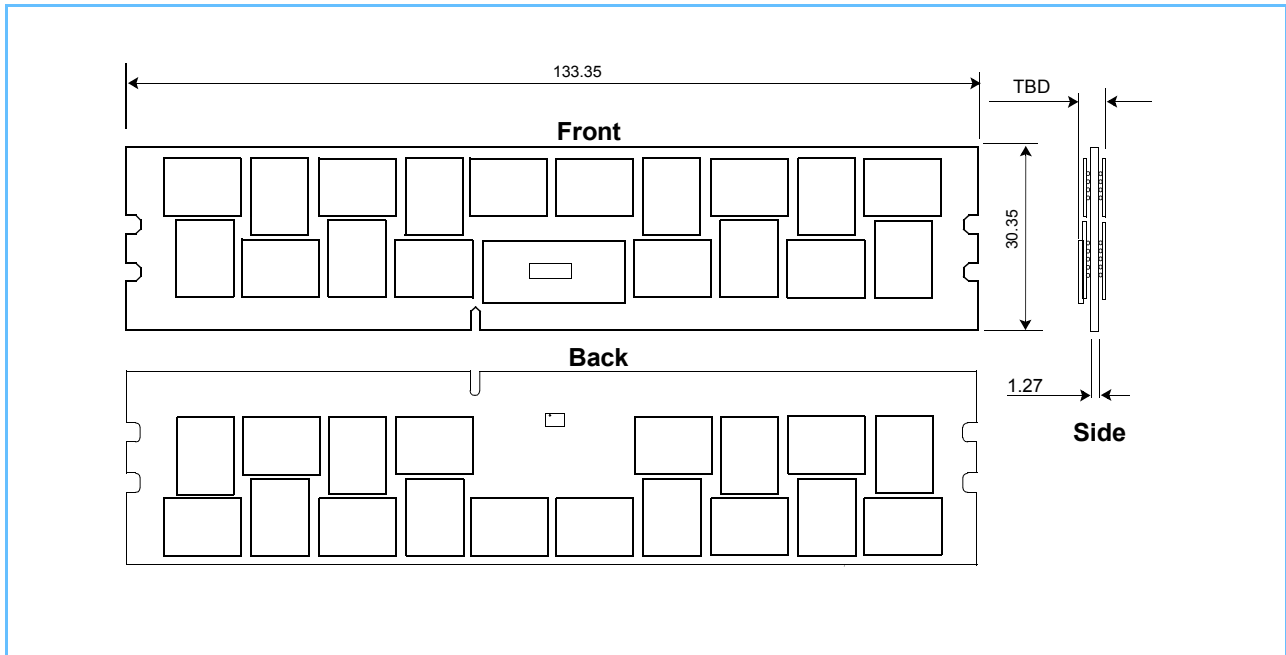
Note P means a proposed speed and voltage at committee ballot.
X will reflect passed committee ballot at the time when the specification is issued at BOD ballot

Design Rules and Deviations

- 1) This design uses blind vias.
- 2) This design places vias on a 0.65 mm grid.
- 3) This design uses 0.2 mm vias.

General Layout

x72 DIMM, populated as four physical ranks of x4 stacked DDR3 SDRAMs



Note 1 All dimension are typical unless otherwise stated. (Millimeters)

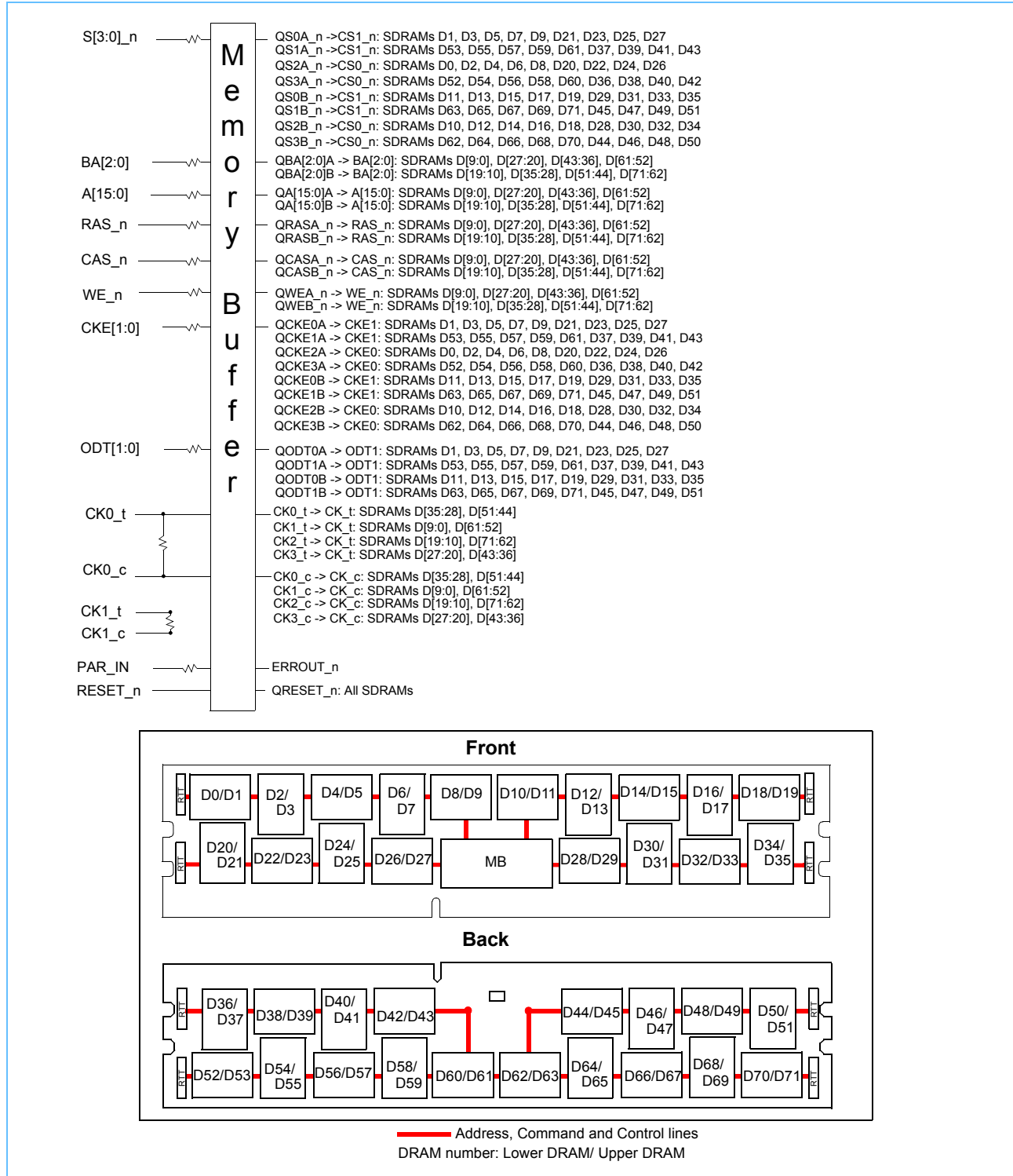
Note 2 Thermal sensor is placed within the Thermal Sensor Placement Area as defined in MO-269.

Note 3 The Memory Buffer is placed within the Memory Buffer Placement Area as defined in MO-269

Note 4 Implementation and dimensions shown without heat spreader.

Block Diagram

x72 DIMM, populated as four physical ranks of x4 stacked DDR3 SDRAMs (Part 1 of 3)

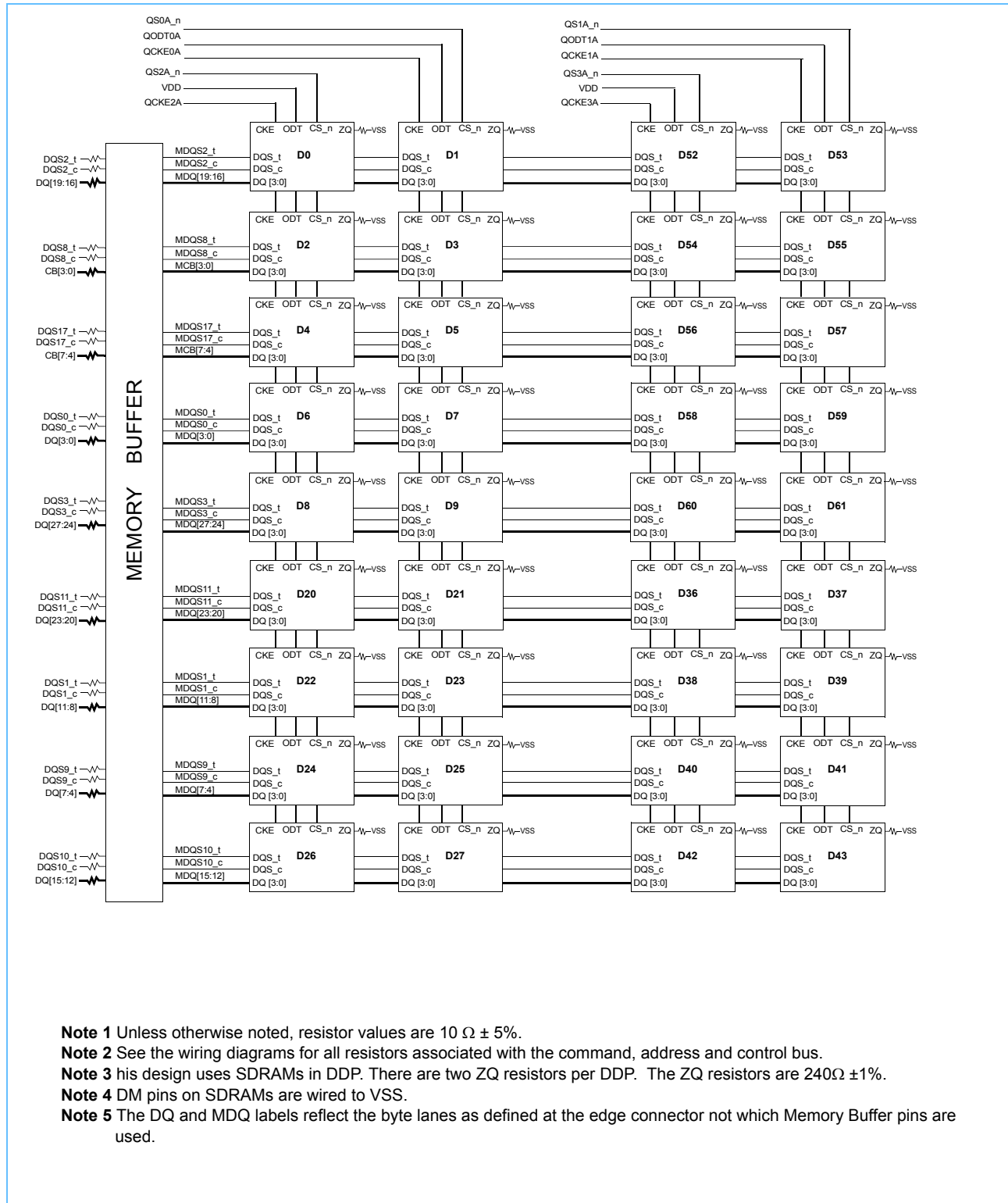


Note 1 CK0_t, CK0_c terminated with 120Ω ± 5% resistor.

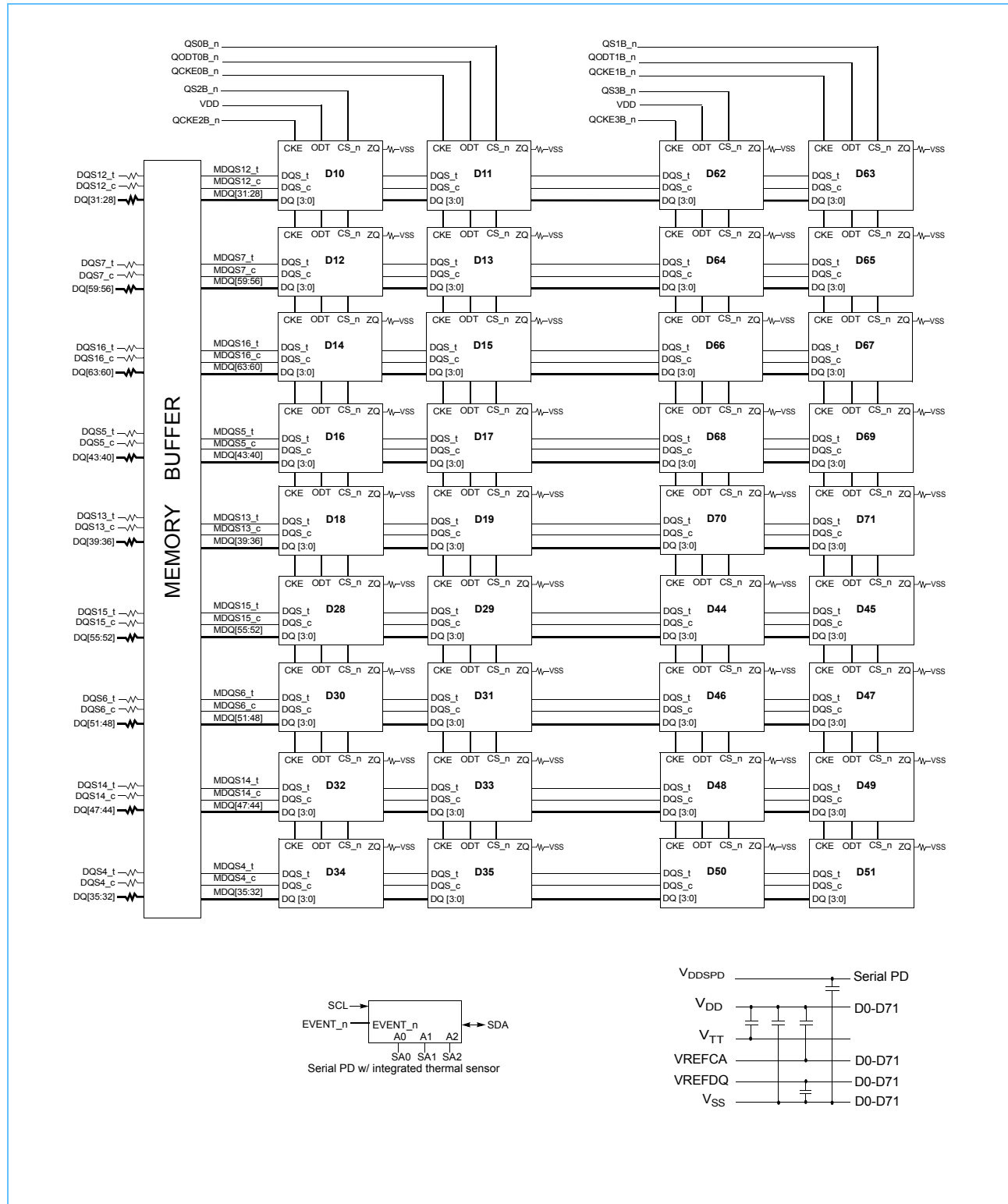
Note 2 CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.

Functional Block Diagram

x72 DIMM, populated as four physical ranks of x4 stacked DDR3 SDRAMs (Part 2 of 3)



x72 DIMM, populated as four physical ranks of x4 stacked DDR3 SDRAMs (Part 3 of 3)



Memory Buffer (MB)

Please refer to the memory buffer vendor data sheets for all technical specifications and requirements.

Component Specifications

MB Grade PC3-6400	MB Grade PC3-8500	MB Grade PC3-10600	MB Grade PC3-12800	MB Grade PC3-14900	MB Grade PC3-17000
P	P	P	P		

Input Loading Matrix

Signal Names	Input to Device	Loads
CK0_t, CK0_c	Memory Buffer	1
CK1_t, CK1_c	Termination Resistor	1
RESET_n	Memory Buffer	1
CKE0, ODT0	Memory Buffer	1 ¹
CKE1, ODT1	Memory Buffer	1 ¹
Ax, BAx, RAS_n, CAS_n, WE_n, Par_In	Memory Buffer	1 ¹
S0_n	Memory Buffer	1 ¹
S1_n	Memory Buffer	1 ¹
S2_n	Memory Buffer	1 ¹
S3_n	Memory Buffer	1 ¹
DQ, CB, DQS_t, DQS_c	Memory Buffer	1 ¹
DM, TDQS_t, TDQS_c	Memory Buffer	N/A ²
SCL, SDA, SA[2:0], EVENT_n	SPD with integrated Thermal Sensor + Memory Buffer	1 + 1 ¹
Note 1 Programmable resistive terminations are available on the Memory Buffer. Note 2 These pins mapped as the upper DQS_t and DQS_c signals.		