

4.20.25 - 260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/  
PC4-2666/PC4-3200 DDR4 SDRAM SO-DIMM Design Specification

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## DDR4 SDRAM SO-DIMM Design Specification

**Revision 1.20**

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## 1 Product Description

This specification defines the electrical and mechanical requirements for 260 pin, 1.2 V (VDD), Small Outline, Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR4 SDRAM SO-DIMMs). These DDR4 SO-DIMMs are intended for use as main memory when installed in PCs, laptops and other systems.

Reference design examples are included which provide an initial basis for DDR4 SO-DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity and thermal requirements for PC4-1600, PC4-1866, PC4-2133, PC4-2400, PC4-2666 and PC4-3200 support. All DDR4 SO-DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

This specification follows the JEDEC standard DDR4 component specification (refer to JEDEC standard JESD79-4, at [www.jedec.org](http://www.jedec.org)).

**Table 1 — Product Family Attributes**

|                                                      |                                               |                                                                                                                                                                                    |
|------------------------------------------------------|-----------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DIMM Organization                                    | x64, x72 ECC                                  | Notes                                                                                                                                                                              |
| DIMM Dimensions (nominal)                            | 69.6 mm x 30.0 mm                             | Refer to MO-310<br>2 mm wider than DDR3                                                                                                                                            |
| Pin Count and Pitch                                  | 260 on 0.5 mm centers                         |                                                                                                                                                                                    |
| DDR4 SDRAMs Supported                                | 4 Gb, 8 Gb, 12 Gb, 16 Gb, 24 Gb, 32 Gb, 64 Gb | 78/106-ball FBGA package for x8 and 96/112-ball FBGA for x16 devices.<br>Refer to MO-207:<br>x8 variations DT-z, DW-z<br>x16 variations DU-z, DY-z                                 |
| Capacity                                             | 2 GB - 256 GB                                 | SDP - 32 GB max, 3DS -256 GB max                                                                                                                                                   |
| DDR4 SDRAM width                                     | x8, x16                                       |                                                                                                                                                                                    |
| Serial Presence Detect, Thermal Sensor (SPD-TSE/SPD) | 512 byte                                      | See EE1004-v and TSE2004av specifications                                                                                                                                          |
| Voltage Options                                      | PC4 - 1.2 V for VDD                           | All DDR4 modules use a common VDD–VDDQ power plane. They are tied together on the DIMM, but by standard definition are supported on the pinout to accommodate future enhancements. |
|                                                      | PC4 - 0.6 V for VTT                           | Termination voltage for Address, Command, and Control.                                                                                                                             |
|                                                      | 2.5 V for VPP                                 | This supply has VSS as its return path. On DIMM It is treated as a separate supply from VDDSPD.                                                                                    |
|                                                      | 2.5 V or 3.3 V for VDDSPD                     | SPD supply is operable with 2.5 V or 3.3 V.                                                                                                                                        |
| Interface                                            | 1.2 V signaling                               |                                                                                                                                                                                    |

## 2 Environmental Requirements

DDR4 SO-DIMMs are intended for use in mobile computing environments that have limited capacity for heat dissipation. These will typically be non-ECC SO-DIMMs.

DDR4 SO-DIMMs that have ECC support are intended for use in standard office environments that have limited capacity for heating and air conditioning.

**Table 2 — Environmental Parameters**

| Symbol                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Parameter                                 | Rating      | Units | Notes |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|-------------|-------|-------|
| T <sub>OPR</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Operating Temperature (ambient)           | 0 to +55    | °C    | 3     |
| H <sub>OPR</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Operating Humidity (relative)             | 10 to 90    | %     |       |
| T <sub>STG</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Storage Temperature                       | -50 to +100 | °C    | 1     |
| H <sub>STG</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Storage Humidity (without condensation)   | 5 to 95     | %     | 1     |
| P <sub>BAR</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Barometric Pressure (operating & storage) | 105 to 69   | kPa   | 1, 2  |
| <b>Note 1</b> Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.<br><b>Note 2</b> Up to 9850 ft.<br><b>Note 3</b> The component maximum case temperature (T <sub>CASE</sub> ) shall not exceed the value specified in the DDR4 DRAM component specification. |                                           |             |       |       |

### 3 Connector Pinout and Signal Description

**Table 3 — Connector Pin Definition**

| Pin Name                                                                                                                                                                                                      | Description                                                 | Pin Name           | Description                                                      |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------|--------------------|------------------------------------------------------------------|
| A0–A16                                                                                                                                                                                                        | SDRAM address bus                                           | SCL                | I <sup>2</sup> C serial bus clock for SPD/TS                     |
| BA0, BA1                                                                                                                                                                                                      | SDRAM bank select                                           | SDA                | I <sup>2</sup> C serial bus data line for SPD/TS                 |
| BG0, BG1                                                                                                                                                                                                      | SDRAM bank group select                                     | SA0–SA2            | I <sup>2</sup> C slave address select for SPD/TS                 |
| RAS <sub>n</sub> <sup>1</sup>                                                                                                                                                                                 | SDRAM row address strobe                                    | PARITY             | SDRAM parity input                                               |
| CAS <sub>n</sub> <sup>2</sup>                                                                                                                                                                                 | SDRAM column address strobe                                 | VDD                | SDRAM I/O & core power supply                                    |
| WE <sub>n</sub> <sup>3</sup>                                                                                                                                                                                  | SDRAM write enable                                          | VPP                | SDRAM activating power supply                                    |
| CS0 <sub>n</sub> , CS1 <sub>n</sub><br>CS2 <sub>n</sub> , CS3 <sub>n</sub>                                                                                                                                    | Rank Select Lines                                           | C0, C1             | Chip ID lines for 3DS components                                 |
| CKE0, CKE1                                                                                                                                                                                                    | SDRAM clock enable lines                                    | VREFCA             | SDRAM command/address reference supply                           |
| ODT0, ODT1                                                                                                                                                                                                    | SDRAM on-die termination control lines                      | VSS                | Power supply return (ground)                                     |
| ACT <sub>n</sub>                                                                                                                                                                                              | SDRAM activate                                              | VDDSPD             | Serial SPD/TS positive power supply                              |
| DQ0–DQ63                                                                                                                                                                                                      | DIMM memory data bus                                        | ALERT <sub>n</sub> | SDRAM ALERT <sub>n</sub>                                         |
| CB0–CB7                                                                                                                                                                                                       | DIMM ECC check bits                                         |                    |                                                                  |
| DQS0 <sub>t</sub> –DQS8 <sub>t</sub>                                                                                                                                                                          | SDRAM data strobes<br>(positive line of differential pair)  | RESET <sub>n</sub> | Set SDRAMs to a Known State                                      |
| DQS0 <sub>c</sub> –DQS8 <sub>c</sub>                                                                                                                                                                          | SDRAM data strobes<br>(negative line of differential pair)  | EVENT <sub>n</sub> | SPD signals a thermal event has occurred.                        |
| DM0 <sub>n</sub> –DM8 <sub>n</sub> ,<br>DBI0 <sub>n</sub> –DBI8 <sub>n</sub>                                                                                                                                  | SDRAM data masks/data bus inversion<br>(x8-based x72 DIMMs) | VTT                | Termination supply for the Address, Com-<br>mand and Control bus |
| CK0 <sub>t</sub> , CK1 <sub>t</sub>                                                                                                                                                                           | SDRAM clocks (positive line of differential<br>pair)        | NC                 | No connection                                                    |
| CK0 <sub>c</sub> , CK1 <sub>c</sub>                                                                                                                                                                           | SDRAM clocks (negative line of differential<br>pair)        |                    |                                                                  |
| <b>Note 1</b> RAS <sub>n</sub> is a multiplexed function with A16.<br><b>Note 2</b> CAS <sub>n</sub> is a multiplexed function with A15.<br><b>Note 3</b> WE <sub>n</sub> is a multiplexed function with A14. |                                                             |                    |                                                                  |

**Table 4 — Input/Output Functional Description**

| Symbol                               | Type             | I/O Level | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------------------------------------|------------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CK0_t, CK0_c<br>CK1_t, CK1_c         | Input            | VDD       | Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| CKE0, CKE1                           | Input            | VDD       | Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE, are disabled during power-down. Input buffers,excluding CKE, are disabled during Self-Refresh. |
| CS0_n, CS1_n<br>CS2_n, CS3_n         | Input            | VDD       | Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| C0, C1                               | Input            | VDD       | Chip ID : Chip ID is only used for 3DS for 2and4 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| ODT0, ODT1                           | Input            | VDD       | On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/, signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| ACT_n                                | Input            | VDD       | Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| RAS_n/A16.<br>CAS_n/A15.<br>WE_n/A14 | Input            | VDD       | Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table                                                                                                                                                                                                                                                                                                                                           |
| DM_n/DBI_n                           | Input/<br>Output | VDD       | Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH.                                                                                                                                                                                                                               |
| BG0 - BG1                            | Input            | VDD       | Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. For x4/x8 based SDRAMs, BG0 and BG1 are valid. For x16 based SDRAM components only BG0 is valid.                                                                                                                                                                                                                                                                                                                                                                                                             |
| BA0 - BA1                            | Input            | VDD       | Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| A0 - A16                             | Input            | VDD       | Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands.                                                                                                                                                                                                                                                                                                                                             |
| A10 / AP                             | Input            | VDD       | Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.                                                                                                                                                                                                                                                                         |

**Table 4 — Input/Output Functional Description (Cont'd)**

| Symbol           | Type          | I/O Level | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------------------|---------------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A12 / BC_n       | Input         | VDD       | Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.                                                                                                                                                                                                                                                                                                          |
| RESET_n          | CMOS Input    | VDD       | Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.                                                                                                                                                                                                                                                                                                                                                               |
| DQ               | Input/ Output | VDD       | Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific datasheets to determine which DQ is used.                                                                                                                                                                                                   |
| DQS_t, DQS_c     | Input/ Output | VDD       | Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR4 SDRAMs support differential data strobe only and does not support single-ended.                                                                                                                                                                                                                                                                                                               |
| PARITY           | Input         | VDD       | Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then SDRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A16-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW                                                                                                                                                  |
| ALERT_n          | Output        | VDD       | ALERT: It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction is complete. Using this signal or not is dependent on the system. This is an open drain signal. It requires a pullup resistor on the system. |
| EVENT_n          | Output        | VDDSPD    | I2C thermal event indicator. Open drain, requires a pullup resistor on the system.                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| SAVE_n           | Input/ Output | -         | Not used on SODIMMs. SODIMMs will have no connection to this pin. See specifications of NVDIMMs for signal description.                                                                                                                                                                                                                                                                                                                                                                                            |
| SCL              | Input         | VDDSPD    | Bus clock used to strobe data into and out of I2C devices. Open drain and requires a pullup resistor on the system.                                                                                                                                                                                                                                                                                                                                                                                                |
| SDA              | Input/ Output | VDDSPD    | I2C data. Open drain and requires a pullup resistor on the system.                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| SA0-SA2          | Input         | VDDSPD    | Device address for the SPD.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| RFU              |               |           | Reserved for Future Use. No on DIMM electrical connection is present.                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| NC               |               |           | No Connect: No on DIMM electrical connection is present.                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| VDD <sup>1</sup> | Supply        |           | Power Supply: 1.2 V +/- 0.06 V                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| VSS              | Supply        |           | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| VTT <sup>2</sup> | Supply        |           | Power Supply: 0.6 V                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| VPP              | Supply        |           | DRAM Activating Power Supply: 2.5 V (2.375 V min, 2.75 V max)                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| VREFCA           | Supply        |           | Reference voltage for CA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| VDDSPD           | Supply        |           | Power supply used to power the I2C bus on the SPD.                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

### 3.1 DDR4 SO-DIMM Connector Pin Assignments

**Table 5 — DDR4 SO-DIMM 260 Pin Connector Pin Wiring Assignments**

| Front Side<br>Pin Label | Pin | Pin | Back side<br>Pin Label | Front Side<br>Pin Label | Pin | Pin | Back side<br>Pin Label |
|-------------------------|-----|-----|------------------------|-------------------------|-----|-----|------------------------|
| VSS                     | 1   | 2   | VSS                    | A3                      | 131 | 132 | A2                     |
| DQ5                     | 3   | 4   | DQ4                    | A1                      | 133 | 134 | EVENT_n                |
| VSS                     | 5   | 6   | VSS                    | VDD                     | 135 | 136 | VDD                    |
| DQ1                     | 7   | 8   | DQ0                    | CK0_t                   | 137 | 138 | CK1_t                  |
| VSS                     | 9   | 10  | VSS                    | CK0_c                   | 139 | 140 | CK1_c                  |
| DQS0_c                  | 11  | 12  | DM0_n, DBI0_n, NC      | VDD                     | 141 | 142 | VDD                    |
| DQS0_t                  | 13  | 14  | VSS                    | PARITY                  | 143 | 144 | A0                     |
| VSS                     | 15  | 16  | DQ6                    | <b>KEY</b>              |     |     |                        |
| DQ7                     | 17  | 18  | VSS                    | BA1                     | 145 | 146 | A10/AP                 |
| VSS                     | 19  | 20  | DQ2                    | VDD                     | 147 | 148 | VDD                    |
| DQ3                     | 21  | 22  | VSS                    | CS0_n                   | 149 | 150 | BA0                    |
| VSS                     | 23  | 24  | DQ12                   | A14/WE_n                | 151 | 152 | A16/RAS_n              |
| DQ13                    | 25  | 26  | VSS                    | VDD                     | 153 | 154 | VDD                    |
| VSS                     | 27  | 28  | DQ8                    | ODT0                    | 155 | 156 | A15/CAS_n              |
| DQ9                     | 29  | 30  | VSS                    | CS1_n                   | 157 | 158 | A13                    |
| VSS                     | 31  | 32  | DQS1_c                 | VDD                     | 159 | 160 | VDD                    |
| DM1_n, DBI1_n, NC       | 33  | 34  | DQS1_t                 | ODT1                    | 161 | 162 | C0, CS2_n, NC          |
| VSS                     | 35  | 36  | VSS                    | VDD                     | 163 | 164 | VREFCA                 |
| DQ15                    | 37  | 38  | DQ14                   | C1, CS3_n, NC           | 165 | 166 | SA2                    |
| VSS                     | 39  | 40  | VSS                    | VSS                     | 167 | 168 | VSS                    |
| DQ10                    | 41  | 42  | DQ11                   | DQ37                    | 169 | 170 | DQ36                   |
| VSS                     | 43  | 44  | VSS                    | VSS                     | 171 | 172 | VSS                    |
| DQ21                    | 45  | 46  | DQ20                   | DQ33                    | 173 | 174 | DQ32                   |
| VSS                     | 47  | 48  | VSS                    | VSS                     | 175 | 176 | VSS                    |
| DQ17                    | 49  | 50  | DQ16                   | DQS4_c                  | 177 | 178 | DM4_n, DBI4_n, NC      |
| VSS                     | 51  | 52  | VSS                    | DQS4_t                  | 179 | 180 | VSS                    |
| DQS2_c                  | 53  | 54  | DM2_n, DBI2_n, NC      | VSS                     | 181 | 182 | DQ39                   |
| DQS2_t                  | 55  | 56  | VSS                    | DQ38                    | 183 | 184 | VSS                    |
| VSS                     | 57  | 58  | DQ22                   | VSS                     | 185 | 186 | DQ35                   |
| DQ23                    | 59  | 60  | VSS                    | DQ34                    | 187 | 188 | VSS                    |
| VSS                     | 61  | 62  | DQ18                   | VSS                     | 189 | 190 | DQ45                   |
| DQ19                    | 63  | 64  | VSS                    | DQ44                    | 191 | 192 | VSS                    |
| VSS                     | 65  | 66  | DQ28                   | VSS                     | 193 | 194 | DQ41                   |
| DQ29                    | 67  | 68  | VSS                    | DQ40                    | 195 | 196 | VSS                    |
| VSS                     | 69  | 70  | DQ24                   | VSS                     | 197 | 198 | DQS5_c                 |
| DQ25                    | 71  | 72  | VSS                    | DM5_n, DBI5_n, NC       | 199 | 200 | DQS5_t                 |
| VSS                     | 73  | 74  | DQS3_c                 | VSS                     | 201 | 202 | VSS                    |
| DM3_n, DBI3_n, NC       | 75  | 76  | DQS3_t                 | DQ46                    | 203 | 204 | DQ47                   |
| VSS                     | 77  | 78  | VSS                    |                         |     |     |                        |

**Table 5 — DDR4 SO-DIMM 260 Pin Connector Pin Wiring Assignments (Cont'd)**

| Front Side<br>Pin Label | Pin | Pin | Back side<br>Pin Label | Front Side<br>Pin Label | Pin | Pin | Back side<br>Pin Label |
|-------------------------|-----|-----|------------------------|-------------------------|-----|-----|------------------------|
| DQ30                    | 79  | 80  | DQ31                   | VSS                     | 205 | 206 | VSS                    |
| VSS                     | 81  | 82  | VSS                    | DQ42                    | 207 | 208 | DQ43                   |
| DQ26                    | 83  | 84  | DQ27                   | VSS                     | 209 | 210 | VSS                    |
| VSS                     | 85  | 86  | VSS                    | DQ52                    | 211 | 212 | DQ53                   |
| CB5, NC                 | 87  | 88  | CB4, NC                | VSS                     | 213 | 214 | VSS                    |
| VSS                     | 89  | 90  | VSS                    | DQ49                    | 215 | 216 | DQ48                   |
| CB1, NC                 | 91  | 92  | CB0, NC                | VSS                     | 217 | 218 | VSS                    |
| VSS                     | 93  | 94  | VSS                    | DQS6_c                  | 219 | 220 | DM6_n, DBI6_n, NC      |
| DQS8_c                  | 95  | 96  | DM8_n, DBI8_n, NC      | DQS6_t                  | 221 | 222 | VSS                    |
| DQS8_t                  | 97  | 98  | VSS                    | VSS                     | 223 | 224 | DQ54                   |
| VSS                     | 99  | 100 | CB6, NC                | DQ55                    | 225 | 226 | VSS                    |
| CB2, NC                 | 101 | 102 | VSS                    | VSS                     | 227 | 228 | DQ50                   |
| VSS                     | 103 | 104 | CB7, NC                | DQ51                    | 229 | 230 | VSS                    |
| CB3, NC                 | 105 | 106 | VSS                    | VSS                     | 231 | 232 | DQ60                   |
| VSS                     | 107 | 108 | RESET_n                | DQ61                    | 233 | 234 | VSS                    |
| CKE0                    | 109 | 110 | CKE1                   | VSS                     | 235 | 236 | DQ57                   |
| VDD                     | 111 | 112 | VDD                    | DQ56                    | 237 | 238 | VSS                    |
| BG1                     | 113 | 114 | ACT_n                  | VSS                     | 239 | 240 | DQS7_c                 |
| BG0                     | 115 | 116 | ALERT_n                | DM7_n, DBI7_n, NC       | 241 | 242 | DQS7_t                 |
| VDD                     | 117 | 118 | VDD                    | VSS                     | 243 | 244 | VSS                    |
| A12                     | 119 | 120 | A11                    | DQ62                    | 245 | 246 | DQ63                   |
| A9                      | 121 | 122 | A7                     | VSS                     | 247 | 248 | VSS                    |
| VDD                     | 123 | 124 | VDD                    | DQ58                    | 249 | 250 | DQ59                   |
| A8                      | 125 | 126 | A5                     | VSS                     | 251 | 252 | VSS                    |
| A6                      | 127 | 128 | A4                     | SCL                     | 253 | 254 | SDA                    |
| VDD                     | 129 | 130 | VDD                    | VDDSPD                  | 255 | 256 | SA0                    |
|                         |     |     |                        | VPP                     | 257 | 258 | VTT                    |
|                         |     |     |                        | VPP                     | 259 | 260 | SA1                    |

## 4 Power Details

### 4.1 DIMM Voltage Requirements

The DIMM voltage requirements and the SDRAM voltage requirements are not identical. There must be some allowance for a small voltage drop across the DIMM. Table 6 defines the requirements for the Host at the DIMM socket.

Some modules have lower current requirements. Any specific module must meet the SDRAM voltage requirements for its worst case supply currents.

**Table 6 — DDR4 SO-DIMM DC Operating Voltage<sup>1,2,3</sup> - 1.2 V operation**

| Symbol           | Parameter                 | Voltage Rating (V) |                      |         | Maximum Expected Current (AMPs) | Power State |
|------------------|---------------------------|--------------------|----------------------|---------|---------------------------------|-------------|
|                  |                           | Minimum            | Typical <sup>4</sup> | Maximum |                                 |             |
| VDD              | Supply Voltage            | 1.16               | 1.21                 | 1.26    | 5.0                             | Operational |
| VPP              | Activation Supply Voltage | 2.41               | 2.50                 | 2.75    | 1.5                             | Operational |
| VTT <sup>5</sup> | Termination Voltage       | 0.565              | 0.605                | 0.64    | 0.5                             | Operational |
| VDDSPD           | SPD Supply Voltage        | 2.41               | 2.5                  | 2.75    | 0.1                             | Operational |

**Note 1** 20 MHz bandwidth limited measurement for all voltages in the table.

**Note 2** Voltages are measured at the DIMM gold fingers.

**Note 3** The SDRAM specification must be met and take precedence over this document.

**Note 4** Typical voltage is platform dependent, suggested value only.

**Note 5** At the DIMM interface VTT is the only voltage during normal operating conditions that can both source and sink current.

**Note 6** SDRAM VDD specification range.

## 4.2 Rules for Power-Up Sequence

The timing characteristics are illustrated in Figure 1.

VPP is the point of reference for the power on sequence. Note the following points of interest:

1. VDDSPD is an independent power source which has no specific relationship to the other power sources.
2. VTT has a specific relationship to VDD:  $V_{TT} = V_{DD}/2$ .

The CK\_t/CK\_c input signals must be driven LOW throughout the VDD power ramp at least until the VDD supply voltage has settled to its final value.

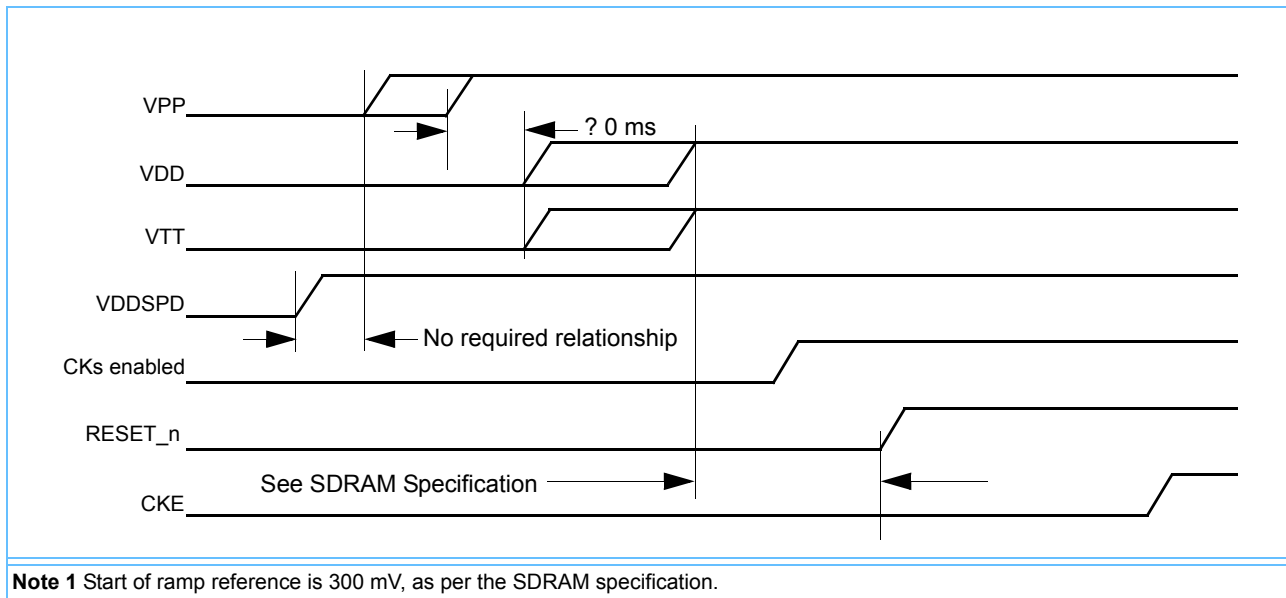


**Figure 1 — Graphical View of Recommended Power Sequence**

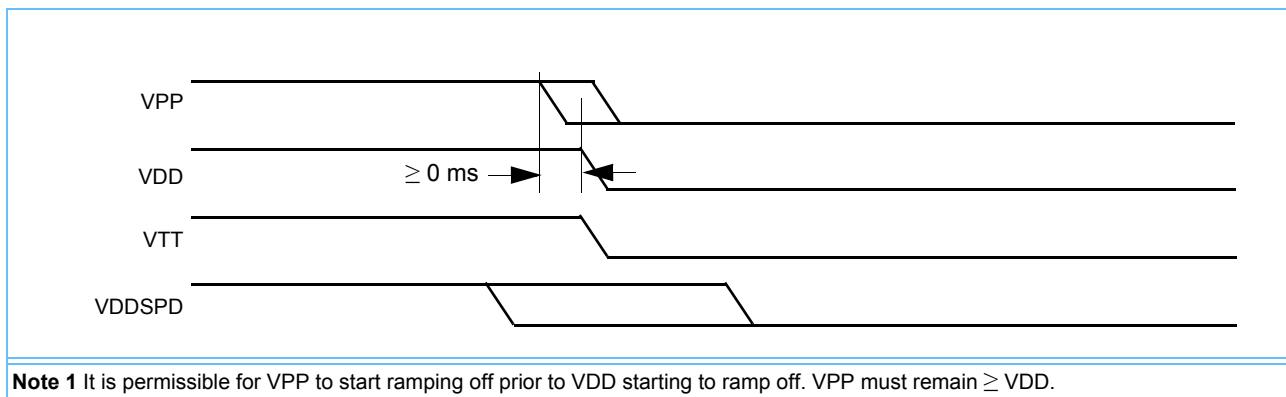


**Figure 2 — Graphical View of Recommended Power Down Sequence**

### 4.3 Feed Through Voltage (VFT)

The normal power down sequence requires the voltage relationships established during power on be maintained. VFT is defined as the voltage delta between VSS and the associated power plane with no power applied to that plane. The absolute value of this voltage must remain less than 200 mV ( $|VFT| \leq 0.20 \text{ V}$ ), which is less than the 300 mV DRAM ramp reference level for start or end of voltage ramp.