

Annex A - Raw Card A

DDR4 Small Outline DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
A0	PC4-SODIMM_V090_RC_A0_20131025.brd	PC4-SODIMM_V090_RC_A0_20140131-BOM.xlsx
A1	PC4-SODIMM_V200_RC_A1_20141015.brd	PC4-SODIMM_V090_RC_A1_20141015-BOM.docx

Note 1 "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.

Module Configuration

DIMM		SDRAM		# of SDRAM die	# of Package Ranks	# of Address bits row/col	MO-310 variation
Maximum Capacity	Organization	Die Density	Organization				
2 GB	256 Mx64	2 Gb	256 M x 8	8	1	14/10 ¹	AAxA
4 GB	512 Mx64	4 Gb	512 M x 8	8	1	15/10 ¹	AAxA
8 GB	1 Gx64	8 Gb	1 G x 8	8	1	16/10 ¹	AAxA
16 GB	2 Gx64	16 Gb	2 G x 8	8	1	17/10	AAxA

Note 1 Address A16 is the highest address bit used based on it being multiplexed with RAS_n.

SDRAM Configuration

Raw Card	Supported DRAM Outline (Width x Length) nom.	# of Banks in SDRAM BA/BG	SDRAM Package Type	Package Type	MO-207 variation
A0	10.0 x 13.0	2/2	78 Ball FBGA	SDP	DW-z
A1	9.0 x 13.0	2/2	78 Ball FBGA	SDP	DW-z

Note 1 SDP is a single die per package

Supported Speeds

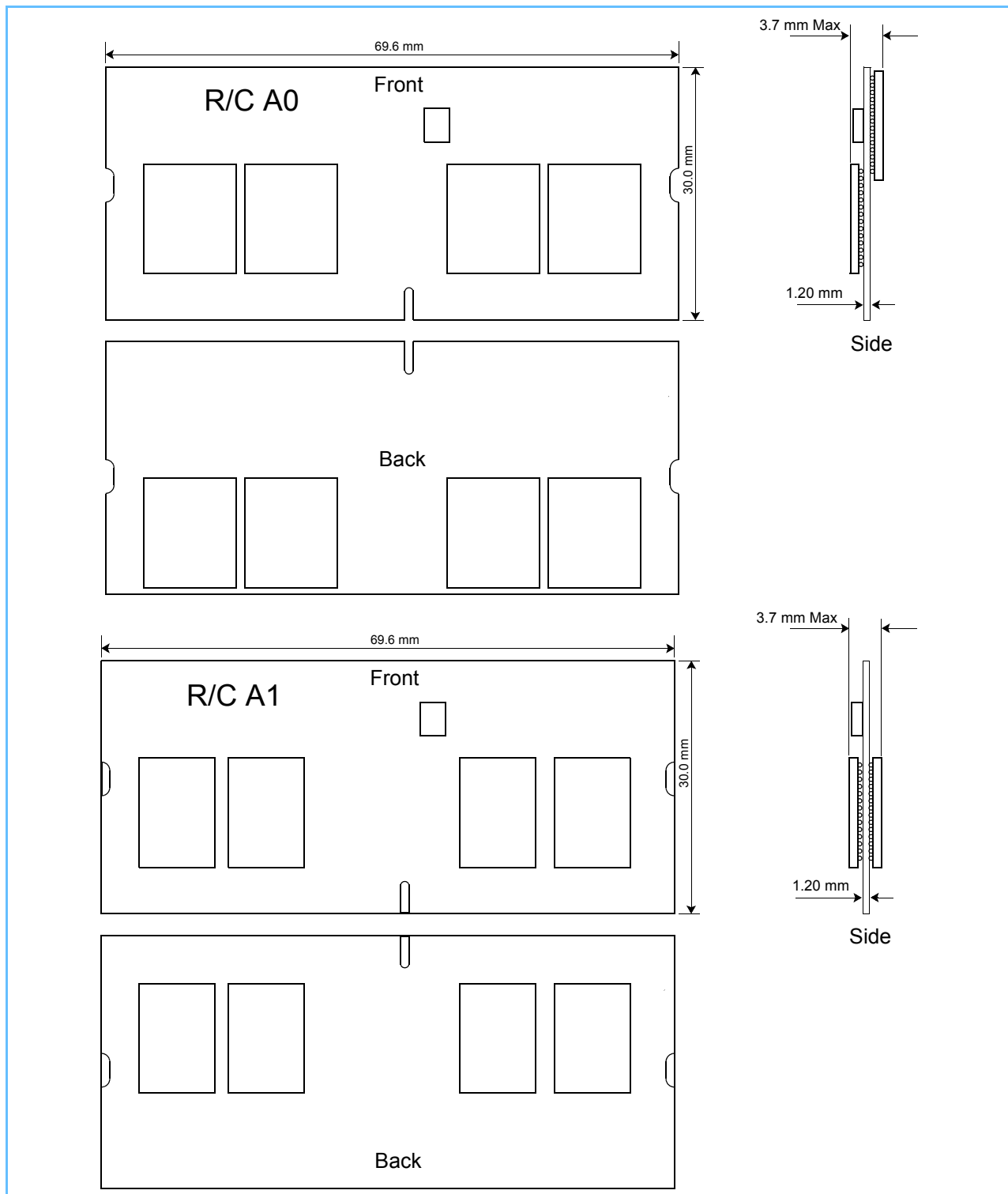
Raw Card	PC4-1333	PC4-1600	PC4-1866	PC4-2133	PC4-2400	PC4-2666	PC4-3200	Notes
A0	X	X	X	X				1, 2
A1	X	X	X	X	X	N		1, 2

Note 1 X reflects speed grades approved from previously.
Note 2 N denotes NEW speed grades.

Design Deviations

Note 1 R/C A1 - Uses double drop for some CA connections. Not covered in the Common section.
Note 2 R/C A1 - Does not follow the CK to Byte lane order used for most of the SODIMMs.

General Layout

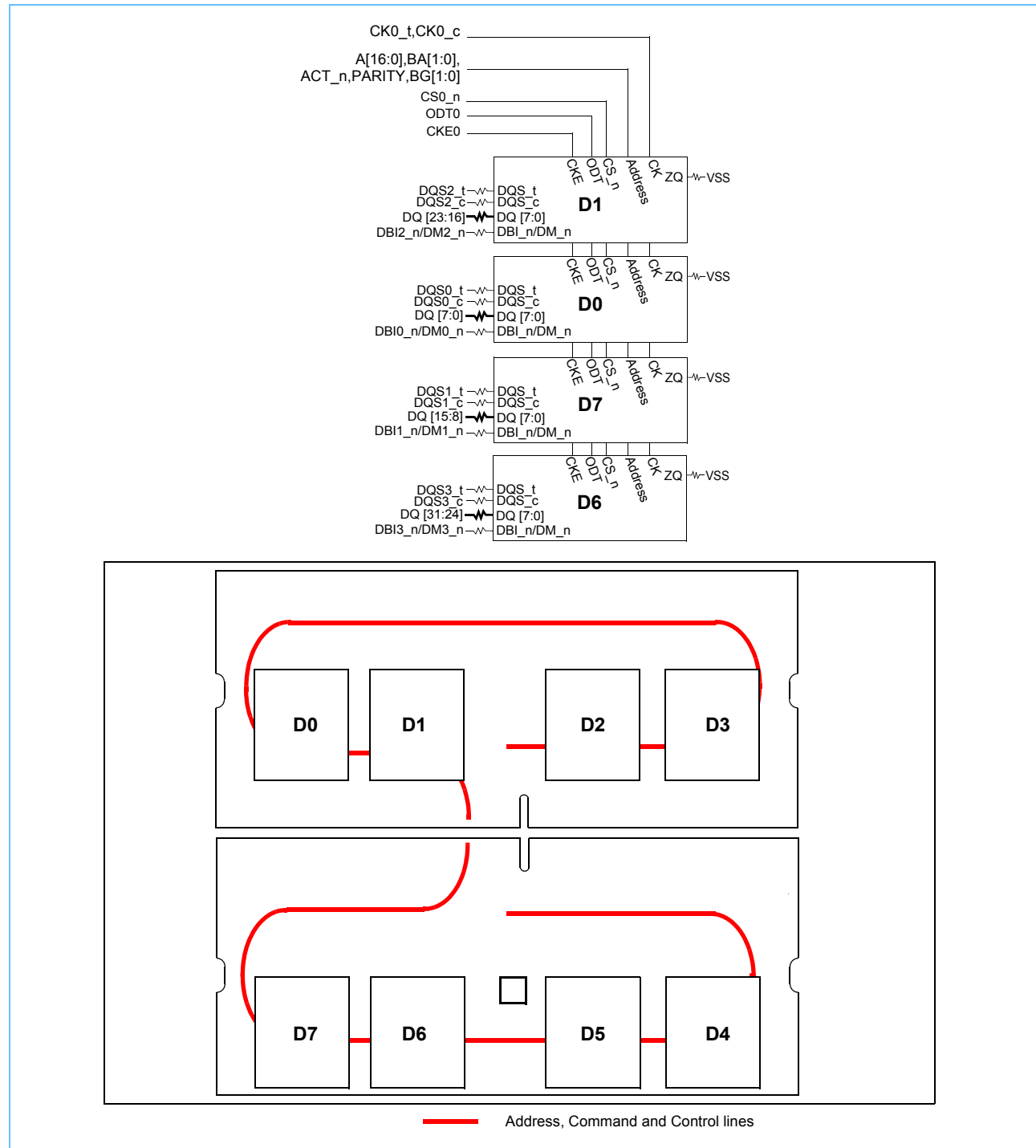


Note 1 Refer to MO-310 for more detailed information.

Note 2 Variation is AAxA (A-Module height, A-Module thickness, x-plating, A-DDR4 keying).

Functional Block Diagram

R/C A0 - x64 SO-DIMM, one package rank of x8 DDR4 SDRAMs (Part 1 of 4)

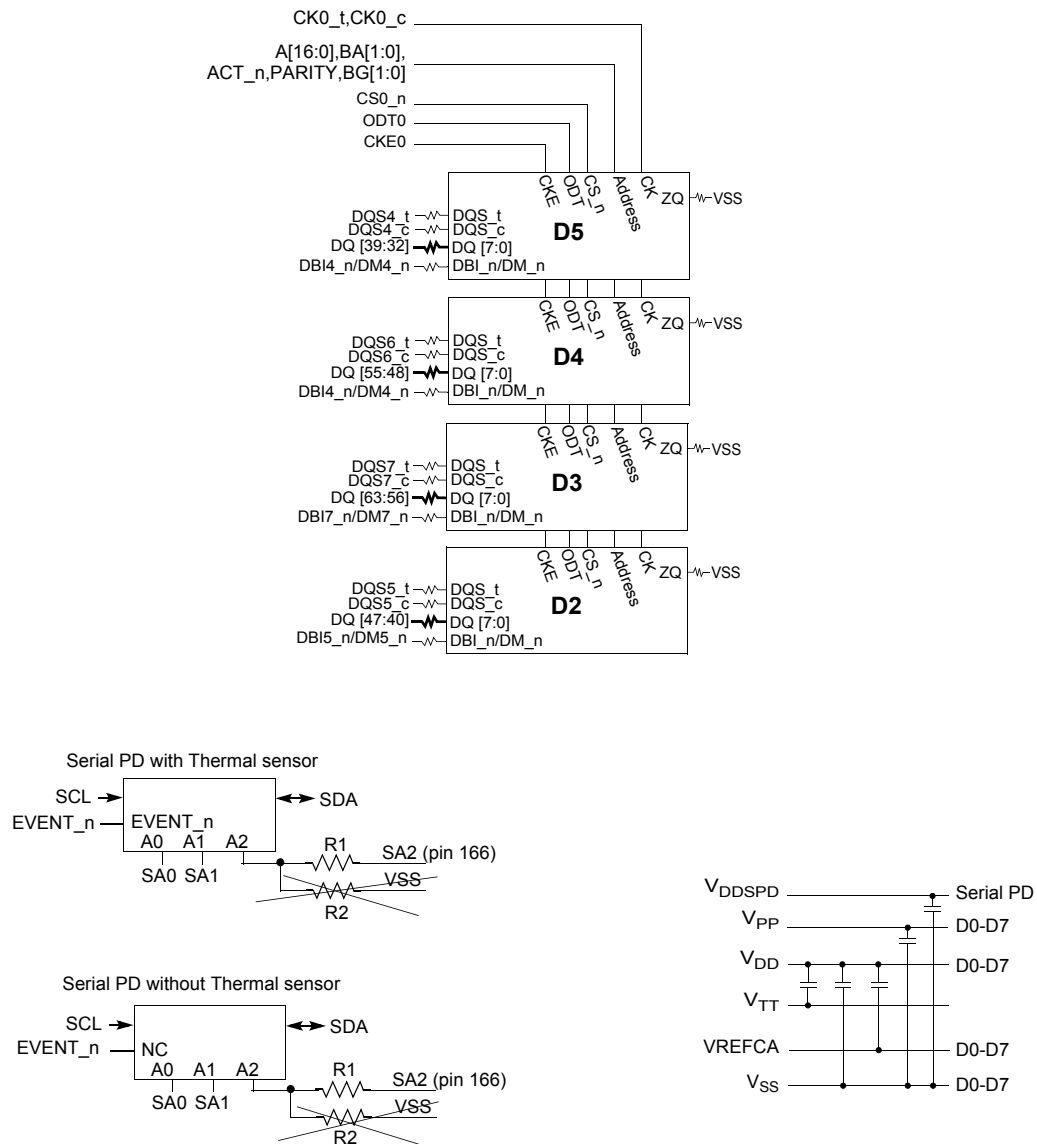


Note 1 Unless otherwise noted, resistor values are $15\ \Omega \pm 5\%$.

Note 2 ZQ resistors are $240\ \Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.

Functional Block Diagram

R/C A0 - x64 SO-DIMM, one package rank of x8 DDR4 SDRAMs (Part 2 of 4)



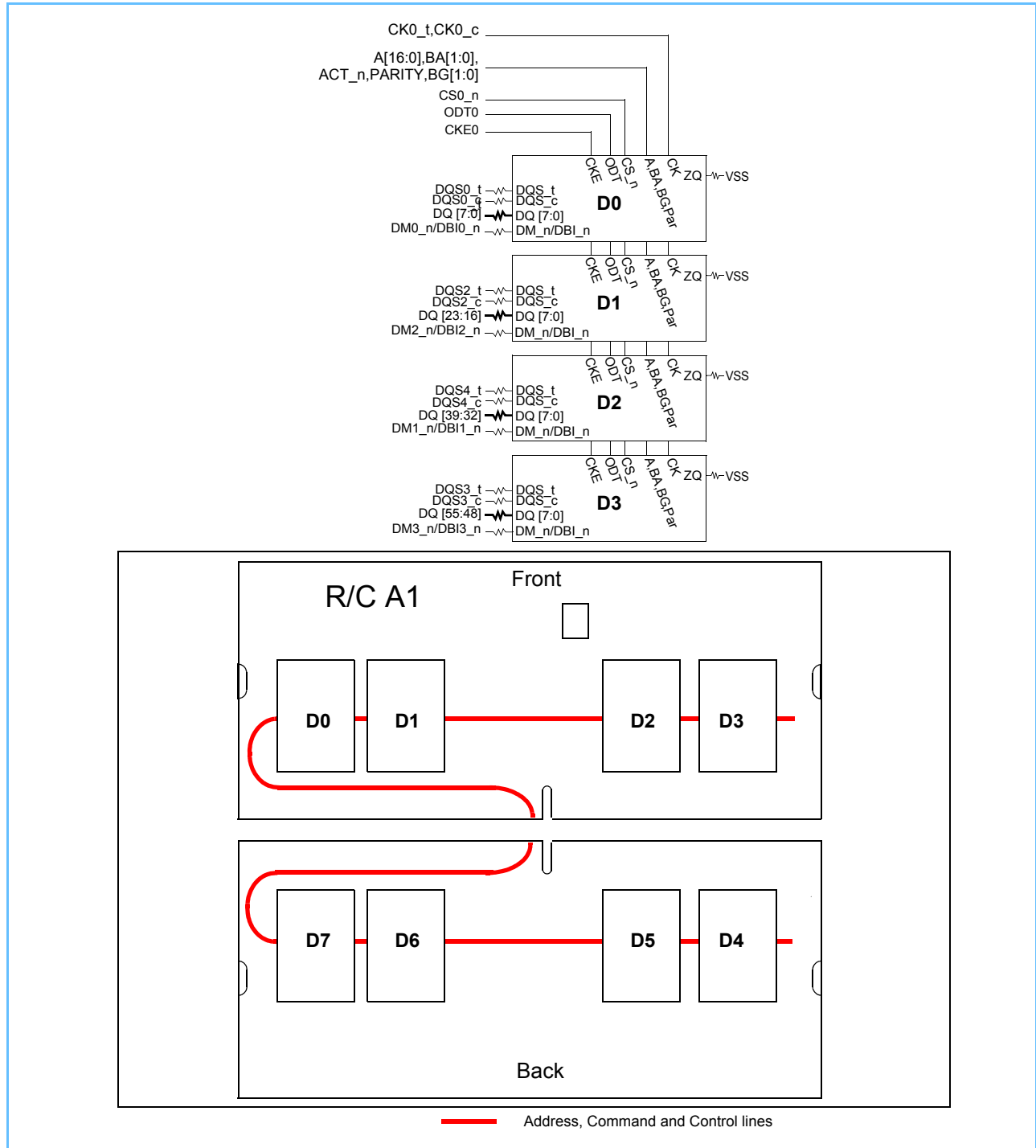
Note 1 Unless otherwise noted, resistor values are $15 \Omega \pm 5\%$.

Note 2 ZQ resistors are $240 \Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.

Note 3 To connect the SPD A2 input to the edge connector pin 166 install R1. SPD input A2 should not be tied to GND.

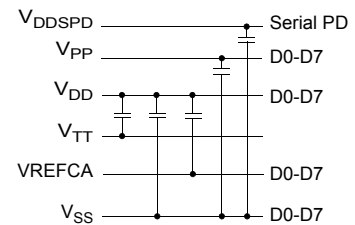
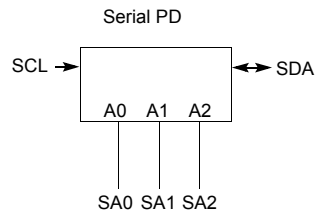
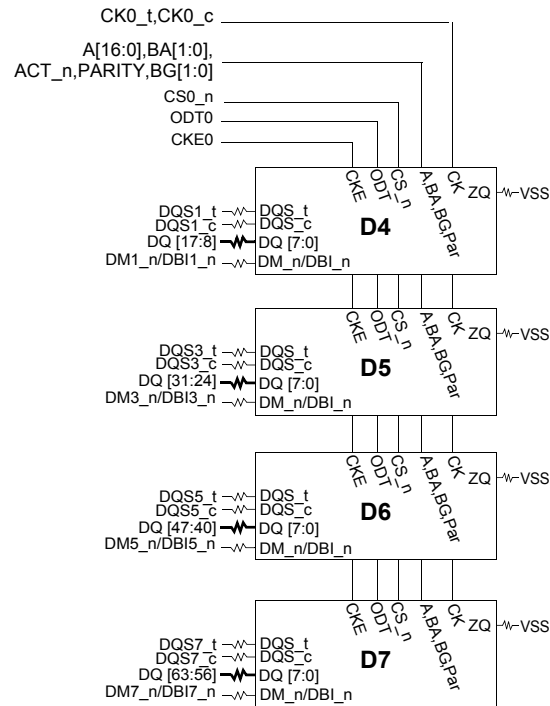
Functional Block Diagram

R/C A1 - x64 SO-DIMM, one package rank of x8 DDR4 SDRAMs (Part 3 of 4)



Functional Block Diagram

R/C A1 - x64 SO-DIMM, one package rank of x8 DDR4 SDRAMs (Part 4 of 4)



Note 1 Unless otherwise noted, resistor values are $15\ \Omega \pm 5\%$.

Note 2 ZQ resistors are $240\ \Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.