

Annex B - Raw Card B

DDR4 SODIMM Design File

Raw Card	Applicable Design File	Applicable BOM
B0	The B0 design is obsolete. Please use the B1 design.	
B1	PC4-SODIMM_V100_RC_B1_20141219.brd	PC4-SODIMM_V100_RC_B0_20151028_BOM.docx

Note 1 "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.

Module Configuration

SDRAM			DIMM					
Die Density	Die Organization	Package Type	# of Package Ranks per DIMM	# of SDRAM die per DIMM	Capacity per DIMM	Organization of DIMM	# of Address bits row/col	MO-310 variation
2 Gb	256M x 8	SDP	2	16	4 GB	512M x 64	14/10 ¹	AAxA
4 Gb	512M x 8	SDP	2	16	8 GB	1G x 64	15/10 ¹	AAxA
8 Gb	1G x 8	SDP	2	16	16 GB	2G x 64	16/10	AAxA
16 Gb	2G x 8	SDP	2	16	32 GB	4G x64	17/10	AAxA

Note 1 Address A16 is the highest address bit used based on it being multiplexed with RAS_n.

SDRAM Configuration

Supported DRAM Outline (Width x Length) nominal	# of Banks in SDRAM BA/BG	SDRAM Package Type	Package Type	MO-207 variation
9.0 x 13.0	2 / 2	78 Ball FBGA	SDP	DW-z

Note 1 SDP is a single die per package.

Supported Speeds

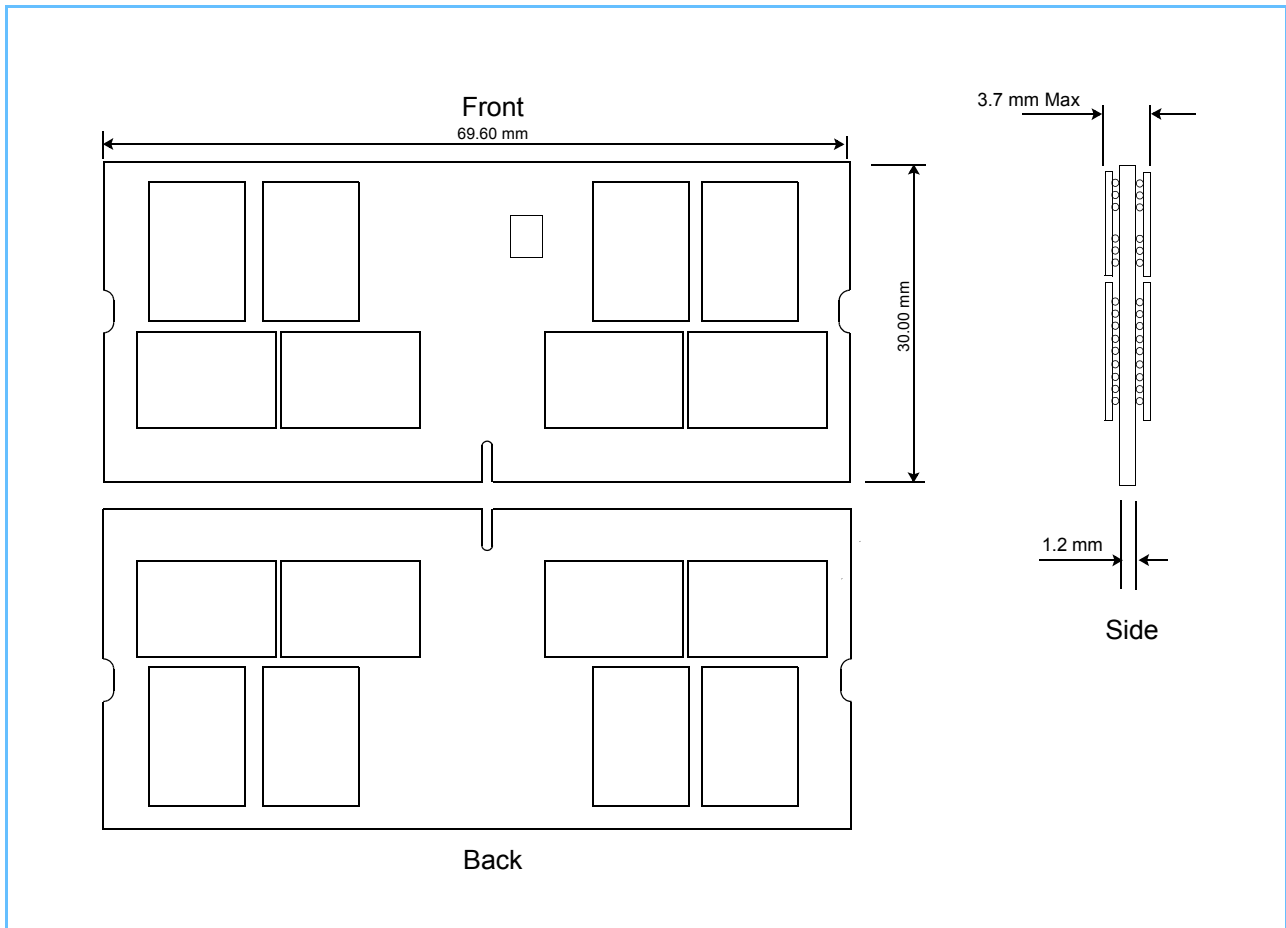
Raw Card	Speed	PC4-1600	PC4-1866	PC4-2133	PC4-2400	PC4-2666	PC4-2933	PC4-3200	Notes
B1	DDR4	N	N	N	N				1, 2

Note 1 X reflects speed grades approved previously
Note 2 N denotes new speed grades.

Design Deviations

Note 1 None.

General Layout

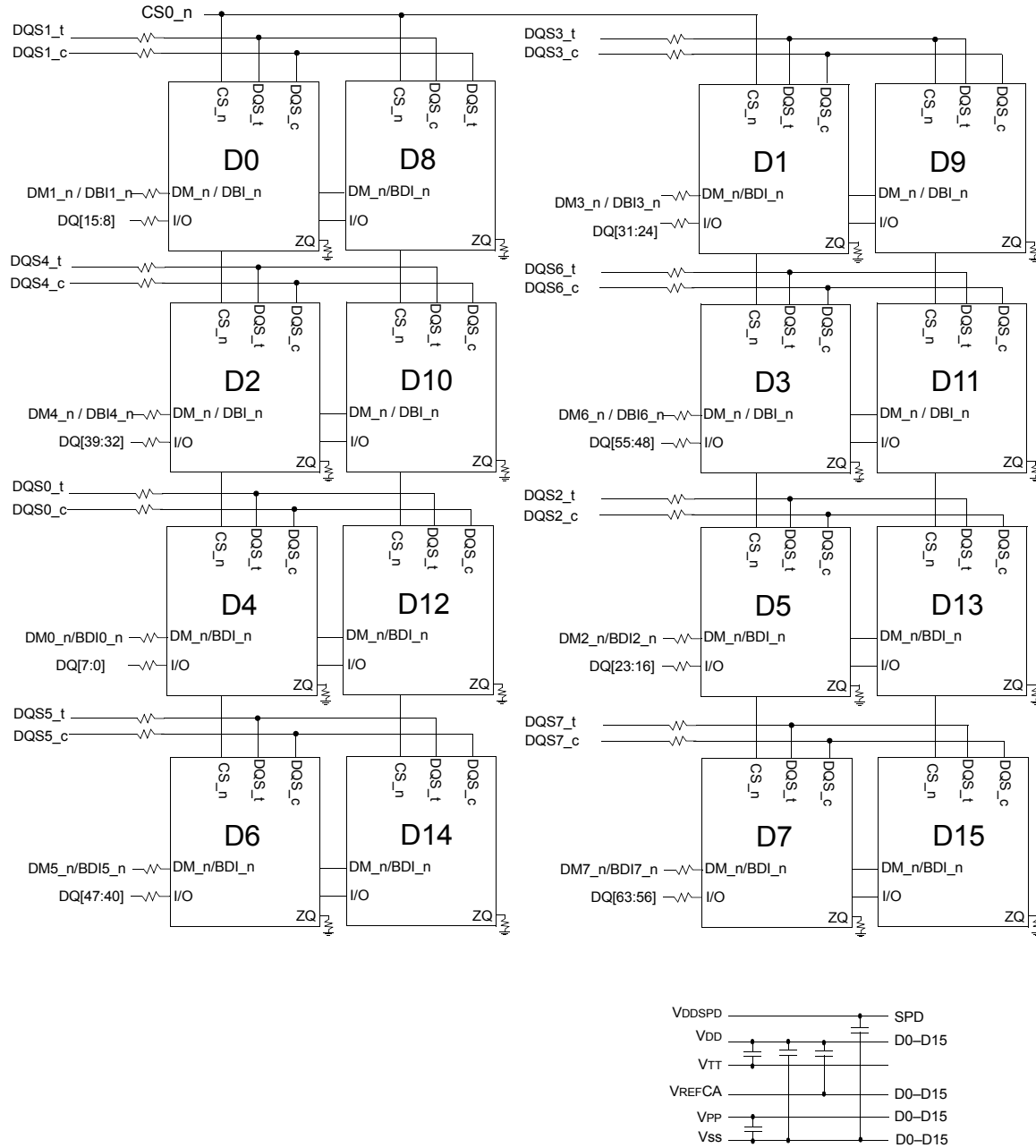


Note 1 Refer to MO-310 for more detailed information.

Note 2 Variation is AAxA (A: Module height, A: Module thickness, x: plating, A: DIMM Type).

Functional Block Diagram

x64 DIMM, populated as two physical ranks of x8 DDR4 SDRAMs (Part 1 of 2)



Note 1 DQ-to-I/O wiring is shown as recommended but may be changed.

Note 2 Unless otherwise noted, resistor values are $15\ \Omega \pm 5\%$.

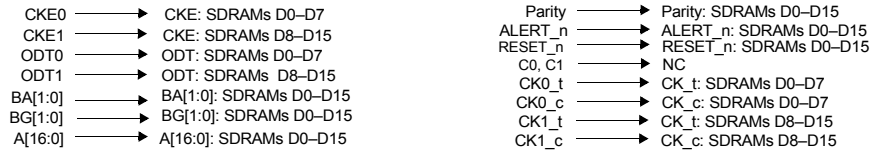
Note 3 See the Net Structure diagrams for all resistors associated with the command, address and control bus.

Note 4 ZQ resistors are $240\ \Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.

Note 5 ECC DQ, DQS, DM/BDI lines remain from contact pad to solder pad of stub resistor, but no stub resistor is mounted.

Functional Block Diagram

x64 DIMM, populated as two physical ranks of x8 DDR4 SDRAMs (Part 2 of 2)



DRAMs for ODD ranks (D8 to D15), which are placed on the back side of the module use the address mirroring for A4-A3, A6-A5, A8-A7, A13-A11, BA1-BA0 and BG1-BG0. The more details are specified in SODIMM common section.

