

Annex D - Raw Card D

DDR4 Small Outline DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
D0	PC4-SODIMM_V095_RC_D0_20131025.brd	PC4-SODIMM_V095_RC_D0_20131025-BOM.xlsx

Note 1 "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.

Module Configuration

DIMM		SDRAM		# of SDRAM die Min/Max	# of package Ranks	# of Address bits row/col	MO-310 variation
Maximum Capacity	Organization	Die Density	Organization				
2GB	256Mx72	2Gbit	256M x 8	9/9	1	14/10 ¹	AAxA
4GB	512Mx72	4Gbit	512M x 8	9/9	1	15/10 ¹	AAxA
8GB	1Gx72	8Gbit	1G x 8	9/9	1	16/10 ¹	AAxA
16GB	2Gx72	16Gbit	2G x 8	9/9	1	17/10	AAxA

Note 1 Address A16 is the highest address bit used based on it being multiplexed with RAS_n. A17 is not valid for x8 based SDRAMs.

SDRAM Configuration

Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM BA/BG	SDRAM Package Type	Package Type	MO-207 variation
10.0 x 13.0	2/2	78 Ball FBGA	SDP	DW-z

Note 1 SDP is a single die per package

Supported Speeds

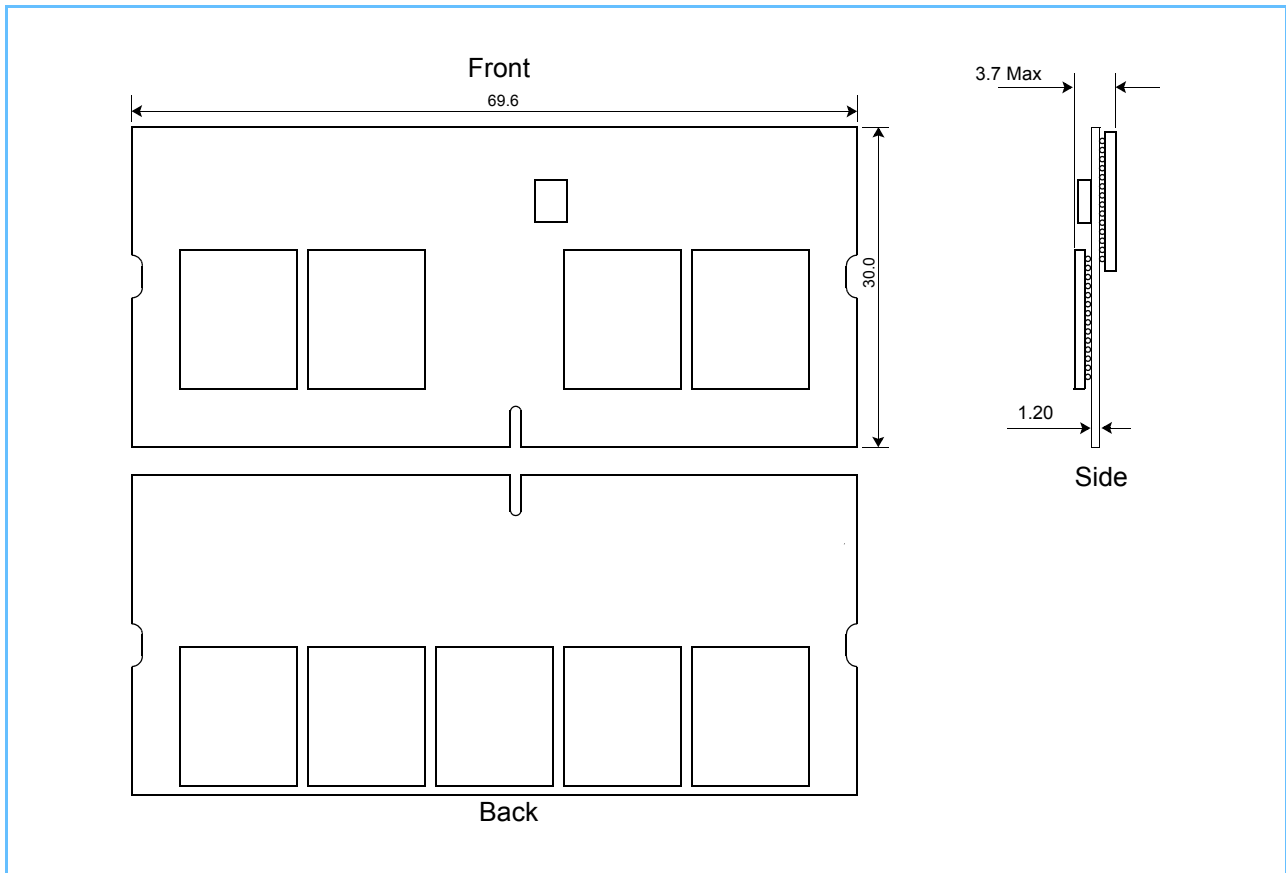
Raw Card	Speed	PC4-1333	PC4-1600	PC4-1866	PC4-2133	PC4-2400	PC4-2666	PC4-3200	Notes
D0	DDR4	X	X	X	X				1, 2
D0	DDR4L								1, 2

Note 1 X reflects speed grades approved from previous ballots.
Note 2 P denotes speed grades being proposed for this most recent ballot

Design Deviations

Note 1 None.

General Layout

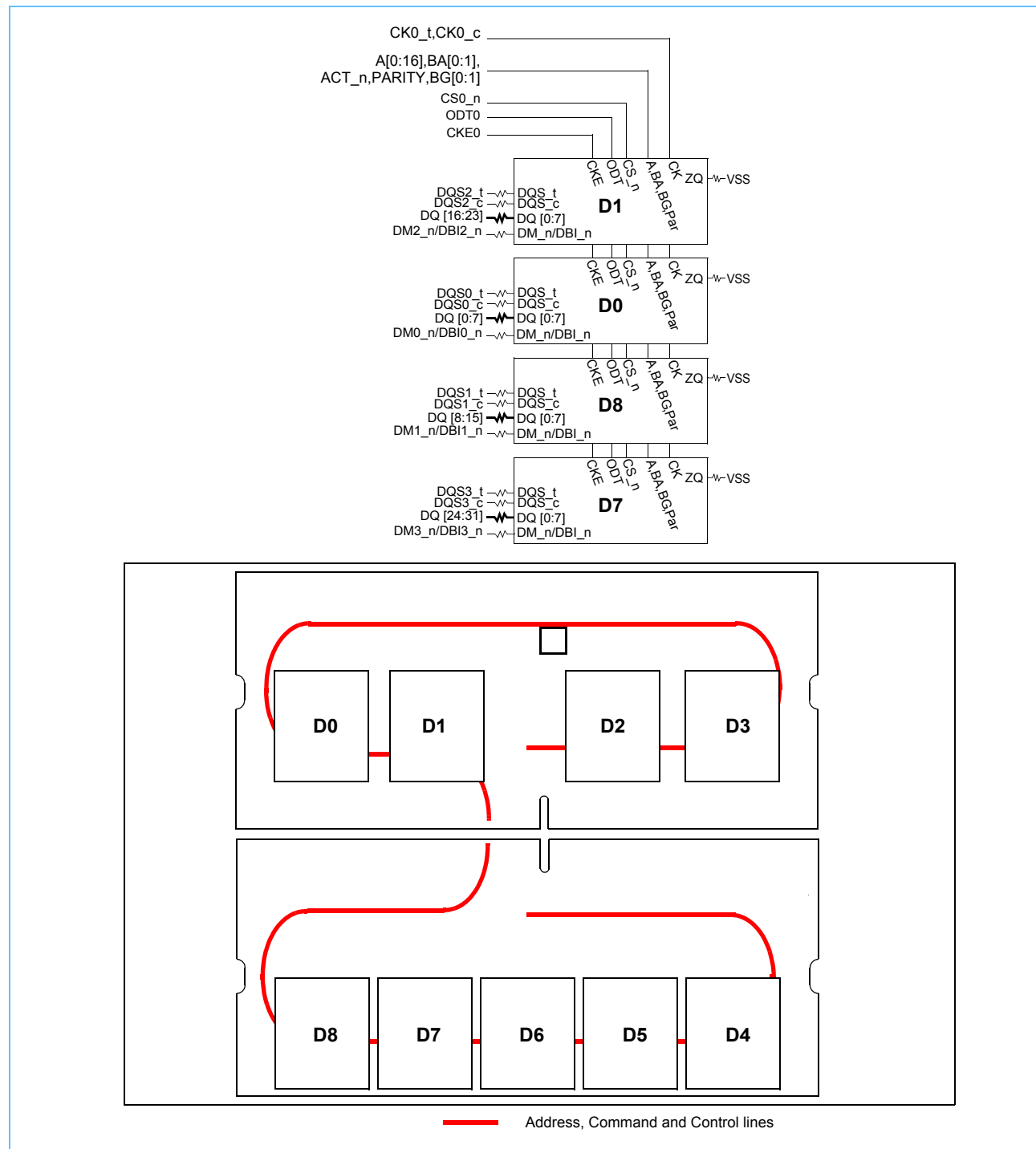


Note 1 Refer to MO-310 for more detailed information.

Note 2 Variation is AAxA (A-Module height, A-Module thickness, x-plating, A-DDR4 key).

Functional Block Diagram

x72 DIMM, populated as one package rank of x8 DDR4 SDRAMs (Part 1 of 2)

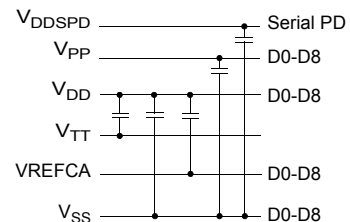
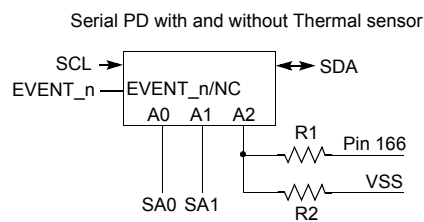
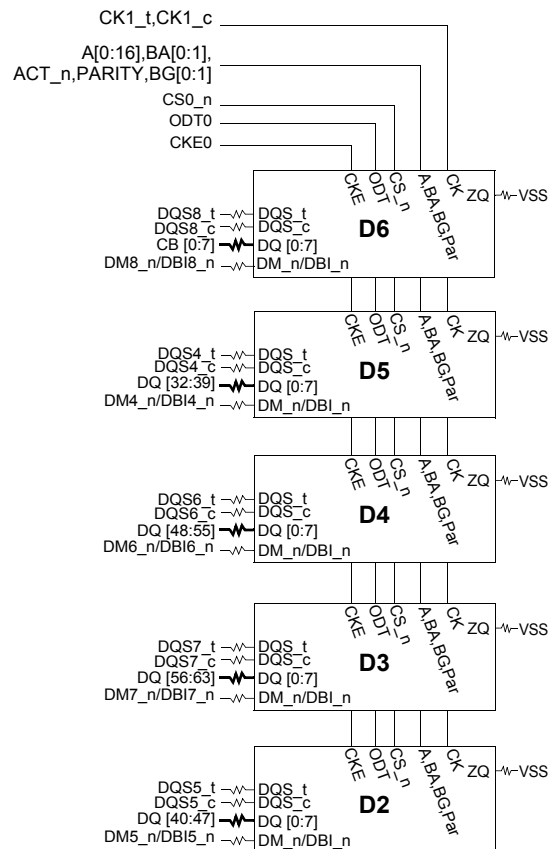


Note 1 Unless otherwise noted, resistor values are $15\Omega \pm 5\%$.

Note 2 ZQ resistors are $240\Omega \pm 1\%$. For all other resistor values, refer to the appropriate wiring diagram.

Functional Block Diagram

x72 DIMM, populated as one package rank of x8 DDR4 SDRAMs (Part 2 of 2)



Note 1 Unless otherwise noted, resistor values are $15\Omega \pm 5\%$.

Note 2 ZQ resistors are $240\Omega \pm 1\%$. For all other resistor values, refer to the appropriate wiring diagram.

Note 3 To connect the SPD A2 input to the edge connector pin 166, install R1. To tie the SPD input A2 to ground, install R2. Do not install both R1 and R2. The values for R1 and R2 are not critical. Any value less than 100 Ohms may be used.