

Annex G - Raw Card G

DDR4 SODIMM Design File

Raw Card	Applicable Design File	Applicable BOM
G0	PC4_SODIMM_V090_RC_G0_20140806.brd	PC4_SODIMM_V090_RC_G0_20140806_BOM.xlsx
G1	PC4-SODIMM_V070_RC_G1_20150805.brd	PC4-SODIMM_V070_RC_G1_20150805_BOM.xlsx

Note 1 "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.

Module Configuration

SDRAM			DIMM					
Die Density	Die Organization	Package Type	# of Package Ranks per DIMM	# of SDRAM die per DIMM	Capacity per DIMM	Organization of DIMM	# of Address bits row/col ¹	MO-310 variation
2 Gb	256M x 8	SDP	2	18	4 GB	512M x 72	14/10	AAxA
4 Gb	512M x 8	SDP	2	18	8 GB	1G x 72	15/10	AAxA
8 Gb	1G x 8	SDP	2	18	16 GB	2G x 72	16/10	AAxA
16 Gb	2G x 8	SDP	2	18	32 GB	4G x 72	17/10	AAxA

Note 1 Address A16 is the highest address bit used based on it being multiplexed with RAS_n.

SDRAM Configuration

Raw Card	Supported DRAM Outline (Width x Length) nom.	# of Banks in SDRAM BA/BG	SDRAM Package Type	Package Type	MO-207 variation
G0	11.0 x 11.5	2/2	78 Ball FBGA	SDP	DW-z
G1	9.0 x 11.5	2/2	78 Ball FBGA	SDP	DW-z

Note 1 SDP is a single die per package.

Supported Speeds

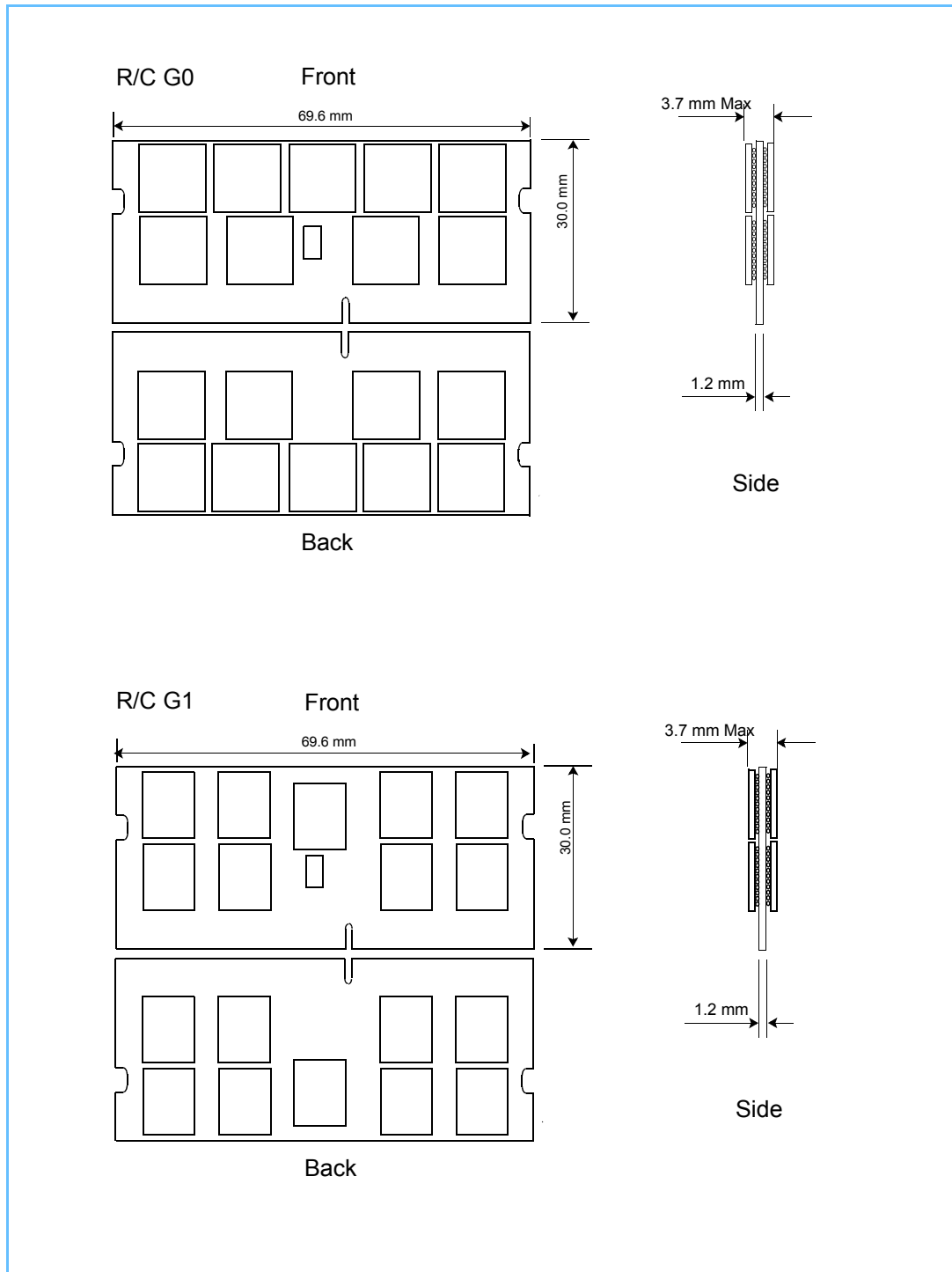
Raw Card	Speed	PC4-1333	PC4-1600	PC4-1866	PC4-2133	PC4-2400	PC4-2666	PC4-3200	Notes
G0	DDR4	X	X	X	X				1, 2
G1	DDR4	N	N	N	N	N			1, 2

Note 1 X reflects speed grades approved from previous ballots.
Note 2 N denotes NEW speed grades.

Design Deviations

Note 1 None

General Layout

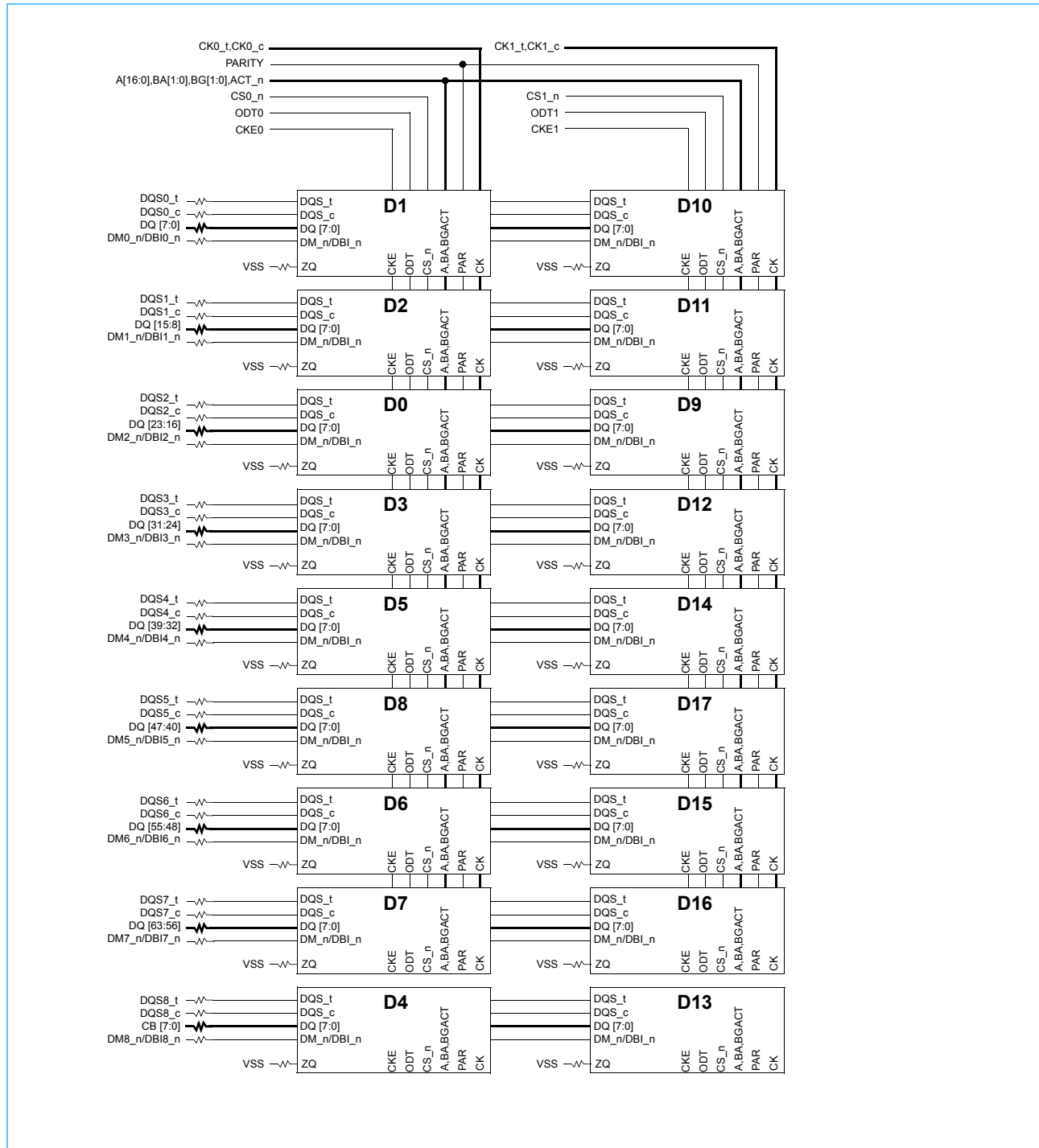


Note 1 Refer to MO-310 for more detailed information.

Note 2 Variation is AAxA (A: Module height, A: Module thickness, x: plating, A: DIMM Type).

Functional Block Diagram

x72 DIMM, populated as two package ranks of x8 DDR4 SDRAMs (Part 1 of 2)



Note 1 DQ-to-I/O wiring is shown as recommended but may be changed.

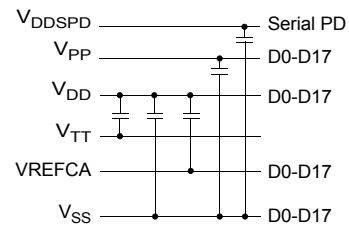
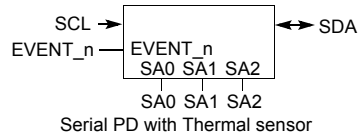
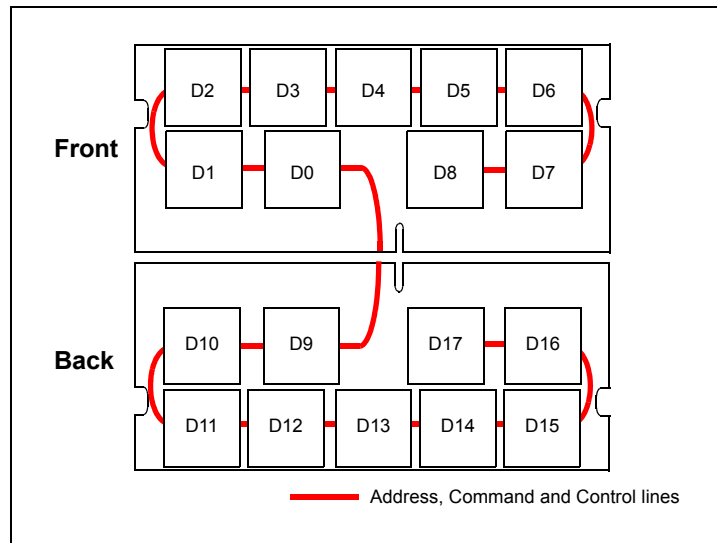
Note 2 Unless otherwise noted, resistor values are $15\ \Omega \pm 5\%$.

Note 3 See the Net Structure diagrams for all resistors associated with the command, address and control bus.

Note 4 ZQ resistors are $240\ \Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.

Functional Block Diagram

x72 DIMM, populated as two package ranks of x8 DDR4 SDRAMs (Part 2 of 2)



Loading and Test Points

Loading

Signal Names	Input to Device	Loads
CK0_t, CK0_c	SDRAMs	9
CK1_t, CK1_c	SDRAMs	9
RESET_n	SDRAMs	18
CKE0, CKE1, ODT0, ODT1	SDRAMs	9
Ax, BAx, BGx, PARITY, ACT_n	SDRAMs	18
CS0_n, CS1_n	SDRAMs	9
DQ, CB, DQS_t, DQS_c	SDRAMs	2
DMx_n/DBIx_n	SDRAMs	2
SCL, SDA, SA0, SA1, SA2, EVENT_n	SPD	1
ALERT_n	SDRAMs	18

Test Point Locations

Signal Group	Signal	Signal locations
Address/Command/ Control/Parity	All	Termination resistors on the end of the module
DQ, CB, DMx_n, DBIx_n	All	15 Ω resistors
DQSx_t, DQSx_c	All	15 Ω resistors
Clock	All	Termination resistors
Note 1 Refer to the registration package for additional test point information.		