

Annex A - Raw Card A

DDR4 Unbuffered DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
A0	PC4-UDIMM_V080_RC_A0_20140425.brd	PC4-UDIMM_V080_RC_A0_20140425_BOM.xlsx
A1	PC4-UDIMM_V191_RC_A1_D1_20150424.brd	PC4-UDIMM_V191_RC_A1_20150424_BOM.xlsx

Note 1 "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.

Module Configuration

DIMM		SDRAM		# of SDRAM die Min/Max	# of Logical Ranks per DIMM Min/Max	# of Package Ranks per DIMM Min/Max	# of Address bits row/col	MO-309 variation
Maximum Capacity	Organization	Die Density	Organization					
2 GB	256 Mb x64	2 Gb	256 Mb x 8	8 / 8	1	1	14 / 10 ¹	AAxA
4 GB	512 Mb x64	4 Gb	512 Mb x 8	8 / 8	1	1	15 / 10 ¹	AAxA
8 GB	1 Gb x64	8 Gb	1 Gb x 8	8 / 8	1	1	16 / 10 ¹	AAxA
16 GB	2 Gb x64	16 Gb	2 Gb x 8	8 / 8	1	1	17 / 10	AAxA

Note 1 Address A16 is the highest address bit used based on it being multiplexed with RAS_n

SDRAM Configuration

Supported DRAM Outline (Width x Length) nom.	# of Banks in SDRAM BA/BG	SDRAM Package Type	Package Type	MO-207 variation
11.0 x 13.0 (mm)	2 / 2	78 Ball FBGA	SDP	DW-z

Note 1 SDP is a Single Die per Package.

Supported Speeds

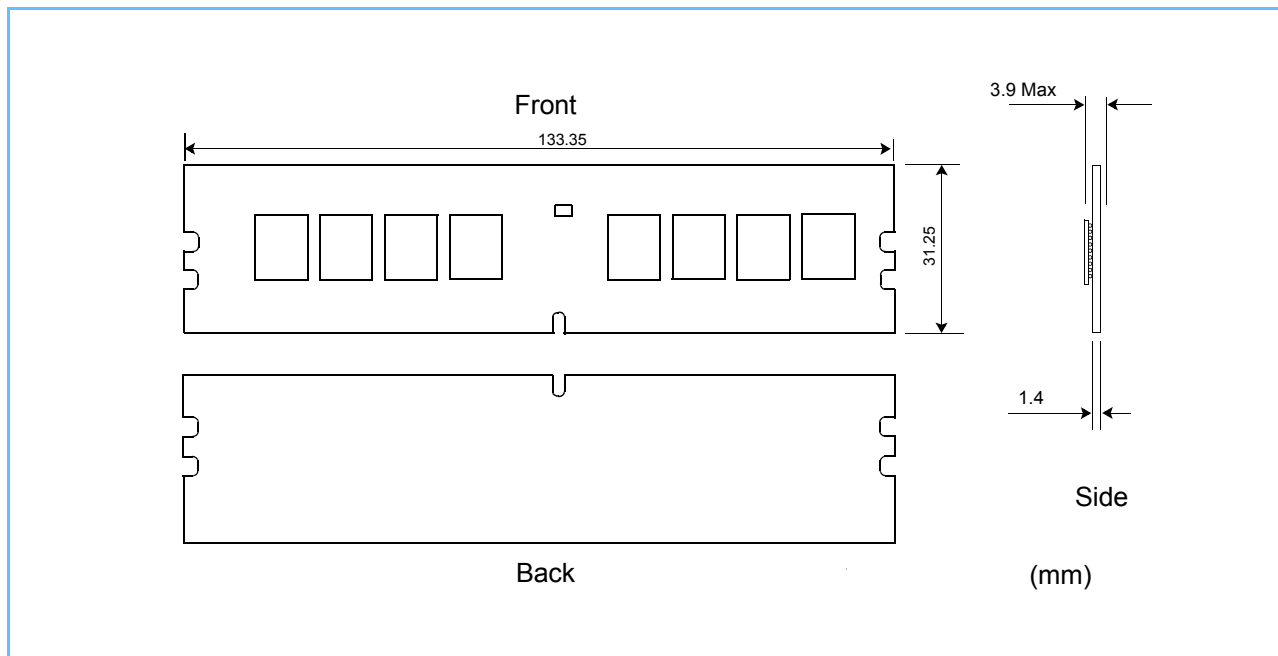
Raw Card	Speed	PC4-1333	PC4-1600	PC4-1866	PC4-2133	PC4-2400	PC4-2666	PC4-3200	Notes
A0	DDR4	X	X	X	X				1, 2
A1	DDR4	N	N	N	N	N			1, 2

Note 1 X reflects speed grades approved from previous ballots.
Note 2 N denotes speed grades being proposed for this most recent ballot

Design Deviations

Note 1 None.

General Layout



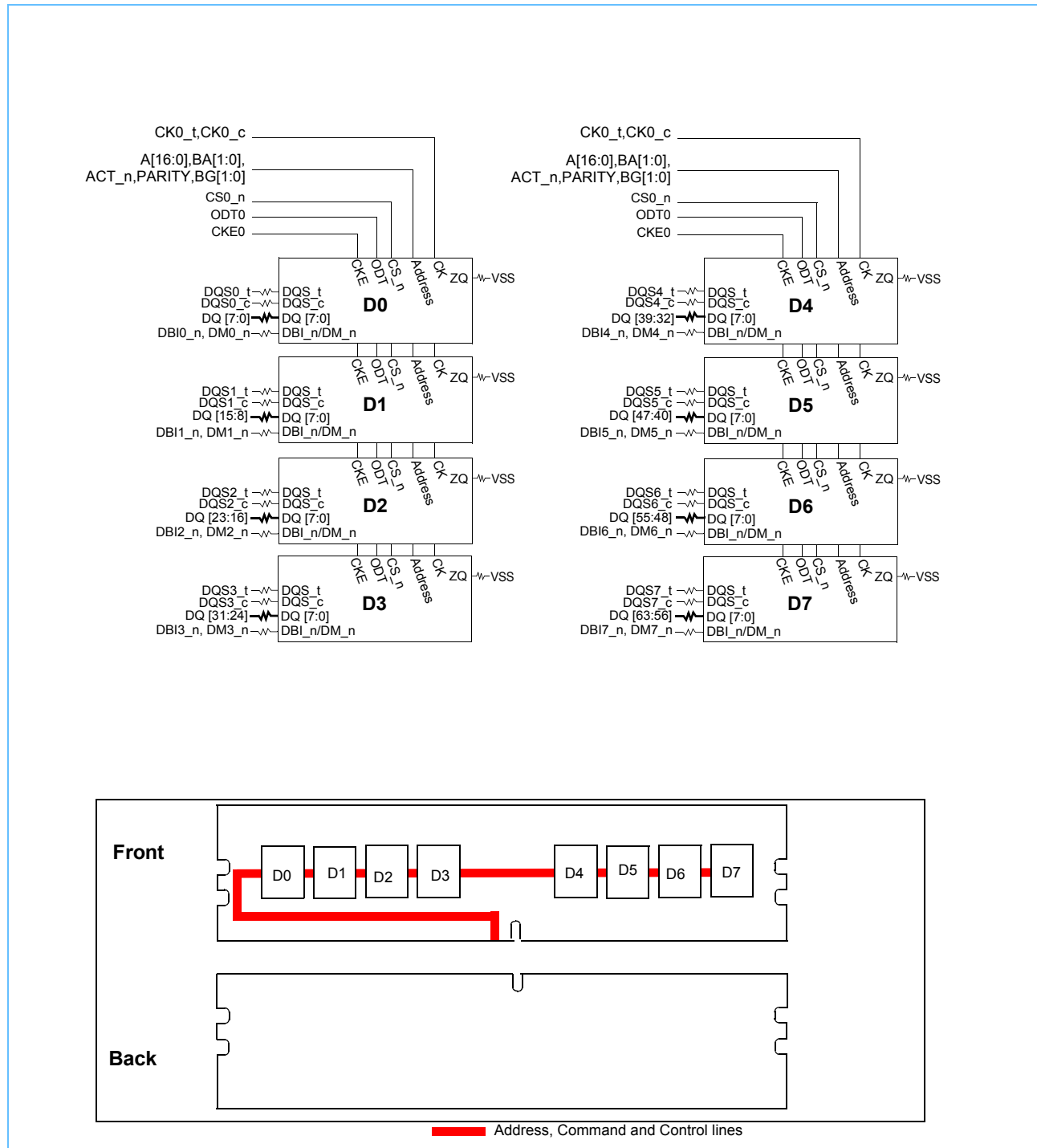
Note 1 Refer to MO-309 for more detailed information.

Note 2 Variation is AAxA (A Module height, A Module thickness, x plating, A Key Position).

Note 3 Module thickness may vary with DRAM thickness and passive components.

Functional Block Diagram

x64 DIMM, populated as one package rank of x8 DDR4 SDRAMs (Part 1 of 2)



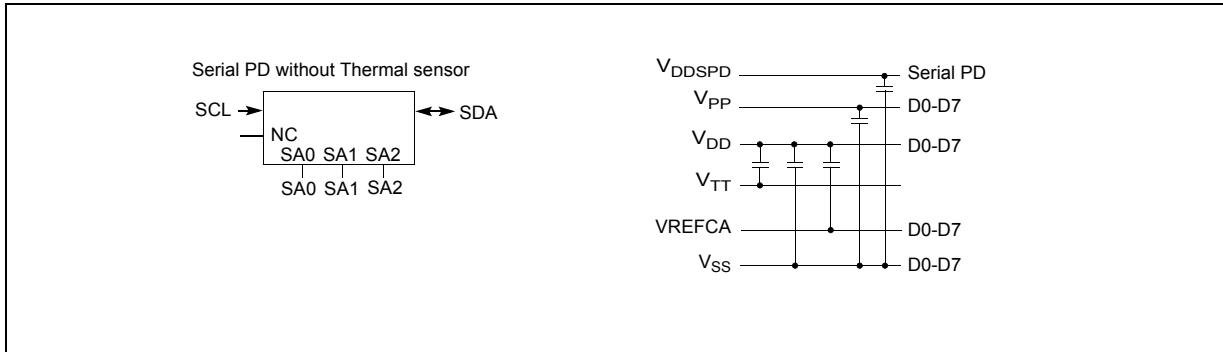
Note 1 CK1_t, CK1_c terminated with $75\ \Omega \pm 5\%$ resistor.

Note 2 Unless otherwise noted resistors are $15\ \Omega \pm 5\%$.

Note 3 ZQ resistors are $240\ \Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.

Note 4 Event_n isn't used for SPD without TS. Option Resistor for it should be unplaced.

x64 DIMM, populated as one package rank of x8 DDR4 SDRAMs (Part 2 of 2)



Loading and Test Points

Loading

Signal Names	Input to Device	Loads
CK0_t, CK0_c	SDRAMs	8
CK1_t, CK1_c	Termination Resistor Only	1 ¹
RESET_n	SDRAMs	8
CKE0, ODT0	SDRAMs	8
Ax, BAx, BGx, RAS_n, CAS_n, WE_n, PARITY, ACT_n	SDRAMs	8
CS0_n	SDRAMs	8
DQ, DQS_t, DQS_c	SDRAM	1
DMx_n/DBIx_n	SDRAM	1
SCL, SDA, SA[2:0], EVENT_n	SPD	1
ALERT_n	SDRAM	8
Note 1 Connected but not used.		

Test Point Locations

Signal Group	Signal	Signal locations
Address/Command/ Control/PARITY	ALL	Termination resistors on the end of the module
DQ, DM_n, DBI_n	ALL	15 Ω resistors
DQS_t, DQS_c	ALL	15 Ω resistors
Clock	ALL	Termination resistors.
Note 1 Refer to the registration package for additional test point information.		