

Annex B - Raw Card B

DDR4 Unbuffered DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
B0	PC4-UDIMM_V070_RC_B0_20130802.brd	PC4-UDIMM_V070_RC_B0_20130802-Bom.txt
B1	PC4-UDIMM_V200_RC_B1_20140925.brd	PC4-UDIMM_V200_RC_B1_20141021-Bom.docx

Note 1 "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.

Module Configuration

DIMM		SDRAM		# of SDRAM die	# of Package Ranks	# of Address bits row/col	MO-309 variation
Maximum Capacity	Organization	Die Density	Organization				
4 GB	512M x64	2 Gb	256M x 8	16	2	14/10 ¹	AAxA
8 GB	1G x64	4 Gb	512M x 8	16	2	15/10 ¹	AAxA
16 GB	2G x64	8 Gb	1G x 8	16	2	16/10 ¹	AAxA
32 GB	4G x68	16 Gb	2G x 8	16	2	17/10	AAxA

Note 1 Address A16 is the highest address bit used based on it being multiplexed with RAS_n.

SDRAM Configuration

Raw Card	Supported DRAM Outline (Width x Length) nom. (mm)	# of Banks in SDRAM BA/BG	SDRAM Package Type	Package Type	MO-207 variation
B0	10.5 x 13.0	2/2	78 Ball FBGA	SDP	DW-z
B1	9.0 x 13.0	2/2	78 Ball FBGA	SDP	DW-z

Note 1 SDP is a single die per package

Supported Speeds

Raw Card	PC4-1333	PC4-1600	PC4-1866	PC4-2133	PC4-2400	PC4-2666	PC4-3200	Notes
B0	X	X	X	X				1, 2
B1	X	X	X	X	X	N		1, 2

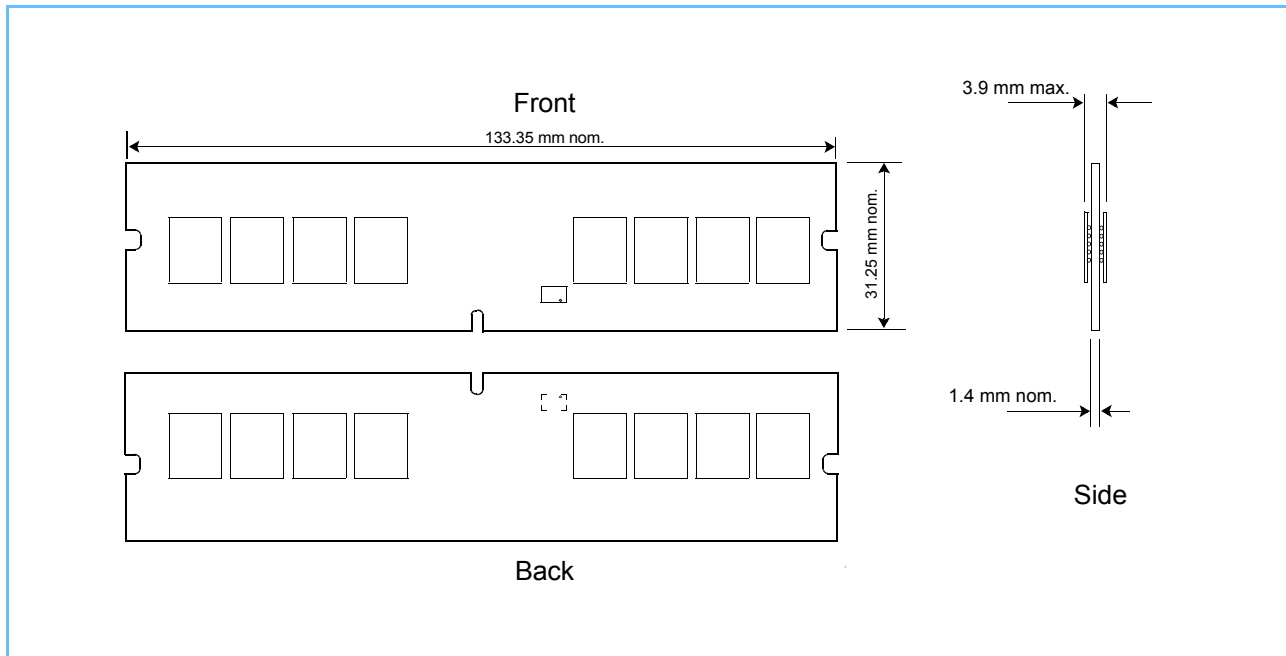
Note 1 X reflects speed grades approved from previous ballots.

Note 2 N denotes speed grades being proposed for this most recent ballot

Design Deviations

Note 1 R/C B0 - Clock mismatch at last SDRAM is 0.5 mm. Design Specification requirement is 0.2 mm.
Note 2 R/C B1 - None.

General Layout

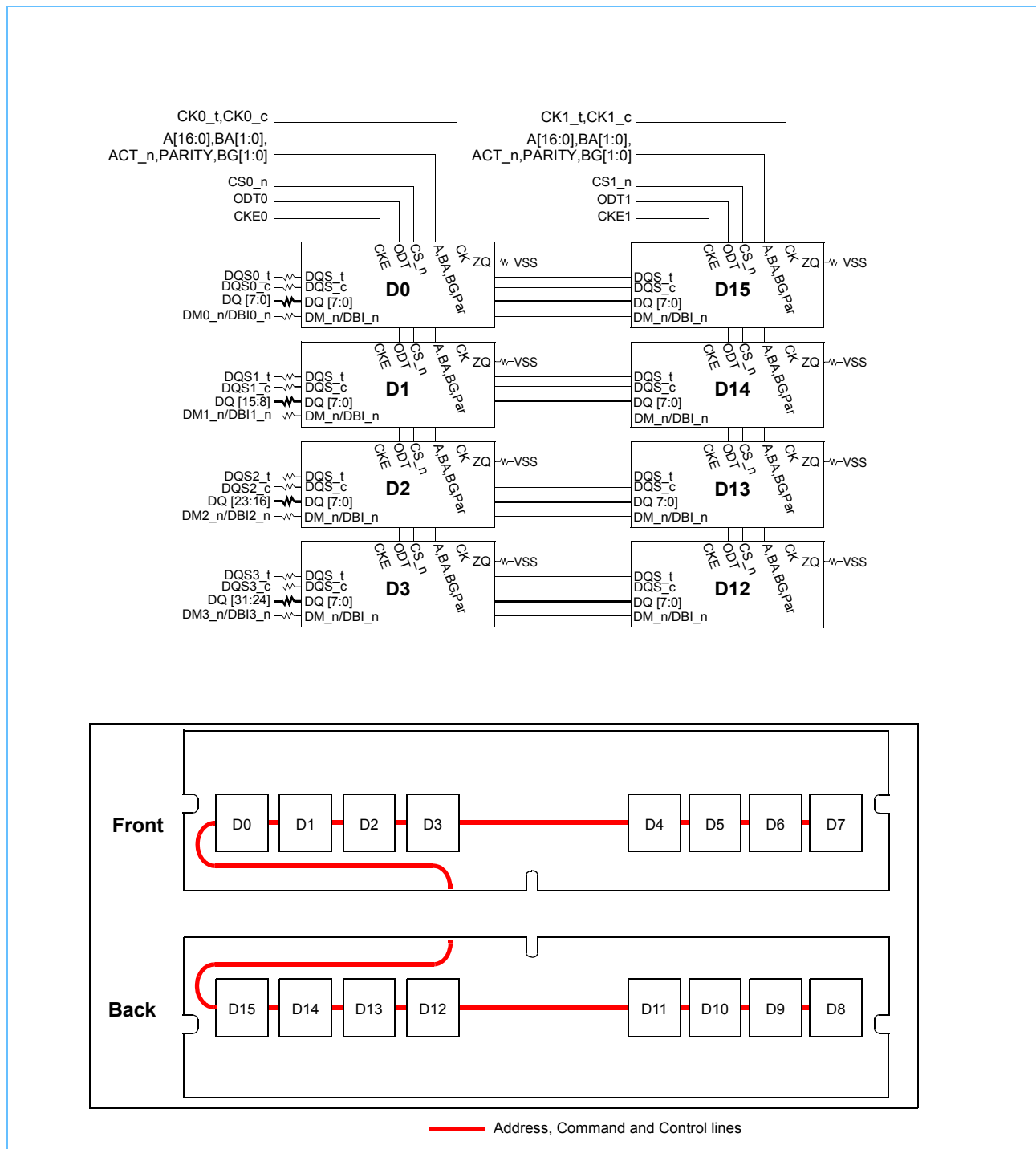


Note 1 Refer to MO-309 for more detailed information.

Note 2 Variation is AAxA (A Module height, A Module thickness, x plating, A Key Position).

Functional Block Diagram

x64 DIMM, populated as two package ranks of x8 DDR4 SDRAMs (Part 1 of 2)



Note 1 Unless otherwise noted, resistor values are $15 \pm 5\%$.

Note 2 ZQ resistors are $240 \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.

Functional Block Diagram

x64 DIMM, populated as two package ranks of x8 DDR4 SDRAMs (Part 2 of 2)

