

Annex C - Raw Card C

DDR4 Unbuffered DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
C0	PC4-UDIMM_V100_RC_C0_20150821.brd	PC4-UDIMM_V100_RC_C0_20151116-BOM.docx
Note 1 "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.		

Module Configuration

DIMM		SDRAM		# of SDRAM die	# of Package Ranks	# of Address bits row/col	MO-309 variation
Maximum Capacity	Organization	Die Density	Organization				
1 GB	128M x64	2 Gb	128M x 16	4	1	14/10 ¹	AAxA
2 GB	256M x64	4 Gb	256M x 16	4	1	15/10 ¹	AAxA
4 GB	512M x64	8 Gb	512M x 16	4	1	16/10 ¹	AAxA
8 GB	1G x64	16 Gb	1G x 16	4	1	17/10	AAxA
Note 1 Address A16 is the highest address bit used based on it being multiplexed with RAS_n.							

SDRAM Configuration

Raw Card	Supported DRAM Outline (Width x Length) nom. (mm)	# of Banks in SDRAM BA/BG	SDRAM Package Type	Package Type	MO-207 variation
C0	10.5 x 14.0	2 / 1	96 Ball FBGA	SDP	DU-z
Note 1 SDP is a single die per package					

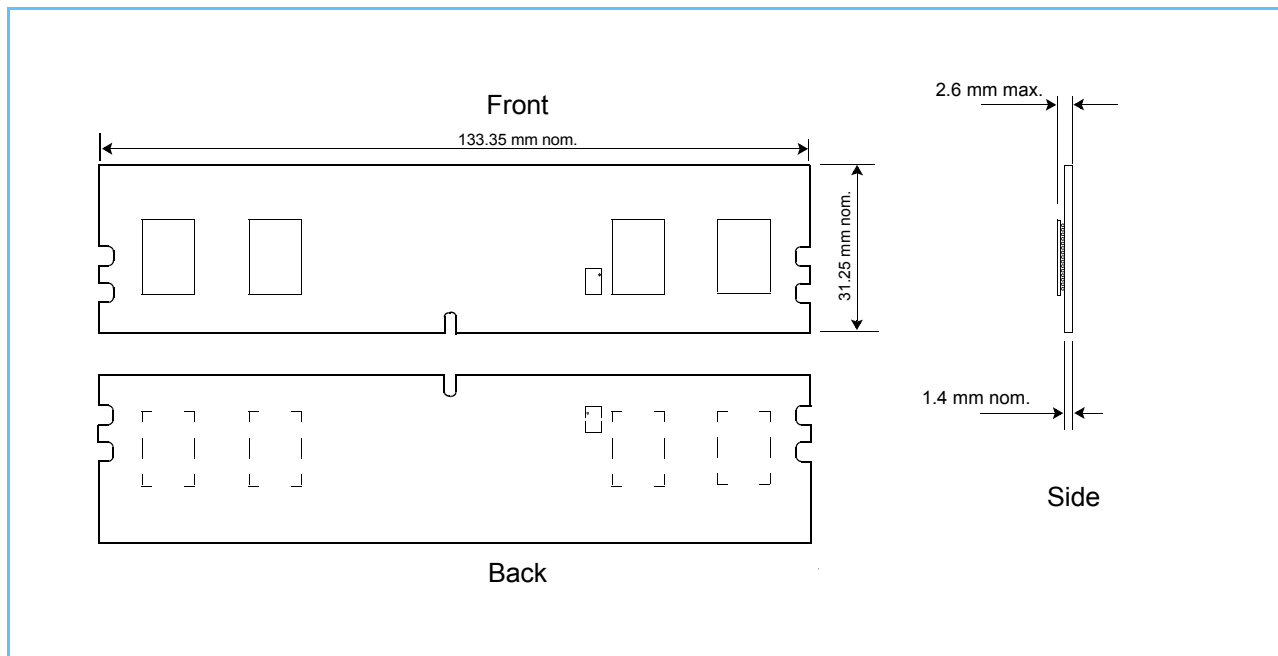
Supported Speeds

Raw Card	PC4-1333	PC4-1600	PC4-1866	PC4-2133	PC4-2400	PC4-2666	PC4-2933	PC4-3200	Notes
C0	N	N	N	N	N				1, 2
Note 1 X reflects speed grades approved from previous ballots. Note 2 N denotes "NEW" speed grades.									

Design Deviations

Note 1 Lead-in is 45 Ohms, not 40 Ohms as recommended in Common Design Specification.

General Layout

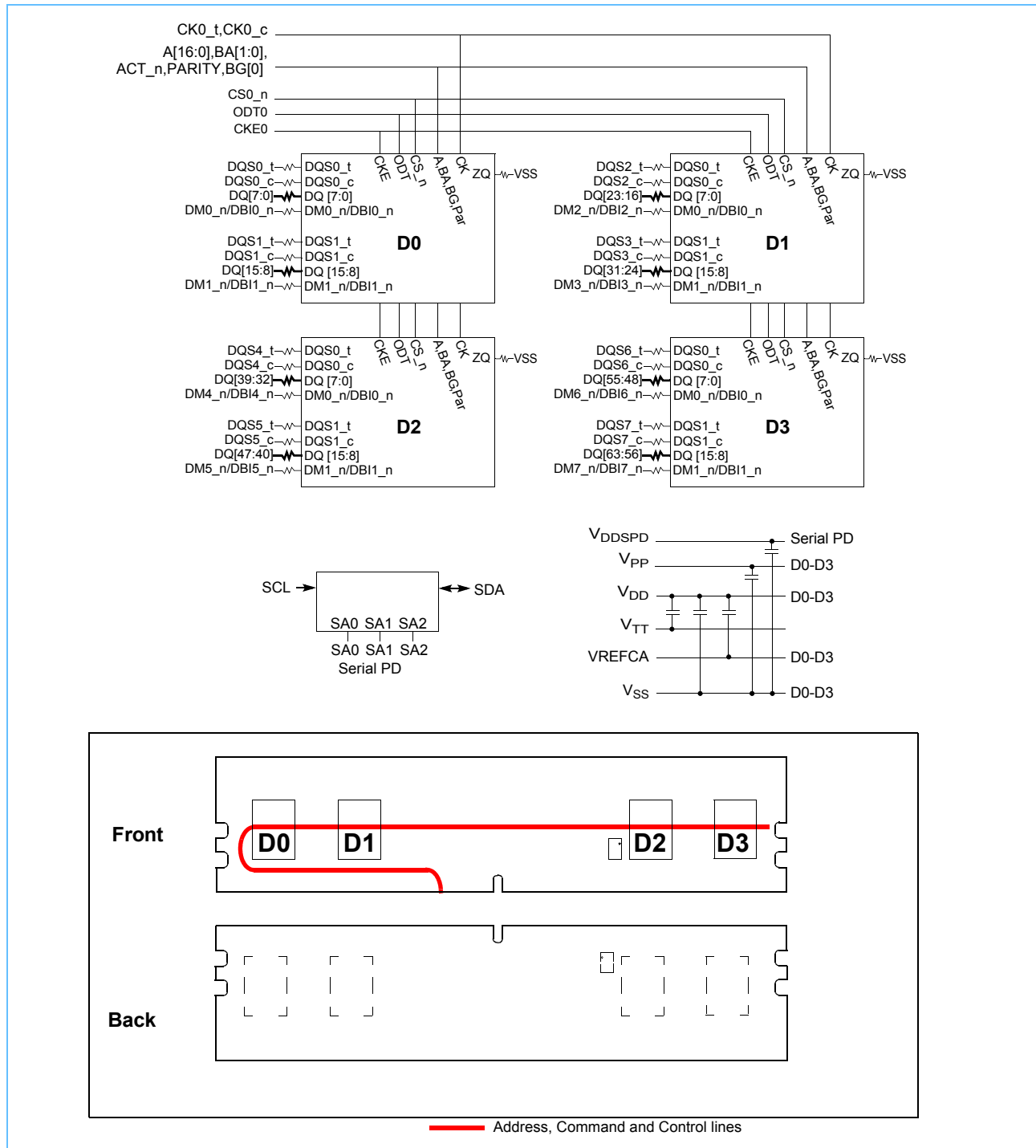


Note 1 Refer to MO-309 for more detailed information.

Note 2 Variation is AAxA (A Module height, A Module thickness, x plating, A Key Position).

Functional Block Diagram

x64 DIMM, populated as one package rank of x16 DDR4 SDRAMs (Part 1 of 2)



Note 1 Unless otherwise noted, resistor values are $15\ \Omega \pm 5\%$.

Note 2 ZQ resistors are $240\ \Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.

Note 3 CK1_t, CK1_c terminated with $75\ \Omega \pm 5\%$ resistor.

Loading and Test Points

Loading

Signal Names	Connecting to Device	Loads
CK0_t, CK0_c	SDRAMs	4
CK1_t, CK1_c ²	Termination	1
RESET_n	SDRAMs	4
CKE0, ODT0	SDRAMs	4
Ax, BAx, BG0, RAS_n, CAS_n, WE_n, ACT_n, PARITY	SDRAMs	4
CS0_n	SDRAMs	4
DQx, DQSx_t, DQSx_c	SDRAMs	1
DMx_n/DBIx_n	SDRAMs	1
SCL, SDA, SA[2:0]	SPD	1
ALERT_n	SDRAMs	4
Note 1 CS1_n, ODT1 and CKE1 are not connected on this module. Note 2 CK1_t and CK1_c are terminated but not used.		

Test Point Locations

Signal Group	Signal	Signal locations
Address / Command/ Control / PARITY	All	Termination resistors on the end of the module
DQ, DM_n, DBI_n	All	15 Ω resistors
DQS_t, DQS_c	All	15 Ω resistors
Clock	All	Termination resistors
Note 1 Refer to the registration package for additional test point information.		