

Annex E - Raw Card E

DDR4 Unbuffered DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
E0	PC4-UDIMM_V091_RC_E0_20141024.brd	PC4-UDIMM_V091_RC_E0_20141024_BOM.htm
E1	PC4-UDIMM_V050_RC_E1_20141126.brd	PC4-UDIMM_V050_RC_E1_20141126_BOM.xlsx

Note 1 "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.

Module Configuration

DIMM		SDRAM		# of SDRAM die Min/Max	# of Package Ranks per DIMM	# of Address bits row/col	MO-309 variation
Maximum Capacity	Organization	Die Density	Organization				
4 GB	512M x72	2 Gb	256M x 8	18/18	2	14/10 ¹	AAxA
8 GB	1G x72	4 Gb	512M x 8	18/18	2	15/10 ¹	AAxA
16 GB	2G x72	8 Gb	1G x 8	18/18	2	16/10 ¹	AAxA
32 GB	4G x72	16 Gb	2G x 8	18/18	2	17/10	AAxA

Note 1 Address A16 is the highest address bit used based on it being multiplexed with RAS_n.

SDRAM Configuration

Supported DRAM Outline (Width x Length) nom. (mm)	# of Banks in SDRAM BA/BG	SDRAM Package Type	Package Type	MO-207 variation
11.0 x 13.0	2/2	78 Ball FBGA	SDP	DW-z

Note 1 Note: SDP is a Single Die Package.

Supported Speeds

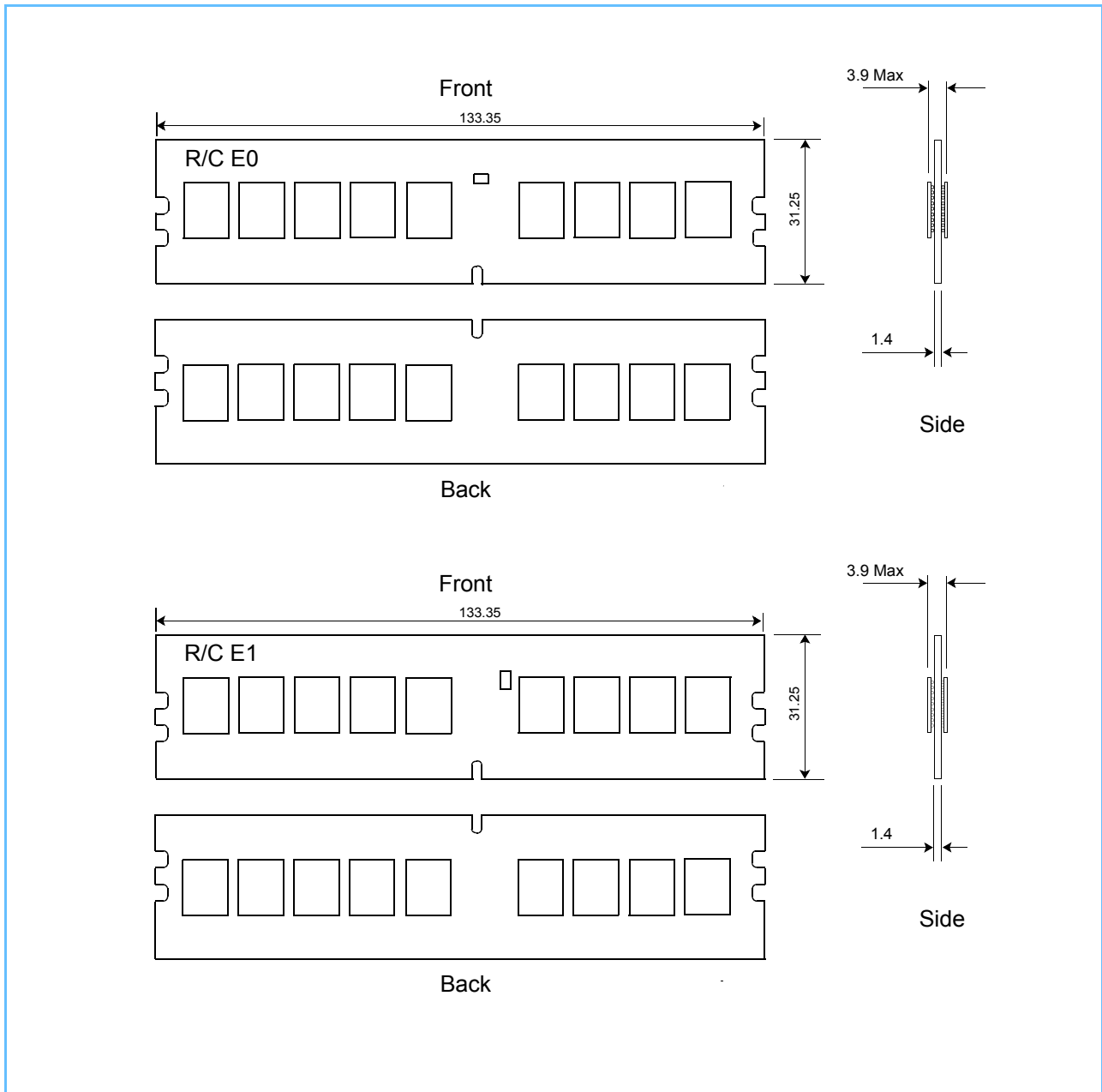
Raw Card	Speed	PC4-1333	PC4-1600	PC4-1866	PC4-2133	PC4-2400	PC4-2666	PC4-3200	Notes
E0	DDR4	X	X	X	X				1, 2
E1	DDR4	P	P	P	P	P			

Note 1 X reflects speed grades approved from previous ballots.
Note 2 P denotes speed grades being proposed for this most recent ballot.

Design Deviations

Note 1 None.

General Layout



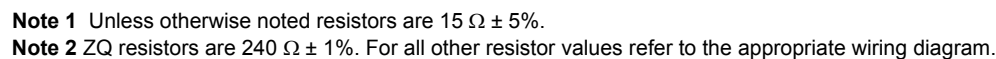
Note 1 Refer to MO-309 for more detailed information.

Note 2 Variation is AAxA (A Module height, A Module thickness, x plating, A Key Position).

Note 3 Module thickness may vary with DRAM thickness and passive components.

Note 4 All distances are given in mm.

x72 DIMM, populated as one package ranks of x8 DDR4 SDRAMs (Part 1 of 1)



Loading and Test Points

Loading

Signal Names	Input to Device	Loads
CK0_t, CK0_c	SDRAMs	9
CK1_t, CK1_c	SDRAMs	9
RESET_n	SDRAMs	18
CKE0, ODT0, CKE1, ODT1	SDRAMs	9
Ax, BAx, BGx, RAS_n, CAS_n, WE_n, PARITY, ACT_n	SDRAMs	18
CS0_n, CS1_n	SDRAMs	9
DQ, CB, DQS_t, DQS_c	SDRAM	2
DMx_n/DBIx_n	SDRAM	2
SCL, SDA, SA[2:0], EVENT_n	SPD	1
ALERT_n	SDRAM	18

Test Point Locations

Signal Group	Signal	Signal locations
Address/Command/ Control/Parity	ALL	Termination resistors on the end of the module.
DQ, CB, DM_n, DBI_n	ALL	15 Ω resistors
DQS_t, DQS_c	ALL	15 Ω resistors
Clock	ALL	Termination resistors on the end of the module.

Note 1 Refer to the registration package for additional test point information.