

4.20.27 - 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/
PC4-2666/PC4-3200 DDR4 SDRAM Load Reduced DIMM Design Specification

DDR4 SDRAM Load Reduced DIMM Design Specification

Revision 1.00

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Table of Contents

1	Product Description	5
2	Environmental Requirements.....	6
3	Connector Pinout and Signal Description.....	7
4	Power Details	12
4.1	DIMM Voltage Requirements	12
4.1.1	VTT Range	12
4.1.2	Load Line	12
4.2	Rules for Power-Up Sequence.....	13
4.3	12 V Power.....	13
5	Component Details	14
5.1	Component Types and Placement	16
5.2	Decoupling Guidelines	16
6	DIMM Design Details	17
6.1	Signal Groups	17
6.2	General Net Structure Routing Rules	17
6.2.1	Clock, Control, and Address/Command Groups	19
6.2.2	PreRegister ADD/CMD and CTRL	19
6.2.3	PreRegister CK	19
6.2.4	PostRegister ADD/CMD	20
6.2.5	PostRegister CTRL Group	21
6.2.6	PreDataBuffer DQ Group	21
6.2.7	PostDataBuffer DQ.....	23
6.3	Plane Referencing.....	23
6.4	Address Mirroring.....	23
6.5	DQ Mapping to Support CRC.....	24
6.6	DIMM Routing Space Constraints	26
6.7	DIMM Physical Requirements.....	28
6.7.1	Via Size	28
6.7.2	Component Pad Sizes and Geometry.....	28
6.7.3	DRAM Package Size.....	28
6.7.4	Clock Termination	28
6.7.5	DQ Resistor.....	28
6.8	LRDIMM Configuration	29
6.8.1	Control Wiring.....	29
6.8.2	AVDD Filter Circuit	30
6.8.3	ALERT_n Circuit Wiring	30
6.8.4	ZQ Calibration Wiring	30
6.8.5	TEN Pin Wiring.....	31
6.9	SPD-TSE Signal Wiring, Selection, and Placement.....	31
7	Serial Presence Detect - Thermal Sensor.....	32
8	Product Label.....	34
8.1	DDR4 DIMM Label Format for DRAM-only module types.....	34
8.2	DDR4 DIMM Label Format for Hybrid module types.....	38
9	JEDEC Process.....	41

List of Tables

Table 1 — DDR4 Product Family Attributes	5
Table 2 — Environmental Parameters	6
Table 3 — Pin Definition	7
Table 4 — Input/Output Functional Description	8
Table 5 — DDR4 288 Pin LRDIMM Pin Wiring Assignments	10
Table 6 — DDR4 LRDIMM DC Operating Voltage ¹ , 2, 3 - 1.2 V operation	12
Table 7 — DDR4 x4 SDRAM DIMM Pad Array	15
Table 8 — LRDIMM Decoupling Capacitor Guidelines.....	16
Table 9 — Simulation Conditions	18
Table 10 — PreRegister ADD/CMD and CTRL Definition Example	19
Table 11 — PreRegister CK Length Example	20
Table 12 — PostRegister ADD/CMD Definition Example	21
Table 13 — PreDataBuffer DQ Example	22
Table 14 — Plane Referencing	23
Table 15 — DIMM Wiring Definition for Address Mirroring	23
Table 16 — SPD DQ Nibble Map for CRC	24
Table 17 — Nibble/Byte DQ Map Patterns for CRC	25
Table 18 — Example of DQ Mapping for CRC.....	26
Table 19 — Routing Space Constraints	27
Table 20 — SPD Address Map.....	32
Table 21 — Block 0: Base Configuration and DRAM Parameters.....	32

List of Figures

Figure 1 — Graphical View of Power Sequence	13
Figure 2 — DIMM Ball Patterns for DDR4 SDRAM Components	14
Figure 3 — LRDIMM Topologies	17
Figure 4 — PreRegister ADD/CMD and CTRL Diagram Example	19
Figure 5 — PreRegister CK Diagram Example	20
Figure 6 — PostRegister ADD/CMD Diagram Example	21
Figure 7 — Example DQ Net Structure	22
Figure 8 — Example of DQ Wiring with Mapping for CRC	26
Figure 9 — DDR4 QRx4 (DDP) Control Wiring	29
Figure 10 — DDR4 2R/4R/8R/16R (planar/3DS) Control Wiring	29
Figure 11 — AVDD Filter Circuit Wiring	30
Figure 12 — Example Wiring of the ALERT_n Function	30
Figure 13 — Block Diagram: SPD-TSE and DDR4RCD01	31

1 Product Description

This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Load Reduced, Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR4 SDRAM LRDIMMs). These DDR4 Load Reduced DIMMs (LRDIMMs) are intended for use as main memory when installed in PCs.

Reference design examples are included that provide an initial basis for DDR4 LRDIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC4-1600, PC4-1866, PC4-2133, PC4-2400, PC4-2666, and PC4-3200 support. All DDR4 LRDIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

An additional lower voltage of TBD is defined. PC4L is used to reference DIMMs capable of operation at this voltage level. The annex for each raw card will have specific entries to indicate DIMM operation at PC4 and PC4L voltage levels.

This specification follows the JEDEC standard DDR4 component specification (refer to JEDEC standard JESD79-4, at www.jedec.org).

Table 1 — DDR4 Product Family Attributes

DIMM Organization	x64, x72 ECC	Notes
DIMM Dimensions (nominal)	133.35 mm x 31.25 mm	Refer to MO-309
	133.35 mm x 18.75 mm	Refer to MO-309
Pin Count	288	
DDR4 SDRAMs Supported	4 Gb, 8 Gb, 16 Gb	78/106-ball FBGA package for x4 devices. Refer to MO-207: variations DT-z, DW-z
Capacity	16 GB, 32GB, 64 GB, 128 GB	
SDRAM width	x4	No designs using x8 SDRAMs currently planned.
Serial PD, Thermal Sensor (SPD-TSE)	512 byte	See EE1004-v and TSE2004av specifications
Voltage Options	VDD: PC4 - 1.2 V $\pm$ 5%, PC4L - TBD	
	VPP: 2.5 V, + 10%, - 5%	This supply has VSS as its return path. It is a separate supply VDDSPD.
	VDDSPD: 2.5 V $\pm$ 10%	This supply has VSS as its return path. This supply is separate from the VPP. VDDSPD is shared between the SPD-TSE and RCD (register). The RCD only supports 2.5 V.
	12 V $\pm$ 15%	May be available on the connector but not used by LRDIMMs
Interface	1.2 V signaling	

2 Environmental Requirements

288-pin Load Reduced DDR4 SDRAM DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Table 2 — Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T _{OPR}	Operating Temperature (ambient)	0 to +55	°C	3
H _{OPR}	Operating Humidity (relative)	10 to 90	%	
T _{STG}	Storage Temperature	-50 to +100	°C	1
H _{STG}	Storage Humidity (without condensation)	5 to 95	%	1
P _{BAR}	Barometric Pressure (operating & storage)	105 to 69	kPa	1, 2
Note 1 Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Note 2 Up to 9850 ft. Note 3 The component maximum case temperature (T _{CASE}) shall not exceed the value specified in the DDR4 DRAM component specification.				

3 Connector Pinout and Signal Description

Table 3 — Pin Definition

Pin Name	Description	Pin Name	Description
A0–A17 ¹	SDRAM address bus	SCL	I ² C serial bus clock for SPD-TSE
BA0, BA1	SDRAM bank select	SDA	I ² C serial bus data line for SPD-TSE
BG0, BG1	SDRAM bank group select	SA0–SA2	I ² C slave address select for SPD-TSE
RAS_n ²	SDRAM row address strobe	PAR	SDRAM parity input
CAS_n ³	SDRAM column address strobe	VDD	SDRAM core power supply
WE_n ⁴	SDRAM write enable		
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines	C0, C1, C2	Chip ID lines for 3DS SDRAMs
CKE0, CKE1	SDRAM clock enable lines	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	SDRAM on-die termination control lines	VSS	Power supply return (ground)
ACT_n	SDRAM activate	VDDSPD	Serial SPD-TSE positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	SDRAM alert_n
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS9_t–TDQS17_t TDQS9_c–TDQS17_c	Dummy loads. Not used on LRDIMMs		
DQS0_t–DQS17_t	SDRAM data strobes (positive line of differential pair)	12 V	Optional power Supply on socket but not used on LRDIMM
DQS0_c–DQS17_c	SDRAM data strobes (negative line of differential pair)	RESET_n	Set DRAMs to a Known State
DBI0_n–DBI8_n	Data Bus Inversion. Not used on LRDIMMs.	EVENT_n	SPD-TSE signals a thermal event has occurred.
DM0_n–DM8_n	Data Mask. Not used on LRDIMMs		
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)	VTT	SDRAM I/O termination supply
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)	RFU	Reserved for future use

Note 1 Address A17 is only valid for 16 Gb x4 based SDRAMs.

Note 2 RAS_n is a multiplexed function with A16.

Note 3 CAS_n is a multiplexed function with A15.

Note 4 WE_n is a multiplexed function with A14.

Table 4 — Input/Output Functional Description

Symbol	Type	Function
CK0_t, CK0_c, CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT, and CKE, are disabled during power-down. Input buffer, excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n, CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection. CS_n is considered part of the command code.
C0, C1, C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On-Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 will be considered as Row Address A16, A15, and A14
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command being entered. These pins are multi-function. For example, for activation with ACT_n Low, the pins are Addresses A16, A15, and A14, but for non-activation commands with ACT_n High, these are Command pins for Read, Write, and other commands defined in the command truth table
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write, or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15, and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16 Gb x4 SDRAM configurations.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register, then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor-specific data sheets to determine which DQ is used.

Table 4 — Input/Output Functional Description (Cont'd)

Symbol	Type	Function
TDQS9_t-TDQS17_t TDQS9_c-TDQS17_c	Input	Dummy load for matching the loading for mixed populations of x8 based RDIMMs and x4 based RDIMMs. Not used on LRDIMMs.
DBI0_n-DBI8_n	Input/ Output	Data Bus Inversion. Not used on LRDIMMs.
DM0_n-DM8_n	Input	Data Mask. Not used on LRDIMMs.
DQS0_t-DQS17_t, DQS0_c-DQS17_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
PAR	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Output (Input)	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is an error in the CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is an error in the Command Address Parity Check, then ALERT_n goes LOW for a relatively long period until the ongoing DRAM internal recovery transaction is complete. During Connectivity Test mode, this pin functions as an input. Whether ALERT_n is used or not is system dependent.
RFU		Reserved for Future Use: No on DIMM electrical connection is present.
NC		No Connect: No on-DIMM electrical connection is present.
VDD ¹	Supply	Power Supply: 1.2 V $\pm$ 0.06 V
VSS	Supply	Ground
VTT	Supply	Power Supply for termination of Address, Command and Control, VDD/2.
VPP	Supply	DRAM Activating Power Supply: 2.5 V (2.375 V min, 2.75 V max)
VDDSPD	Supply	Power supply used to power the I2C bus on the SPD-TSE and register.
VREFCA	Supply	Reference voltage for CA
12 V	Supply	12 V supply not used on LRDIMMs

Note 1 For PC4, VDD is 1.2 V. For PC4L, VDD is TBD.

Table 5 — DDR4 288 Pin LRDIMM Pin Wiring Assignments

Front Side Pin Label	Pin	Pin	Back side Pin Label	Front Side Pin Label	Pin	Pin	Back side Pin Label
12 V, NC	1	145	12 V, NC	CK0_t	74	218	CK1_t
VSS	2	146	VREFCA	CK0_c	75	219	CK1_c
DQ4	3	147	VSS	VDD	76	220	VDD
VSS	4	148	DQ5	VTT	77	221	VTT
DQ0	5	149	VSS	KEY			
VSS	6	150	DQ1	EVENT_n	78	222	PARITY
TDQS9_t, DQS9_t, DM0_n, DBI0_n, NC	7	151	VSS	A0	79	223	VDD
TDQS9_c, DQS9_c, NC	8	152	DQS0_c	VDD	80	224	BA1
VSS	9	153	DQS0_t	BA0	81	225	A10/AP
DQ6	10	154	VSS	RAS_n/A16	82	226	VDD
VSS	11	155	DQ7	VDD	83	227	RFU
DQ2	12	156	VSS	CS0_n	84	228	WE_n/A14
VSS	13	157	DQ3	VDD	85	229	VDD
DQ12	14	158	VSS	CAS_n/A15	86	230	NC, SAVE_n
VSS	15	159	DQ13	ODT0	87	231	VDD
DQ8	16	160	VSS	VDD	88	232	A13
VSS	17	161	DQ9	CS1_n, NC	89	233	VDD
TDQS10_t, DQS10_t, DM1_n, DBI1_n, NC	18	162	VSS	VDD	90	234	NC, A17
TDQS10_c, DQS10_c, NC	19	163	DQS1_c	ODT1	91	235	NC, C2
VSS	20	164	DQS1_t	VDD	92	236	VDD
DQ14	21	165	VSS	C0, CS2_n, NC	93	237	NC, CS3_n, C1
VSS	22	166	DQ15	VSS	94	238	SA2
DQ10	23	167	VSS	DQ36	95	239	VSS
VSS	24	168	DQ11	VSS	96	240	DQ37
DQ20	25	169	VSS	DQ32	97	241	VSS
VSS	26	170	DQ21	VSS	98	242	DQ33
DQ16	27	171	VSS	TDQS13_t, DQS13_t, DM4_n, DBI4_n, NC	99	243	VSS
VSS	28	172	DQ17	TDQS13_c, DQS13_c, NC	100	244	DQS4_c
TDQS11_t, DQS11_t, DM2_n, DBI2_n, NC	29	173	VSS	VSS	101	245	DQS4_t
TDQS11_c, DQS11_c, NC	30	174	DQS2_c	DQ38	102	246	VSS
VSS	31	175	DQS2_t	VSS	103	247	DQ39
DQ22	32	176	VSS	DQ34	104	248	VSS
VSS	33	177	DQ23	VSS	105	249	DQ35
DQ18	34	178	VSS	DQ44	106	250	VSS
VSS	35	179	DQ19	VSS	107	251	DQ45
DQ28	36	180	VSS	DQ40	108	252	VSS
VSS	37	181	DQ29	VSS	109	253	DQ41
DQ24	38	182	VSS	TDQS14_t, DQS14_t, DM5_n, DBI5_n, NC	110	254	VSS
VSS	39	183	DQ25	TDQS14_c, DQS14_c, NC	111	255	DQS5_c
TDQS12_t, DQS12_t, DM3_n, DBI3_n	40	184	VSS				

Table 5 — DDR4 288 Pin LRDIMM Pin Wiring Assignments (Cont'd)

Front Side Pin Label	Pin	Pin	Back side Pin Label	Front Side Pin Label	Pin	Pin	Back side Pin Label
<i>TDQS12_c</i> , DQS12_c, <i>NC</i>	41	185	DQS3_c	VSS	112	256	DQS5_t
VSS	42	186	DQS3_t	DQ46	113	257	VSS
DQ30	43	187	VSS	VSS	114	258	DQ47
VSS	44	188	DQ31	DQ42	115	259	VSS
DQ26	45	189	VSS	VSS	116	260	DQ43
VSS	46	190	DQ27	DQ52	117	261	VSS
CB4, <i>NC</i>	47	191	VSS	VSS	118	262	DQ53
VSS	48	192	CB5, <i>NC</i>	DQ48	119	263	VSS
CB0, <i>NC</i>	49	193	VSS	VSS	120	264	DQ49
VSS	50	194	CB1, <i>NC</i>	<i>TDQS15_t</i> , DQS15_t, <i>DM6_n</i> , <i>DBI6_n</i> , <i>NC</i>	121	265	VSS
<i>TDQS17_t</i> , DQS17_t, <i>DM8_n</i> , <i>DBI8_n</i> , <i>NC</i>	51	195	VSS	<i>TDQS15_c</i> , DQS15_c, <i>NC</i>	122	266	DQS6_c
<i>TDQS17_c</i> , DQS17_c, <i>NC</i>	52	196	DQS8_c	VSS	123	267	DQS6_t
VSS	53	197	DQS8_t	DQ54	124	268	VSS
CB6, <i>NC</i>	54	198	VSS	VSS	125	269	DQ55
VSS	55	199	CB7, <i>NC</i>	DQ50	126	270	VSS
CB2, <i>NC</i>	56	200	VSS	VSS	127	271	DQ51
VSS	57	201	CB3, <i>NC</i>	DQ60	128	272	VSS
RESET_n	58	202	VSS	VSS	129	273	DQ61
VDD	59	203	CKE1	DQ56	130	274	VSS
CKE0	60	204	VDD	VSS	131	275	DQ57
VDD	61	205	RFU	<i>TDQS16_t</i> , DQS16_t, <i>DM7_n</i> , <i>DBI7_n</i> , <i>NC</i>	132	276	VSS
ACT_n	62	206	VDD	<i>TDQS16_c</i> , DQS16_c, <i>NC</i>	133	277	DQS7_c
BG0	63	207	BG1	VSS	134	278	DQS7_t
VDD	64	208	ALERT_n	DQ62	135	279	VSS
A12/BC_n	65	209	VDD	VSS	136	280	DQ63
A9	66	210	A11	DQ58	137	281	VSS
VDD	67	211	A7	VSS	138	282	DQ59
A8	68	212	VDD	SA0	139	283	VSS
A6	69	213	A5	SA1	140	284	VDDSPD
VDD	70	214	A4	SCL	141	285	SDA
A3	71	215	VDD	VPP	142	286	VPP
A1	72	216	A2	VPP	143	287	VPP
VDD	73	217	VDD	RFU	144	288	VPP

Note 1 Light colored text indicates functions that are not applicable for LRDIMM wiring. An example is the NC for pin 56 because LRDIMMs defined by this specification will always have DIMM wiring for this pin.

4 Power Details

4.1 DIMM Voltage Requirements

The DIMM voltage requirements and the SDRAM voltage requirements are not identical. There must be some allowance for a small voltage drop across the DIMM. Table 6 defines the requirements for the Host at the DIMM socket.

Some modules have lower current requirements. Any specific module must meet the SDRAM, DDR4RCD01, and DDR4DB01 voltage requirements for its worst case supply currents.

Table 6 — DDR4 LRDIMM DC Operating Voltage^{1,2,3} - 1.2 V operation

Symbol	Parameter	Voltage Rating (Volts)			Maximum Expected Current (AMPs)	Power State
		Minimum	Typical ⁴	Maximum		
VDD	Supply Voltage	1.16	1.21	1.26	11.7	Operational
VPP	Activation Supply Voltage	2.41	2.50	2.75	3.75	Operational
VTT ⁵	Termination Voltage	0.565	0.605	0.64	0.75	Operational
VTT at termination	Termination Voltage	0.95 x VDDmin ⁷ /2 (0.542)	-	1.05 x VDDmax ⁷ /2 (0.662)	0.75	Operational
VDDSPD	SPD-TSE Supply Voltage	2.41	2.5	2.75	0.75	Operational
V ₁₂ (Optional ⁶)	Additional Power for non-volatile technologies	10.2	12.0	13.8	1.17	Operational
		5.8	12.0	13.8	0.7	Backup power off
		5.8	12.0	13.8	500 u	Idle power off

Note 1 20 MHz bandwidth limited measurement for all voltages in the table.

Note 2 Voltages are measured at the DIMM gold fingers.

Note 3 The SDRAM specification must be met and takes precedence over this document.

Note 4 Typical voltage is platform-dependent, suggested value only.

Note 5 At the DIMM interface, VTT is the only voltage during normal operating conditions that can both source and sink current.

Note 6 If 12 volts is supplied it must meet these requirements.

Note 7 SDRAM VDD specification range.

4.1.1 VTT Range

At the termination, Vtt must be within;

Note 1 $> 0.95 \times V_{ddmin}/2 = (0.60V - 0.058V) = 0.542$

Note 2 $< 1.05 \times V_{ddmax}/2 = (0.60V + 0.061V) = 0.662$

VDDmin and VDDmax refer to the SDRAM specification range.

4.1.2 Load Line

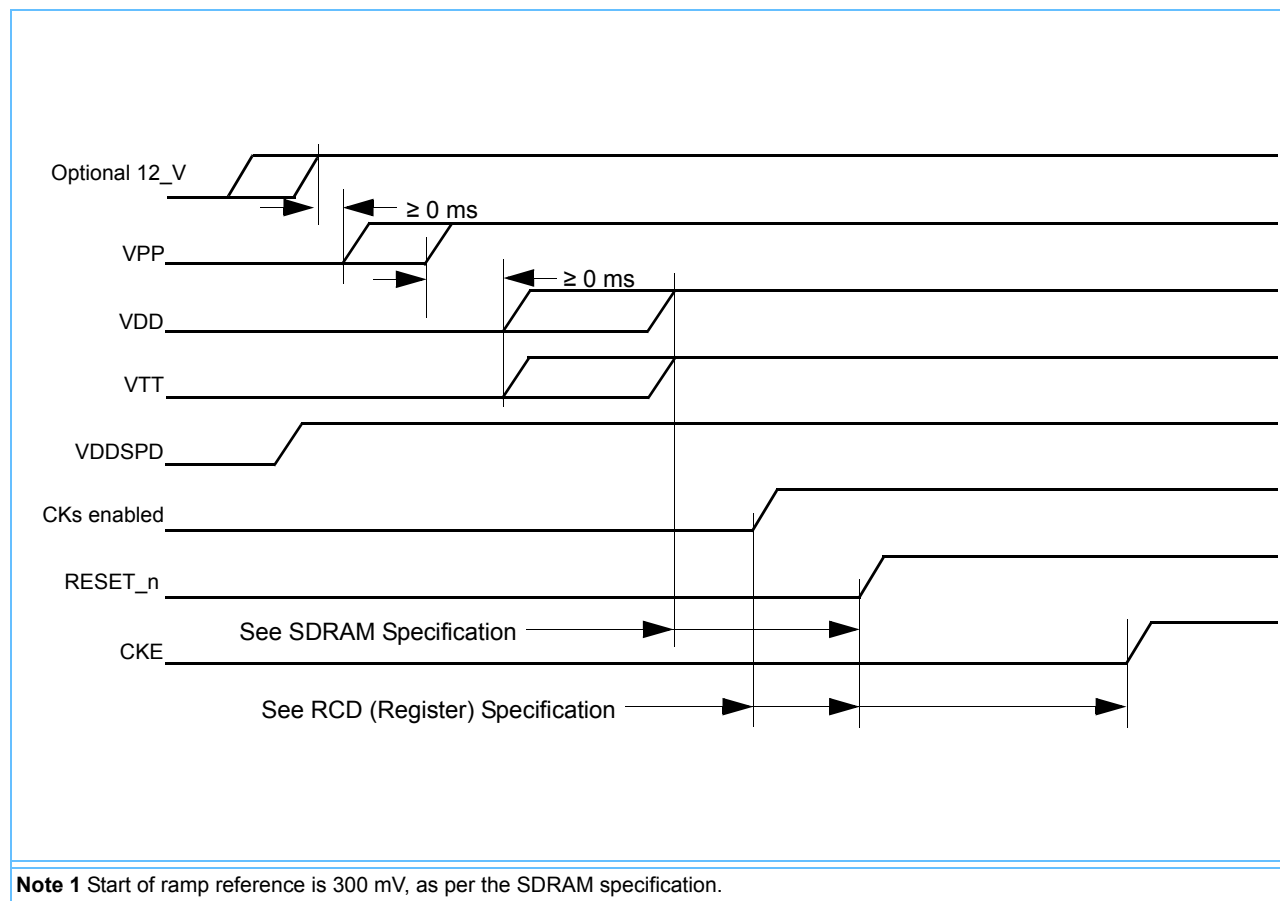
The VDD specification can be considered a load line requirement with the specified voltage drop of 16 mV @ 11.7 Amps being a point on the load line. The load line can be specified as $0.016V \geq Z_{DIMM} \times (I_{VDD} + i_{VDD})$ where ZDIMM is the DIMM power plane impedance, I_{VDD} is the DC DIMM current, and i_{VDD} is the band limited AC DIMM current.

4.2 Rules for Power-Up Sequence

VPP is the point of reference for power on sequence. There are several points of interest:

1. V₁₂ has to ramp with VPP prior to VPP such that it is available as a power source on the DIMMs that may have on-DIMM voltage regulator.
2. VDDSPD is an independent power source that has no specific relationship to the other power sources.
3. VTT has a specific relationship to VDD. That is $V_{TT} = V_{DD}/2$
4. The CK_t/CK_c input signals must be driven LOW (below the VIL(static) DDR4RCD01 parameter) throughout the VDD power ramp at least until the VDD supply voltage has settled to its final value.

Figure 1 — Graphical View of Power Sequence



4.3 12 V Power

The 12 V power source is optionally available for modules that support technologies other than homogeneously populated DRAM modules (e.g., not for UDIMMs, RDIMMs, and LRDIMMs). LRDIMMs may be inserted into sockets that provide 12 V support. If support for 12 V is provided, it must meet the requirements of Sections 4.1 and 4.2. Any module that uses 12 V must not interfere with the power sequence(s) of modules that do not support 12 V. 12 V is expected to remain valid during reduced power modes. The specific load requirements during these modes is product-specific.