

Annex A - Raw Card A

DDR4 Load Reduced DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
A0	PC4-LRDIMM_V090_RC_A0_20140806.brd	PC4-LRDIMM_V090_RC_A0_20140806-BOM.htm

Note 1 "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.

Module Configuration

SDRAM					DIMM											# of Address bits row/col	MO-309 variation
Die Density	Die Organization	Pkg. Type	# of Logical Ranks ^{1,2} per Pkg. Rank		# of Pkg. Ranks ^{1,2} per DIMM	# of Logical Ranks ^{1,2} per DIMM		# of SDRAM die per DIMM		Capacity per DIMM (GB)		DIMM Organization					
			Min.	Max.		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.				
2 Gb	512M x 4	SDP	-	-	2	2	2	36	36	8	8	1G x72	1G x72	15/10	AAxA		
		3DS	2	8	2	4	16	72	288	16	64	2G x72	16G x72				
4 Gb	1G x 4	SDP	-	-	2	2	2	36	36	16	16	2G x72	2G x72	16/10	AAxA		
		3DS	2	8	2	4	16	72	288	32	128	4G x72	32G x72				
8 Gb	2G x 4	SDP	-	-	2	2	2	36	36	32	32	4G x72	4G x72	17/10	AAxA		
		3DS	2	8	2	4	16	72	288	64	256	8G x72	64G x72				
16 Gb	4G x 4	SDP	-	-	2	2	2	36	36	64	64	8G x72	8G x72	18/10	AAxA		
		3DS	2	8	2	4	16	72	288	128	512	16G x72	128G x72				

Note 1 When populated with single die package (SDP), package ranks per DIMM=2.

Note 2 When populated with single load stacked packages (3DS), logical ranks per package rank = 2-8. Logical ranks per DIMM = 4-16.

SDRAM Configuration

Supported DRAM Outline (Width x Length) nom.	# of Bank groups/ Banks in a group	SDRAM Package Type	Package Type	MO-207 variation
11.0 x 11.5	4/4	78 Ball FBGA	SDP, 2H/4H/8H 3DS	DW-z

Note 1 SDP is a single die per package. 2H/4H/8H denotes number of dies stacked using 3DS stacking.

Supported Speeds

Raw Card	Speed	PC4-1333	PC4-1600	PC4-1866	PC4-2133	PC4-2400	PC4-2666	PC4-3200	Notes
A0	DDR4	P	P	P	P				1, 2

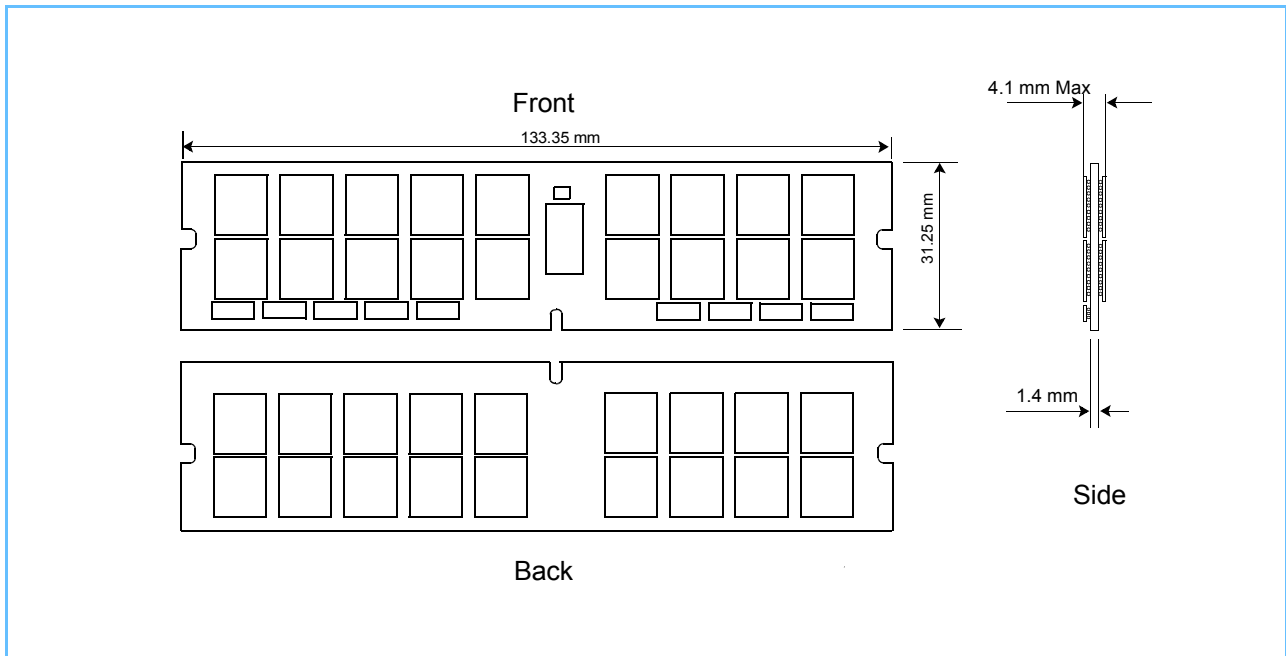
Note 1 X reflects speed grades approved from previous ballots.

Note 2 P denotes speed grades being proposed for this most recent ballot

Design Deviations

Note 1 None.

General Layout



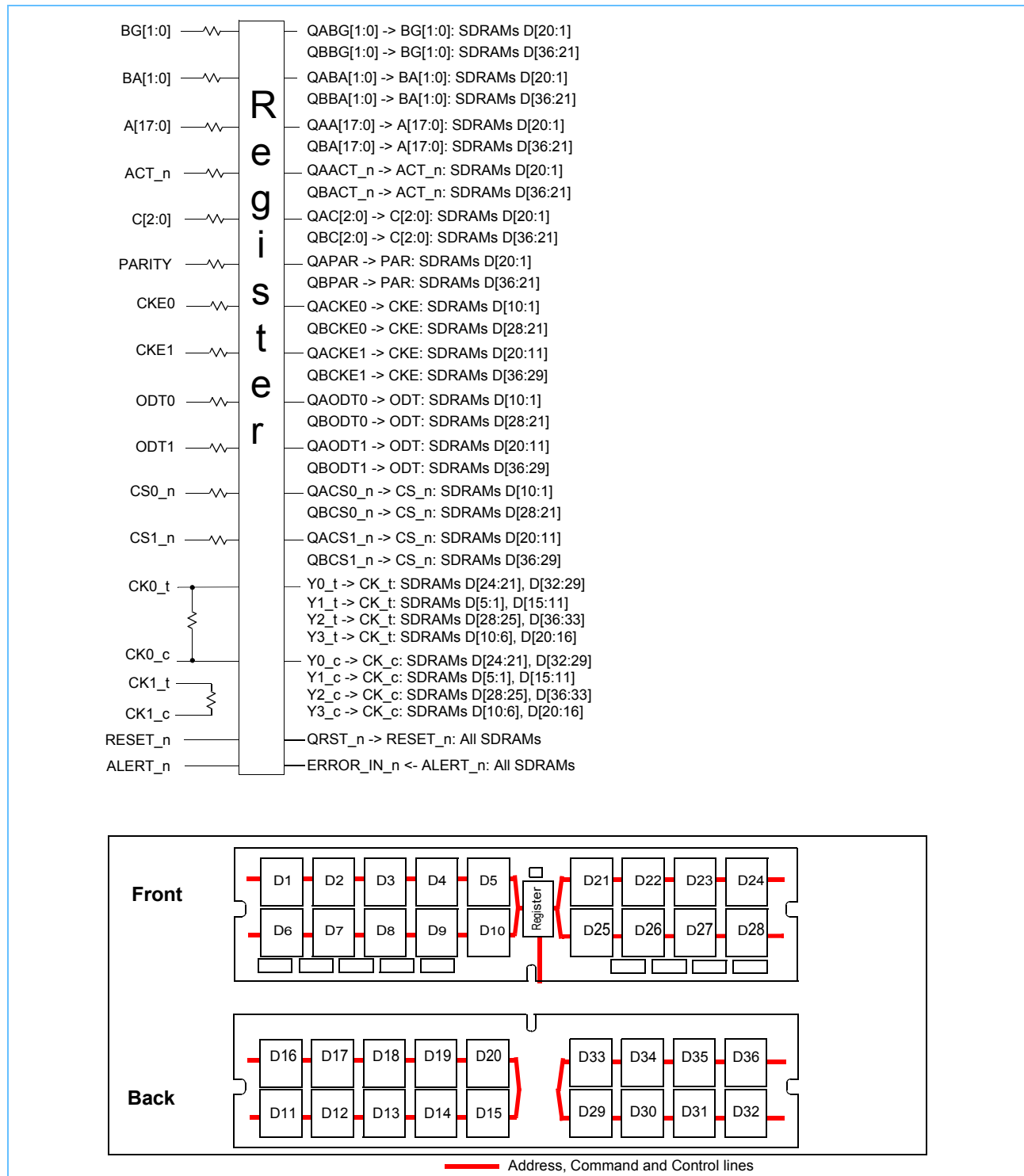
Note 1 Refer to MO-309 for more detailed information.

Note 2 Variation is AAxA (A Module height, A Module thickness, x plating, A Key Position).

Note 3 Module thickness may vary with DRAM thickness. Variation A is valid for DRAMs less than or equal to 1.2 mm maximum and not having a heat spreader attached.

Functional Block Diagram

x72 DIMM, populated as two package ranks of x4 DDR4 SDRAMs (Part 1 of 3)



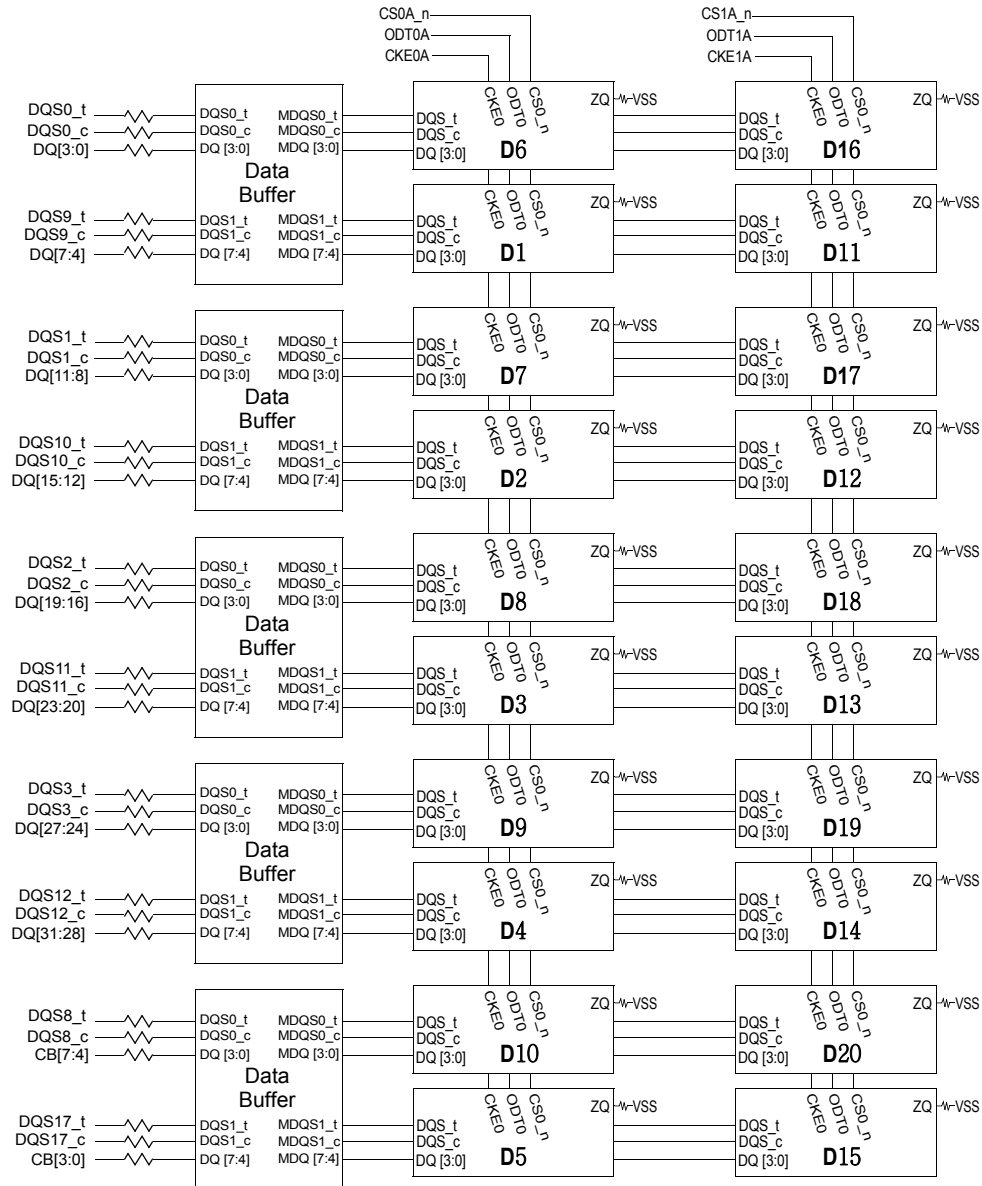
Note 1 CK0_t, CK0_c terminated with 120 $\Omega \pm 5\%$ resistor.

Note 2 CK1_t, CK1_c terminated with 120 $\Omega \pm 5\%$ resistor but not used.

Note 3 Unless otherwise noted, resistors are 22 $\Omega \pm 5\%$.

Functional Block Diagram

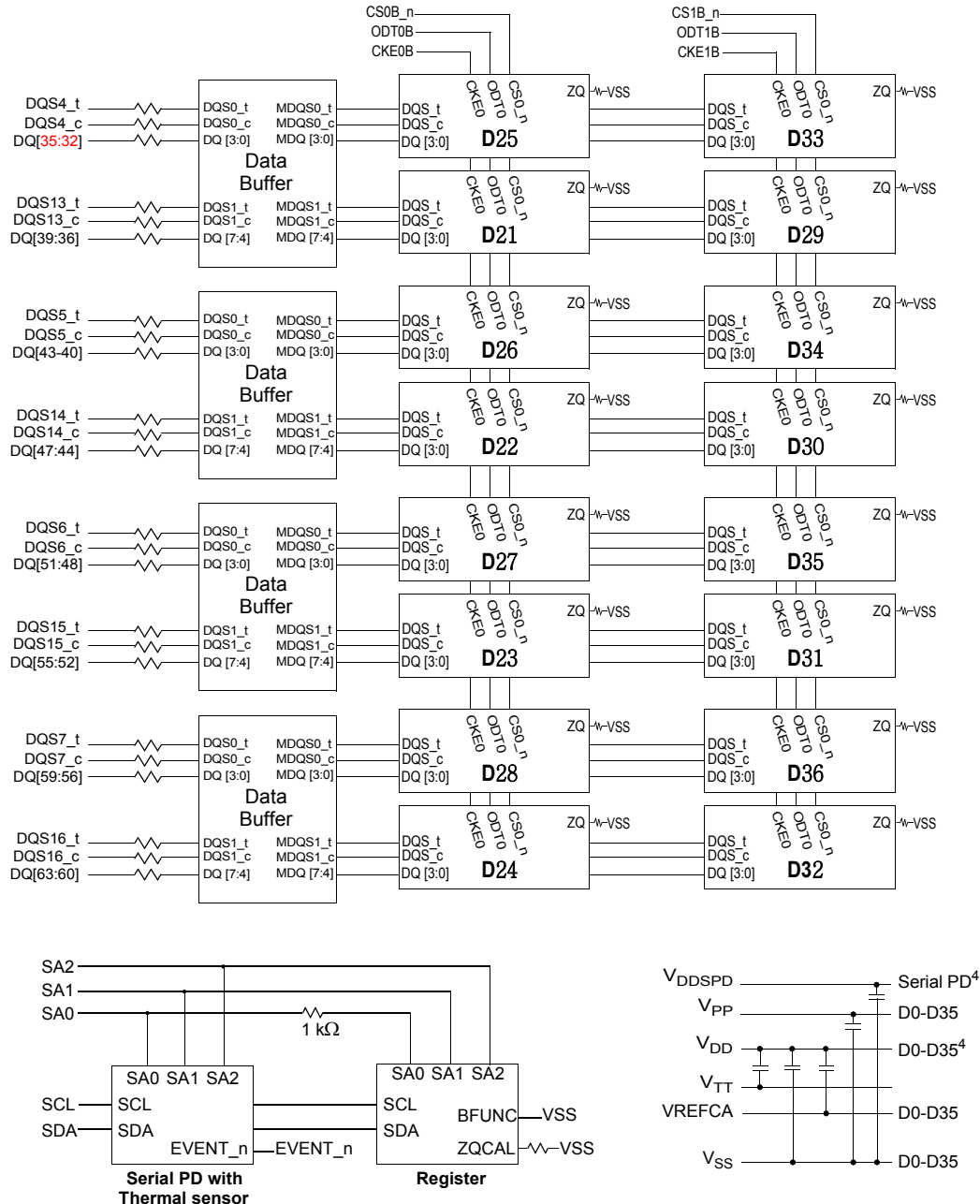
x72 DIMM, populated as two package ranks of x4 DDR4 SDRAMs (Part 2 of 3)



Note 1 ZQ resistors are $240\ \Omega \pm 1\%$. For all other resistor values, refer to the appropriate wiring diagram.
Note 2 See the Net Structure diagrams for all resistors associated with the command, address, and control bus.
Note 3 TEN pin of SDRAMs is tied to VSS.

Functional Block Diagram

x72 DIMM, populated as two package ranks of x4 DDR4 SDRAMs (Part 3 of 3)



Registered Clock Driver, Input Loading and Test Points

Refer to the DDR4RCD01 and DDR4DB01 vendor data sheets for all technical specifications and requirements. The DDR4RCD01 and DDR4DB01 component will be referred to as the register and data buffer throughout this document.

Input Loading

Signal Names	Input to Device	Loads
CK0_t, CK0_c	Register	1
CK1_t, CK1_c ²	Termination Resistor Only	1 ³
RESET_n	Register	1
CKE[1:0], ODT[1:0]	Register	1 ¹
Ax, BAx, BGx, RAS_n, CAS_n, WE_n, PARITY, ACT_n	Register	1 ¹
CS[1:0]_n, C[2:0]	Register	1 ¹
ALERT_n	Register	1
DQ, CB, DQS_t, DQS_c	Data Buffer	1 ²
SCL, SDA, SA[2:0]	SPD with Thermal Sensor, Register	2
EVENT_n	SPD with Thermal Sensor	1
Note 1 Programmable resistive terminations are available on the Register. Note 2 On-Die-Terminations are available on the Data Buffers. Note 3 Connected but not used.		

Test Point Locations

Signal Group	Signal	Signal locations
Address/Command/Control/PARITY	Pre Register	22 Ω series resistor. Closer to the register provides better SI.
	Post Register	Termination resistors on the ends of the module.
DQ,CB	Series resistor	15 Ω resistors
DQS_t, DQS_c	Series resistor	15 Ω resistors
MDQ,MCB		No convenient access.
MDQS_t, MDQS_c		No convenient access.
Clock	Termination resistor	120 Ω termination resistor.
	Post Register	Termination resistors on the ends of the module.
Note 1 Refer to the registration package for additional test point information.		