

Annex B - Raw Card B

DDR4 Registered DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
B0	PC4-LRDIMM_V091_RC_B0_20131203.brd	PC4-LRDIMM_V091_RC_B0_20131207-BOM.txt

Note: "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.

Module Configuration

SDRAM					DIMM										# of Address bits row/col	MO-309 variation
Die Density	Die Organization	Pkg. Type	# of Logical Ranks ^{1,2} per Package Rank		# of Package ranks ^{1,2} per DIMM	# of Logical Ranks ³ per DIMM		# of SDRAM die per DIMM		Capacity per DIMM (GB)		Organization of DIMM				
			Min.	Max.		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.			
2Gbit	512M x 4	SDP	-	-	2	2		36		8		1Gx72		15/10	AAxA	
		3DS	2	8	2		16		288		64		16Gx72			
4Gbit	1G x 4	SDP	-	-	2	2		36		16		2Gx72		16/10	AAxA	
		3DS	2	8	2		16		288		128		32Gx72			
8Gbit	2G x 4	SDP	-	-	2	2		36		32		4Gx72		17/10	AAxA	
		3DS	2	8	2		16		288		256		64Gx72			
16Gbit	4G x 4	SDP	-	-	2	2		36		64		8Gx72		18/10	AAxA	
		3DS	2	8	2		16		288		512		128Gx72			

Note 1 When populated with single die package (SDP), package ranks per DIMM=2.

Note 2 When populated with single load stacked packages (3DS), logical ranks per package rank = 2-8. Logical ranks per package rank x package ranks per DIMM = 4-16.

Note 3 Used only for DIMM capacity calculation because logical rank is only defined for 3DS, not SDP.

SDRAM Configuration

Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM BA/BG	SDRAM Package Type	Package Type	MO-207 variation
9.0 x 13.0	2/2	78 Ball FBGA	SDP/3DS	DW-z

Note 1 SDP is a single die per package. 3DS is typically 2 die or 4 die or 8 die stacks.

Supported Speeds

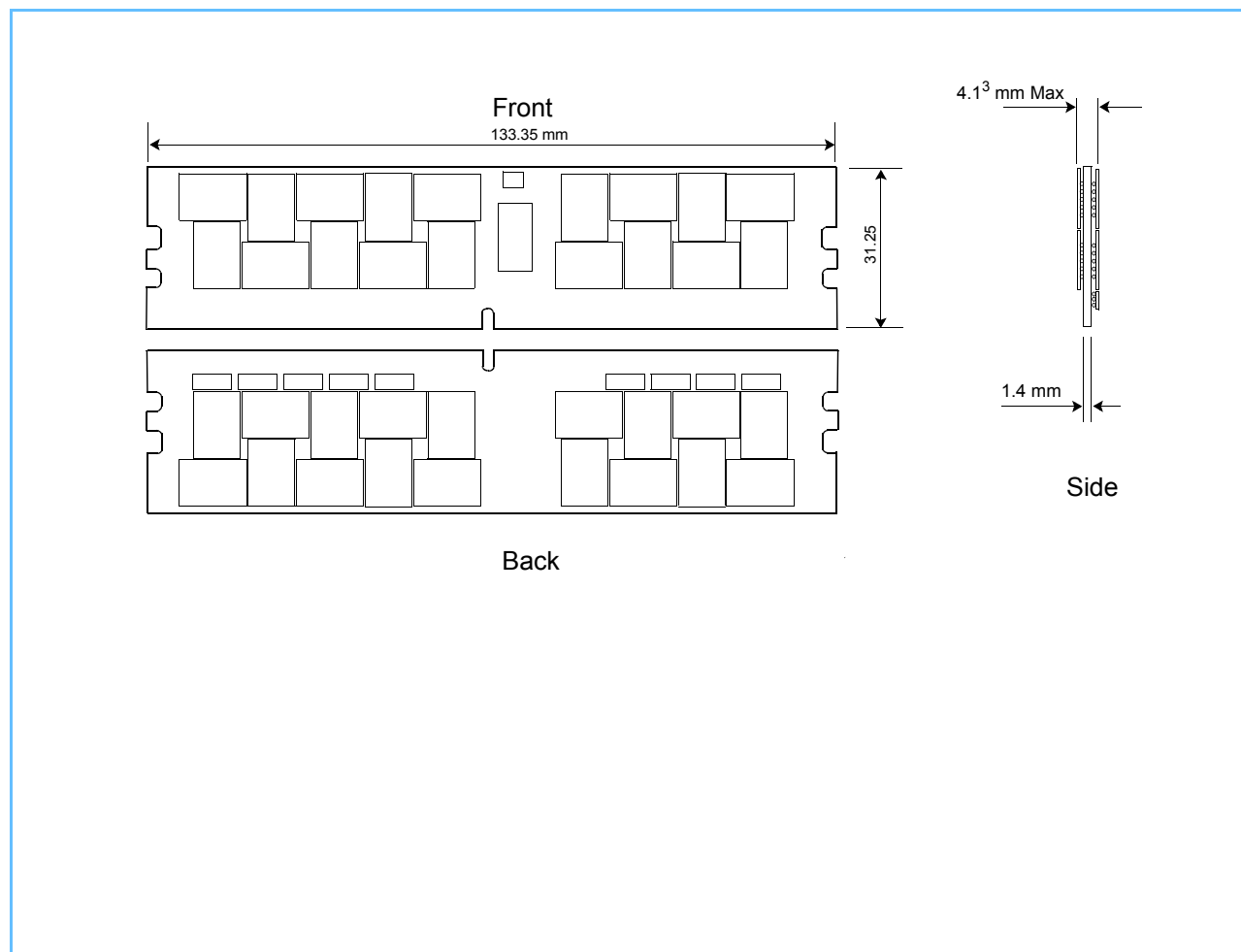
Raw Card	Speed	PC4-1333	PC4-1600	PC4-1866	PC4-2133	PC4-2400	PC4-2666	PC4-3200	Notes
B0	DDR4	P	P	P	P				1, 2
B0	DDR4L								1, 2

Note 1 X reflects speed grades approved from previous ballots.
Note 2 P denotes speed grades being proposed for this most recent ballot

Design Deviations

Note 1 Micro-vias used on this design layers 11 to 12.

General Layout



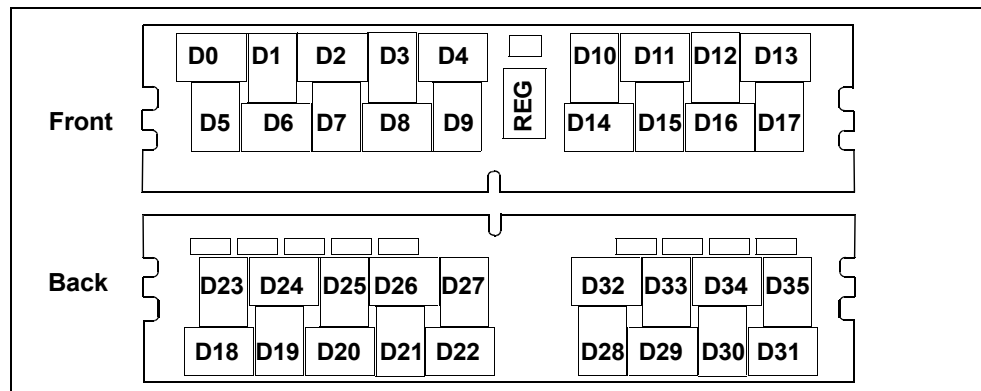
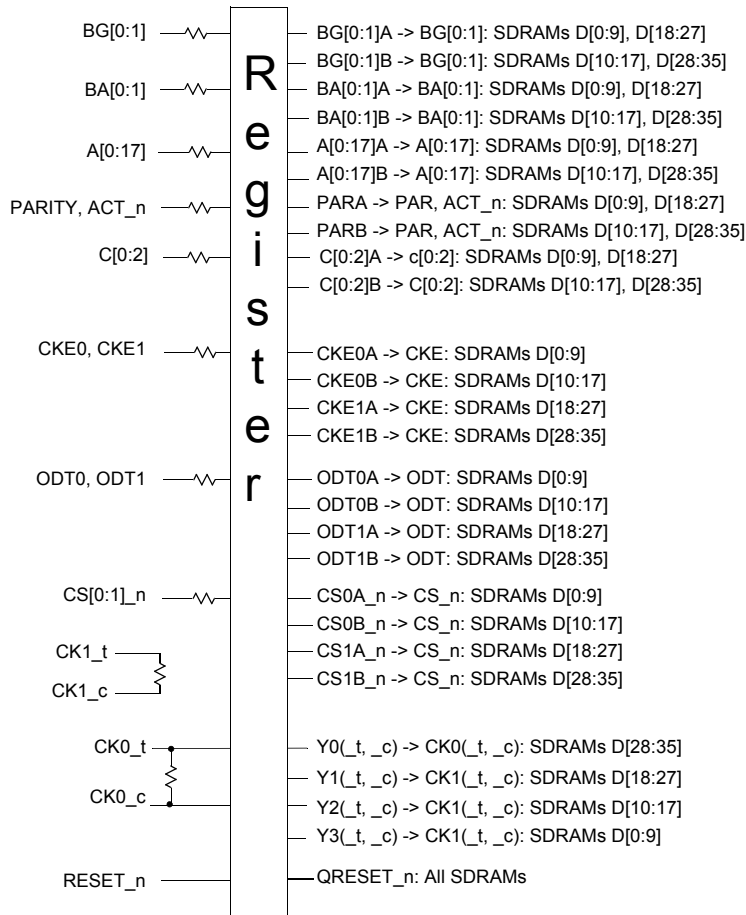
Note 1 Refer to MO-309 for more detailed information.

Note 2 Variation is AAxA (B-Module height, A-Module thickness, x-plating, A-Key Position).

Note 3 Module thickness may vary with DRAM thickness. Variation A is valid for DRAMs less than or equal to 1.2 mm maximum and not having a heat spreader attached.

Functional Block Diagram

x72 DIMM, populated as two package ranks of x4 DDR4 SDRAMs (Part 1 of 3)



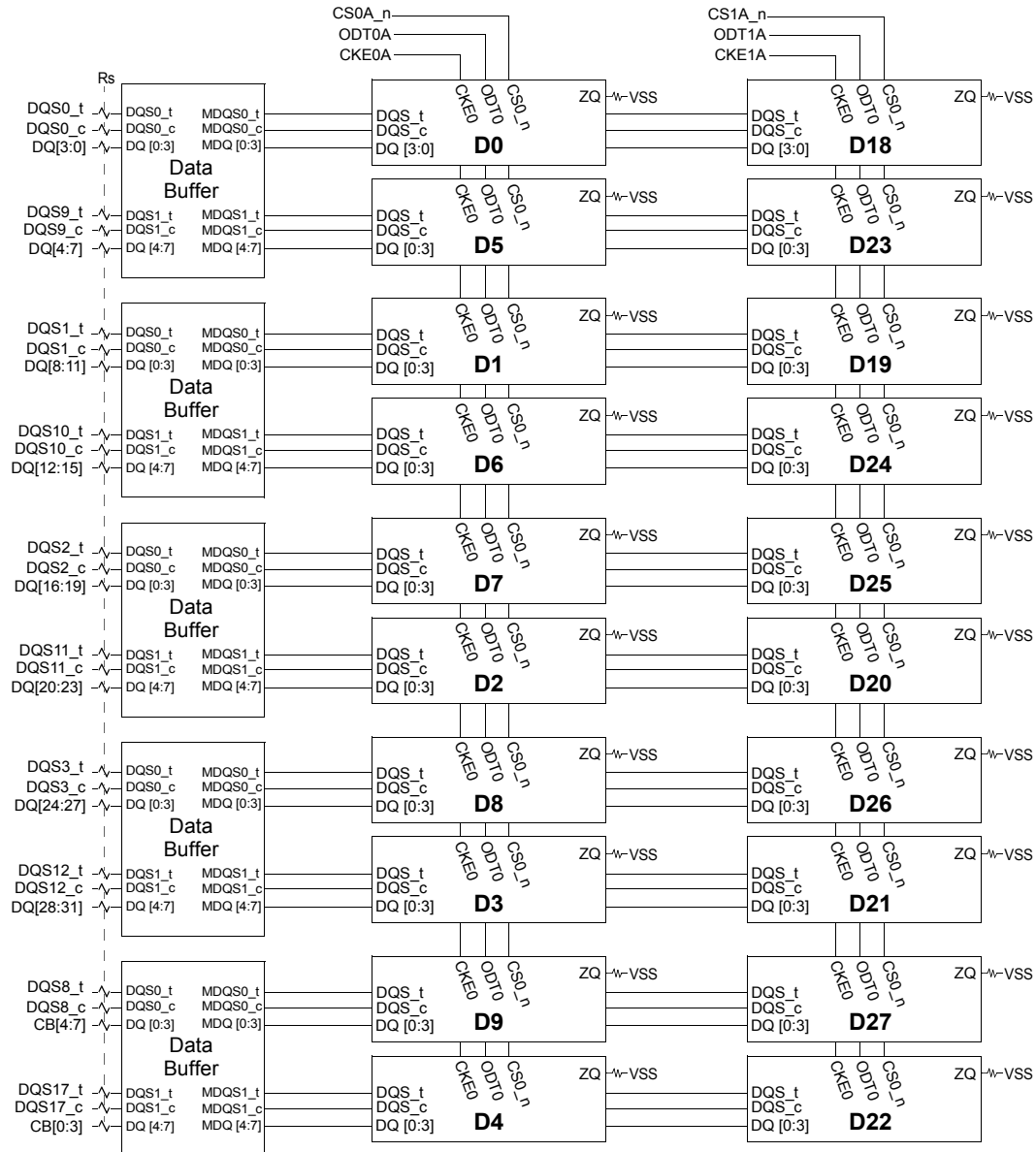
Note 1 CK0_t, CK0_c terminated with 120Ω ± 5% resistor.

Note 2 CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.

Note 3 Unless otherwise noted resistors are 22Ω ± 5%.

Functional Block Diagram

x72 DIMM, populated as two package ranks of x4 DDR4 SDRAMs (Part 2 of 3)



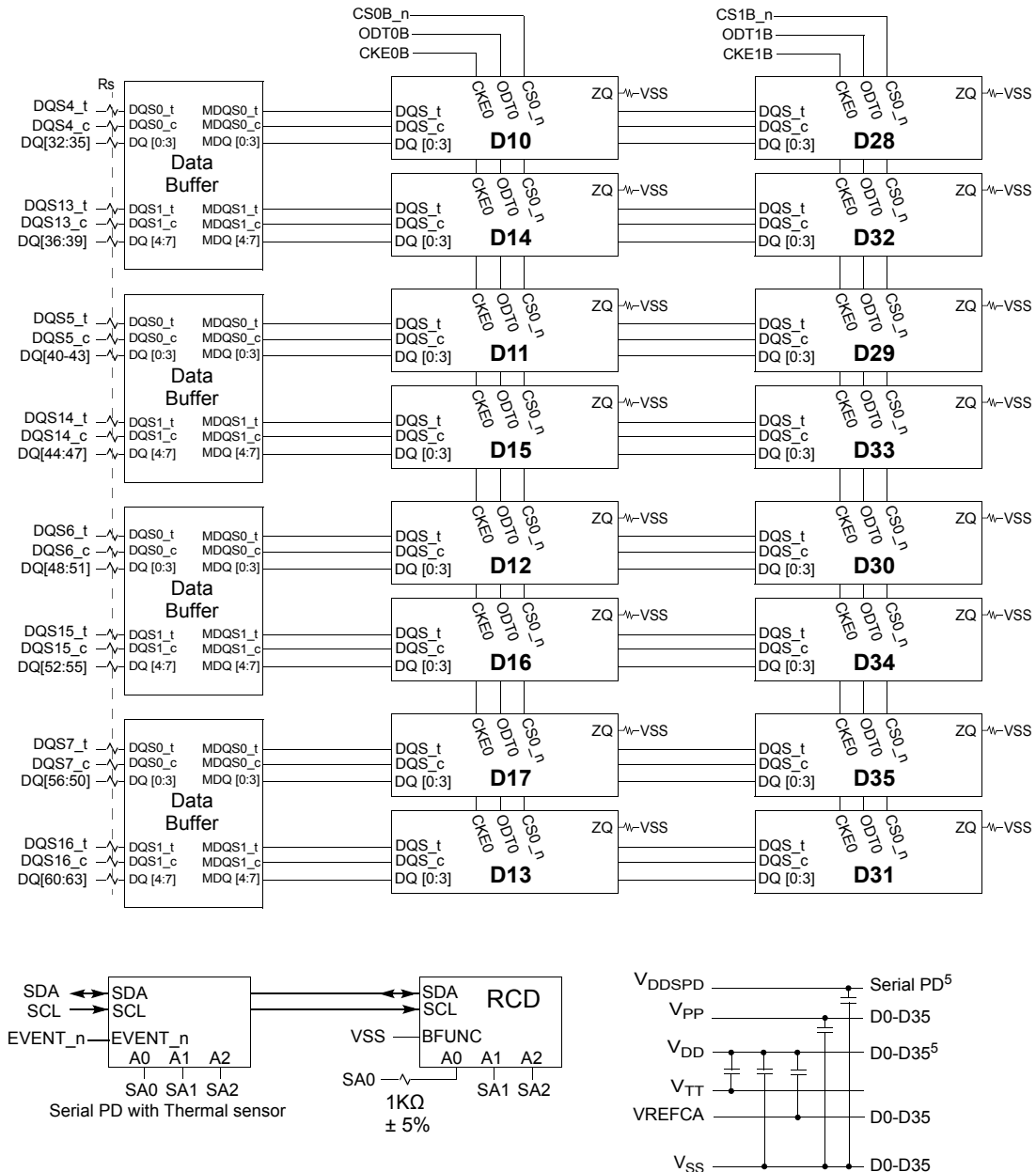
Note 1 ZQ resistors are $240\Omega \pm 1\%$.

Note 2 Rs resistors are $15\Omega \pm 5\%$.

Note 3 See the Net Structure diagrams for all resistors associated with the command, address and control bus.

Note 4 TEN pin of SDRAMs is tied to VSS.

x72 DIMM, populated as two package ranks of x4 DDR4 SDRAMs (Part 3 of 3)



Note 1 ZQ resistors are $240\Omega \pm 1\%$.

Note 2 Rs resistors are $15\Omega \pm 5\%$.

Note 3 See the Net Structure diagrams for all resistors associated with the command, address and control bus.

Note 4 TEN pin of SDRAMs is tied to VSS.

Note 5 VDDSPD is also applied to the register. VDD is also applied to the register and the data buffers.

Registered Clock Driver, Input Loading and Test Points

Refer to the DDR4RCD01 vendor data sheets for all technical specifications and requirements.
The DDR4RCD01 component will be referred to as the register throughout this document.

Loading

Signal Names	Input to Device	Loads
CK0_t, CK0_c	Register	1
CK1_t, CK1_c ²	Termination Resistor Only	1 ²
RESET_n	Register	1
CS0_n, CS1_n, CKE0, CKE1, ODT0, ODT1	Register	1 ¹
Ax, BAx, BGx, ACT_n, PARITY	Register	1 ¹
C0, C1, C2	Register	1 ¹
DQ, CB, DQS_t, DQS_c	SDRAM	1
SCL, SDA, SA[2:0]	SPD with Thermal Sensor, Register	2
EVENT_n	SPD with Thermal Sensor	1
ALERT_n	Register	1
Note 1 Programmable resistive terminations are available in the Register.		
Note 2 Connected but not used.		

Test Point Locations

Signal Group	Signal Area	Signal locations
Address/Command/ Control/PARITY	Pre Register	22 Ohm series resistor. Closer to the register provides better SI.
	Post Register	Termination resistors on the ends of the module.
DQ,CB		Some vias near Data Buffers.
DQS_t, DQS_c		No convenient access.
MDQ,MCB		No convenient access.
MDQS_t, MDQS_c		No convenient access.
Clock	Termination resistor	120 Ohm termination resistor.
	Post Register	Termination resistors on the ends of the module.
Note 1 Refer to the registration package for additional test point information.		

Manufactured DIMM Improvement

Manufactured DIMMs may improve on the reference design as long as the skew is reduced relative to the reference design. It is a requirement that improvements not move the basic timing away from the reference design such that system integrity is jeopardized for systems defined to operate with the original reference design. The skew values reported in the tables only account for skew related to the DIMM PCB traces and vias of the reference design. No other error sources are included. The only exception is if the skew evaluation chose to use an actual SDRAM package or an idealized (uniform) package. This should be identified in a note below each table. The skew is only intended to document the design as a reference point if a manufacturer chooses to improve the design over the reference design. The skew is not a measurable value. Measured values of skew will always be greater than the values reported in the tables because other error sources will also be included.