

Annex D - Raw Card D

DDR4 Load Reduced DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
D0	PC4-LRDIMM_V050_RC_D0_20130828.brd	PC4-LRDIMM_V050_RC_D0_20130828_BOM.xlsx
D1	PC4-LRDIMM_V070_RC_D1_20141106.brd	PC4-LRDIMM_V070_RC_D1_20141106_BOM.xlsx
D2	PC4-LRDIMM_RC_D2_R050_V200_20160229.brd	PC4-LRDIMM_RC_D2_R050_V200_20160229_BOM.xlsx

Note "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.

Module Configuration

DIMM		SDRAM		# of SDRAM die	# of Package Ranks per DIMM	# of Logical-Ranks per DIMM	# of Address bits row/col	MO-309 variation
Maximum Capacity	Organization	Die Density	Organization					
16 GB	2G x72	2 Gb	512M x 4	36	4	4	15/10	AAxA
32 GB	4G x72	4 Gb	1G x 4	36	4	4	16/10	AAxA
64 GB	8G x72	8 Gb	2G x 4	36	4	4	17/10	AAxA
128 GB	16G x72	16 Gb	4G x 4	36	4	4	18/10	AAxAN

Note When populated Dual Die Packages (DDP), logical ranks has no meaning.

SDRAM Configuration

R/C	Supported DRAM Outline (Width x Length) max. (mm)	# of Banks in SDRAM BA/BG	SDRAM Package Type	Package Type	MO-207 variation
D0	11.0 x 11.5	2/2	78 Ball FBGA	DDP	DW-z
D1	11.0 x 11.5	2/2	78 Ball FBGA	DDP	DW-z
D2	11.0 x 11.5	2/2	78 Ball FBGA	DDP	DW-z

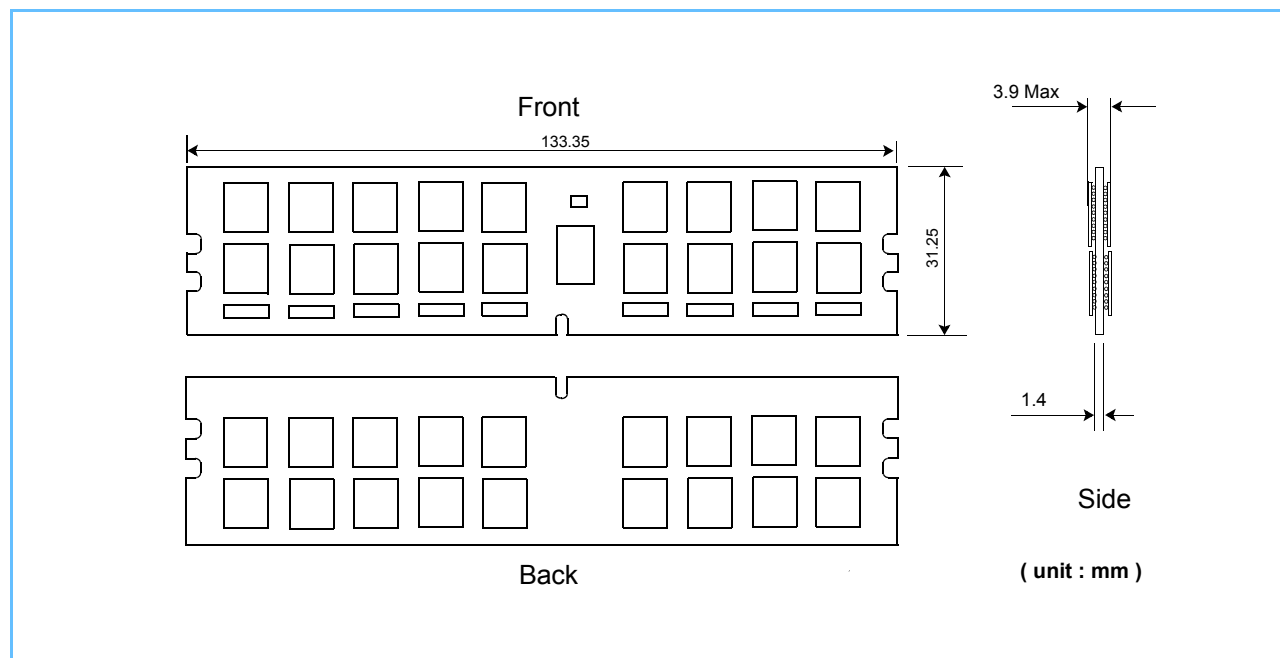
Note DDP is a Dual Die per Package.

Supported Speeds

Raw Card	Speed	PC4-1333	PC4-1600	PC4-1866	PC4-2133	PC4-2400	PC4-2666	PC4-3200	Notes
D0	DDR4	X	X	X	X				1, 2
D1	DDR4	X	X	X	X	X			1, 2
D2	DDR4	N	N	N	N	N	N		1, 2

Note 1 X reflects speed grades approved from previous ballots.
Note 2 N denotes speed grades being proposed for this most recent ballot

General Layout

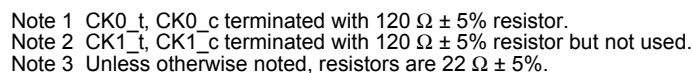


Note 1 Refer to MO-309 for more detailed information.

Note 2 Variation is AAxA (A Module height, A Module thickness, x plating, A Key Position).

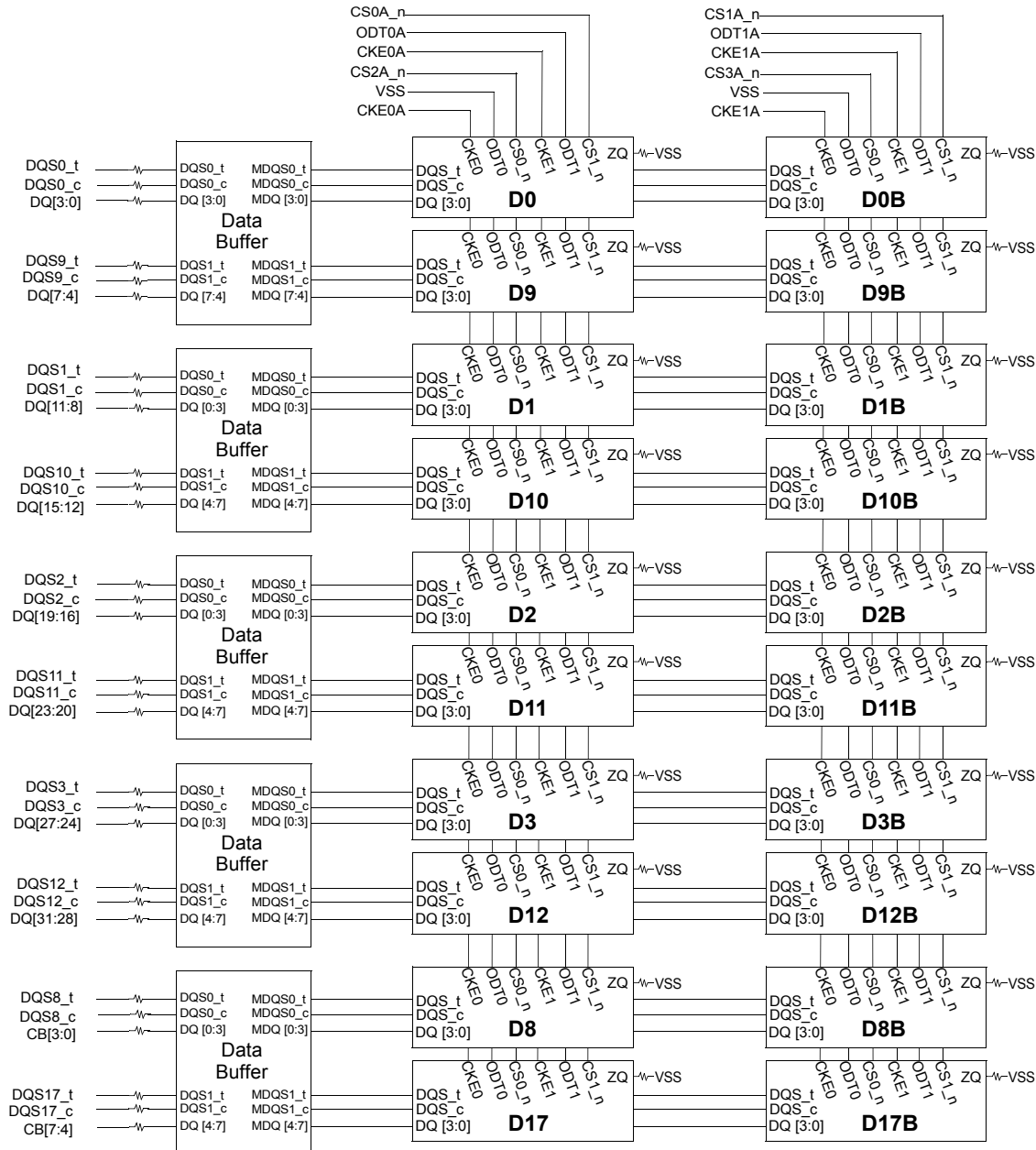
Note 3 Module thickness may vary with DRAM thickness and passive components.

x72 DIMM, populated as four package ranks of x4 DDR4 SDRAMs (Part 1 of 3)



Functional Block Diagram

x72 DIMM, populated as four package ranks of x4 DDR4 SDRAMs (Part 2 of 3)



Note 1: ZQ resistors are 240 $\Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.

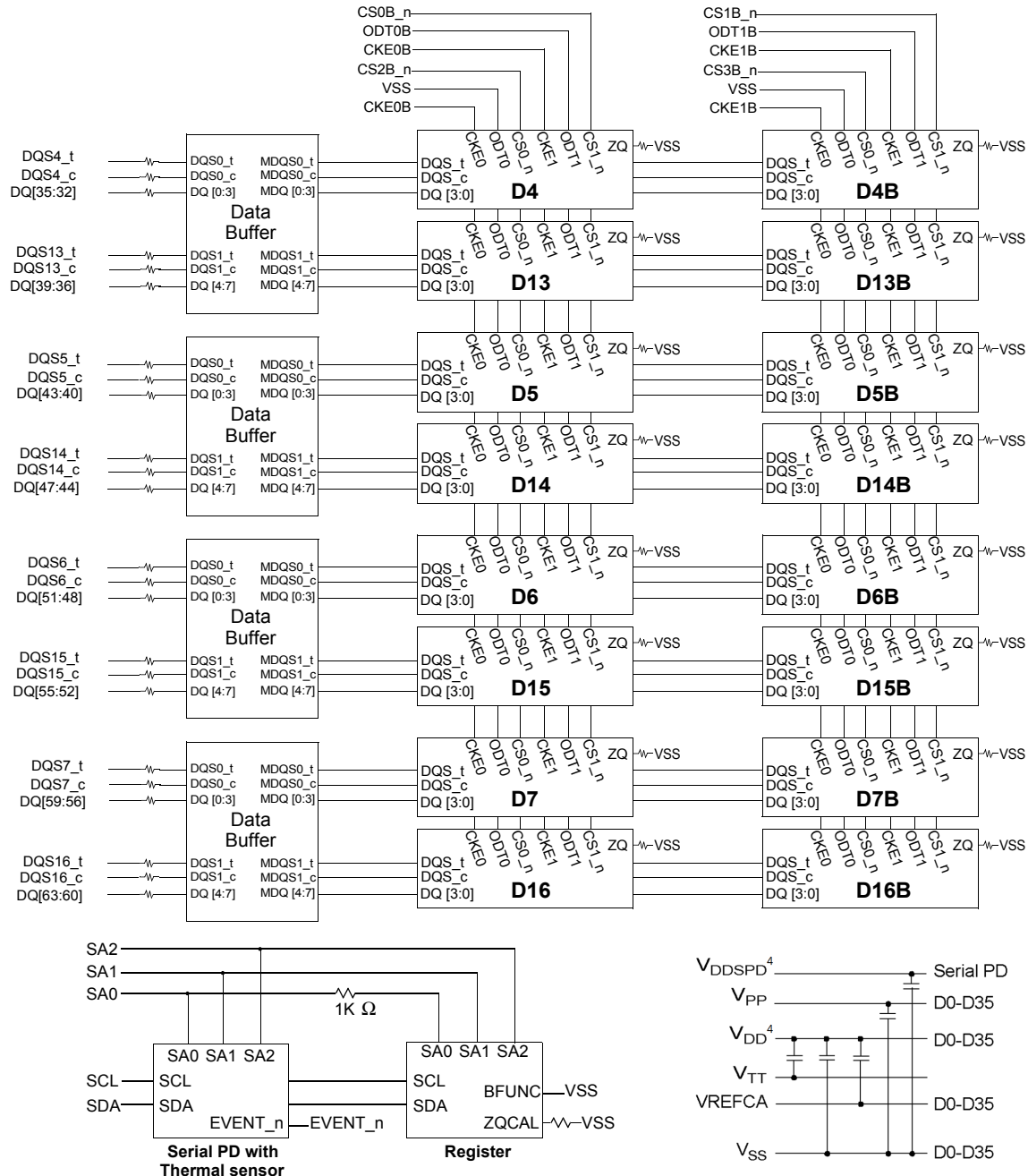
Note 2: See the Net Structure diagrams for all resistors associated with the command, address and control bus.

Note 3: TEN Pin of SDRAMs is tied to VSS

Note 4: DQ stub resistors are 15 $\Omega \pm 5\%$. For all other resistor values refer to the appropriate wiring diagram.

Functional Block Diagram

x72 DIMM, populated as four package ranks of x4 DDR4 SDRAMs (Part 3 of 3)



Registered Clock Driver, Loading and Test Points

Refer to the DDR4RCD01 vendor data sheets for all technical specifications and requirements.
The DDR4RCD01 component will be referred to as the register throughout this document.

Loading

Signal Names	Input to Device	Loads
CK0_t, CK0_c	Register	1
CK1_t, CK1_c ²	Termination Resistor Only	1 ²
RESET_n	Register	1
CS0_n, CS1_n, CS2_n, CS3_n, CKE0, CKE1, ODT0, ODT1	Register	1 ¹
Ax, BAx, BGx, RAS_n, CAS_n, WE_n, PARITY, ACT_n	Register	1 ¹
ALERT_n	Register	1
C2	Register	1 ²
DQ, CB, DQS_t, DQS_c	Data Buffer	1
SCL, SDA, SA[2:0]	SPD with Thermal Sensor, Register	2
EVENT_n	Output of SPD with Thermal Sensor	1
Note 1 Programmable resistive terminations are available on the Register.		
Note 2 Connected but not used.		

Test Point Locations

Signal Group	Signal	Signal locations
Address/Command/ Control/PARITY	Pre Register	22 Ω series resistor. Closer to the register provides better SI.
	Post Register	Termination resistors on the ends of the module.
DQ,CB	Series resistor	NO Convenient test point
DQS_t, DQS_c	Series resistor	NO Convenient test point
MDQ, MCB	Series resistor	NO Convenient test point
MDQS_t, MDQS_c	Series resistor	NO Convenient test point
Clock	Termination resistor	120 Ω termination resistor.
	Post Register	Termination resistors on the ends of the module.
Note Refer to the registration package for additional test point information.		

DQ Map for CRC

See Common section of the DDR4 LRDIMM Design Specification for information on interpreting the DQ Mapping table.

SPD Values for DQ Mapping

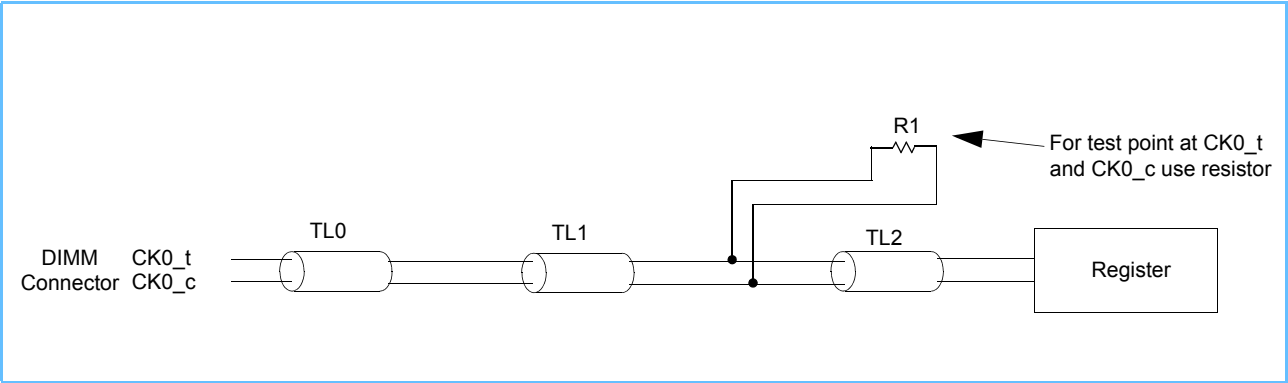
DQ Bits as defined by connector	SPD Byte (Decimal)	SPD Value (Hex)	DQ Bits as defined by connector	SPD Byte (Decimal)	SPD Value (Hex)
DQ0, DQ1, DQ2, DQ3	60	0B	DQ32, DQ33, DQ34, DQ35	70	0B
DQ4, DQ5, DQ6, DQ7	61	0B	DQ36, DQ37, DQ38, DQ39	71	0B
DQ8, DQ9, DQ10, DQ11	62	0B	DQ40, DQ41, DQ42, DQ43	72	0B
DQ12, DQ13, DQ14, DQ15	63	0B	DQ44, DQ45, DQ46, DQ47	73	0B
DQ16, DQ17, DQ18, DQ19	64	0B	DQ48, DQ49, DQ50, DQ51	74	0B
DQ20, DQ21, DQ22, DQ23	65	0B	DQ52, DQ53, DQ54, DQ55	75	0B
DQ24, DQ25, DQ26, DQ27	66	0B	DQ56, DQ57, DQ58, DQ59	76	0B
DQ28, DQ29, DQ30, DQ31	67	0B	DQ60, DQ61, DQ62, DQ63	77	0B
CB0, CB1, CB2, CB3	68	0B			
CB4, CB5, CB6, CB7	69	0B			

Manufactured DIMM Improvement

Manufactured DIMMs may improve on the reference design as long as the skew is reduced relative to the reference design. It is a requirement that improvements not move the basic timing away from the reference design such that system integrity is jeopardized for systems defined to operate with the original reference design. The skew values reported in the tables only accounts for skew related to the DIMM PCB traces and vias of the reference design. No other error sources are included. The only exception is if the skew evaluation chose to use an actual SDRAM package or an idealized (uniform) package. This should be identified in a note below each table. The skew is only intended to document the design as a reference point if a manufacturer chooses to improve the design over the reference design. The skew is not a measurable value. Measured values of skew will always be greater than the values reported in the tables because other error sources will also be included. Manufacturer are allowed additional rules for length and placement adjustment to account for variations in the DRAMs. See Section 6.3 of the DDR4 SDRAM Registered DIMM Design Specification: Modified Rules for RDIMM Designs at 2666 Mbps and Higher.

Clock Input Net Structure

Net Structure Routing for Register Clock Input

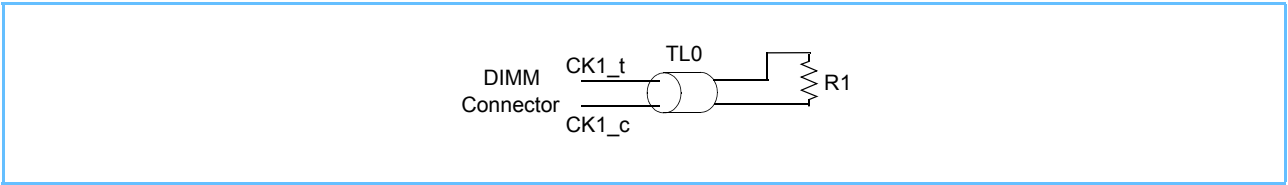


Clock Lengths for Register Input Net Structures

R/C	Signal	TL0	TL1	TL2	TL0 + TL1 + TL2	R1 (Ω)
D0	CK0_t	1.6	21.8	0.5	23.9	120 ± 5%
D1	CK0_c	1.6	21.8	0.5	23.9	
D2						

Note All distances are given in mm and must be kept within a tolerance of ± 0.1 mm.

Net Structure Routing for Unused Clock DIMM Termination



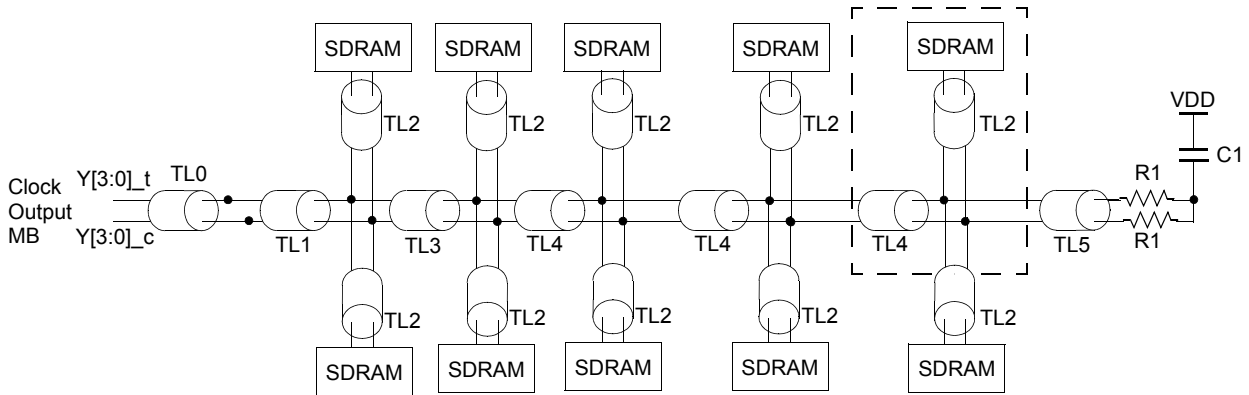
Trace Lengths for Unused Clock DIMM Termination Net Structures

R/C	Signal	TL0	R1 (Ω)	Notes
D0	CK1_t	4.0	120 ± 5%	1
D1	CK1_c	4.0		1
D2				

Note All distances are given in mm and must be kept within a tolerance of ± 0.8 mm.

Register Clock Output Net Structure

R/C D0 Net Structure Routing for Register Clock Output to SDRAM Loads



The left side (Y1, Y3) of the module includes all SDRAMs and transmission line segments.

The right side (Y0, Y2) of the module excludes the SDRAMs and the transmission line segments in the dotted box.

R/C D0 Trace Lengths for Register Clock Output to SDRAM load Net Structures

R/C	Signal	TL0	TL1	TL0 + TL1	TL2	TL3	TL4	TL5	R1 (Ω)	C1 (uF)	Notes
D0	Y[1,3]_t, Y[1,3]_c	0.4	15.6	16.0	2.9	18.3	13.0	7.2	36 ± 5%	0.01	1, 2
	Y[0,2]_t, Y[0,2]_c	0.4	15.6	16.0	2.9	18.3	13.0	7.2			1, 2

Note All distances are given in mm and must be kept within a tolerance of ± 0.8 mm