

Annex E - Raw Card E

DDR4 Load Reduced DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
E0	PC4-LRDIMM_V092_E0_20131205.brd	PC4-LRDIMM_V092_E0_20131207-BOM.txt
E1	PC4-LRDIMM_V200_E1_20141202.brd	PC4-LRDIMM_V200_E1_20150106-BOM.docx

Note 1 "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.

Module Configuration

SDRAM			DIMM					
Die Density	Die Organization	Pkg. Type	# of Pkg. Ranks ¹ per DIMM	# of SDRAM die per DIMM	Capacity per DIMM (GB)	DIMM Organization	# of Address bits row/col	MO-309 variation
2 Gb	512M x 4	DDP	4	72	16	2G x72	15/10	AAxA
4 Gb	1G x 4	DDP	4	72	32	4G x72	16/10	AAxA
8 Gb	2G x 4	DDP	4	72	64	8G x72	17/10	AAxA
12 Gb	3G x 4	DDP	4	72	96	12G x72	18/10	AAxA
16 Gb	4G x 4	DDP	4	72	128	16G x72	18/10	AAxA

Note 1 When populated with Dual Die Packages (DDP) logical ranks have no meaning.

SDRAM Configuration

Supported DRAM Outline (Width x Length) nom. (mm)	# of Banks in SDRAM BA/BG	SDRAM Package Type	Package Type	MO-207 variation
9.5 x 13.0	2/2	78 Ball FBGA	DDP	DW-z

Note 1 DDP refers to Dual Die Packages.

Supported Speeds

Raw Card	PC4-1333	PC4-1600	PC4-1866	PC4-2133	PC4-2400	PC4-2666	PC4-2933	PC4-3200	Notes
E0	X	X	X	X					1, 2
E1	P	P	P	P	P				1, 2

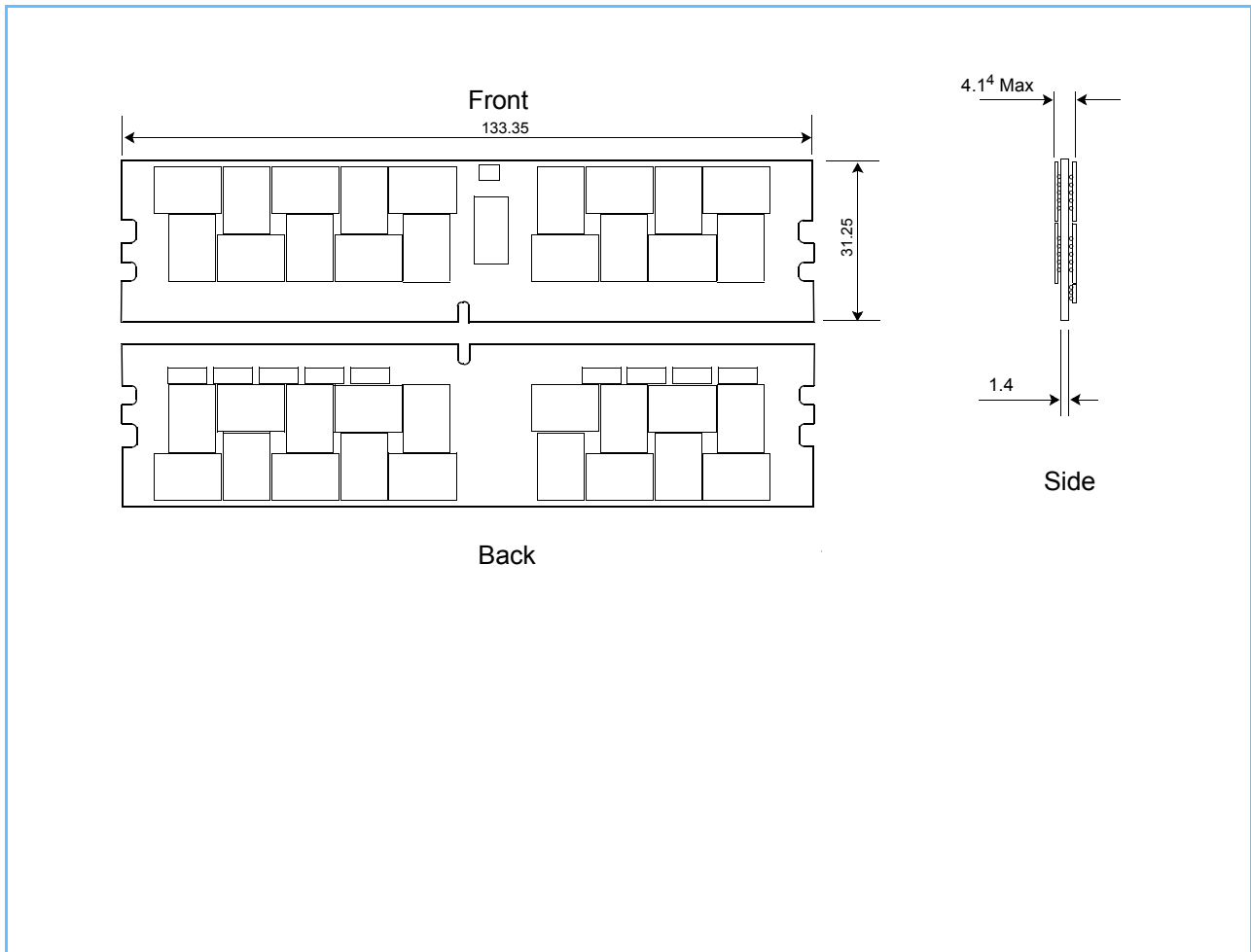
Note 1 X reflects speed grades approved from previous ballots.

Note 2 P denotes speed grades being proposed for this most recent ballot

Design Deviations

Note 1 R/C E1 requires the post register Clocks to be routed as 63 Ω differential pairs (0.15 mm trace with 0.1 mm space).

General Layout



Note 1 All dimensions are in mm.

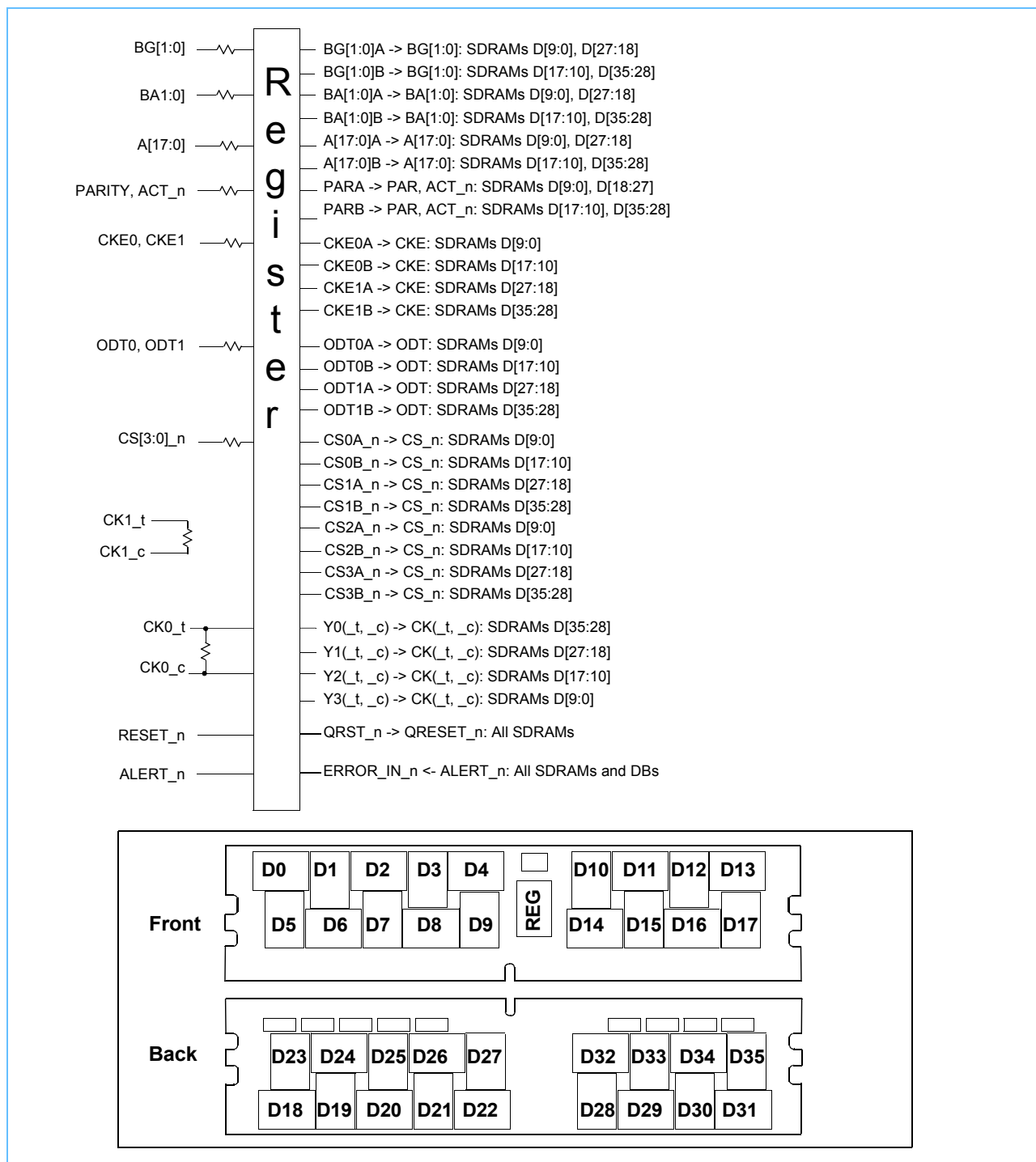
Note 2 Refer to MO-309 for more detailed information.

Note 3 Variation is AAxA (A-Module height, A-Module thickness, x-plating, A-DDR4 Key Position).

Note 4 Module thickness may vary with DRAM thickness. Variation A is valid for DRAMs less than or equal to 1.2 mm maximum.

Functional Block Diagram

x72 DIMM, populated as four package ranks of x4 DDR4 SDRAMs (Part 1 of 3)



Note 1 CK0_t, CK0_c terminated with $120\ \Omega \pm 5\%$ resistor.

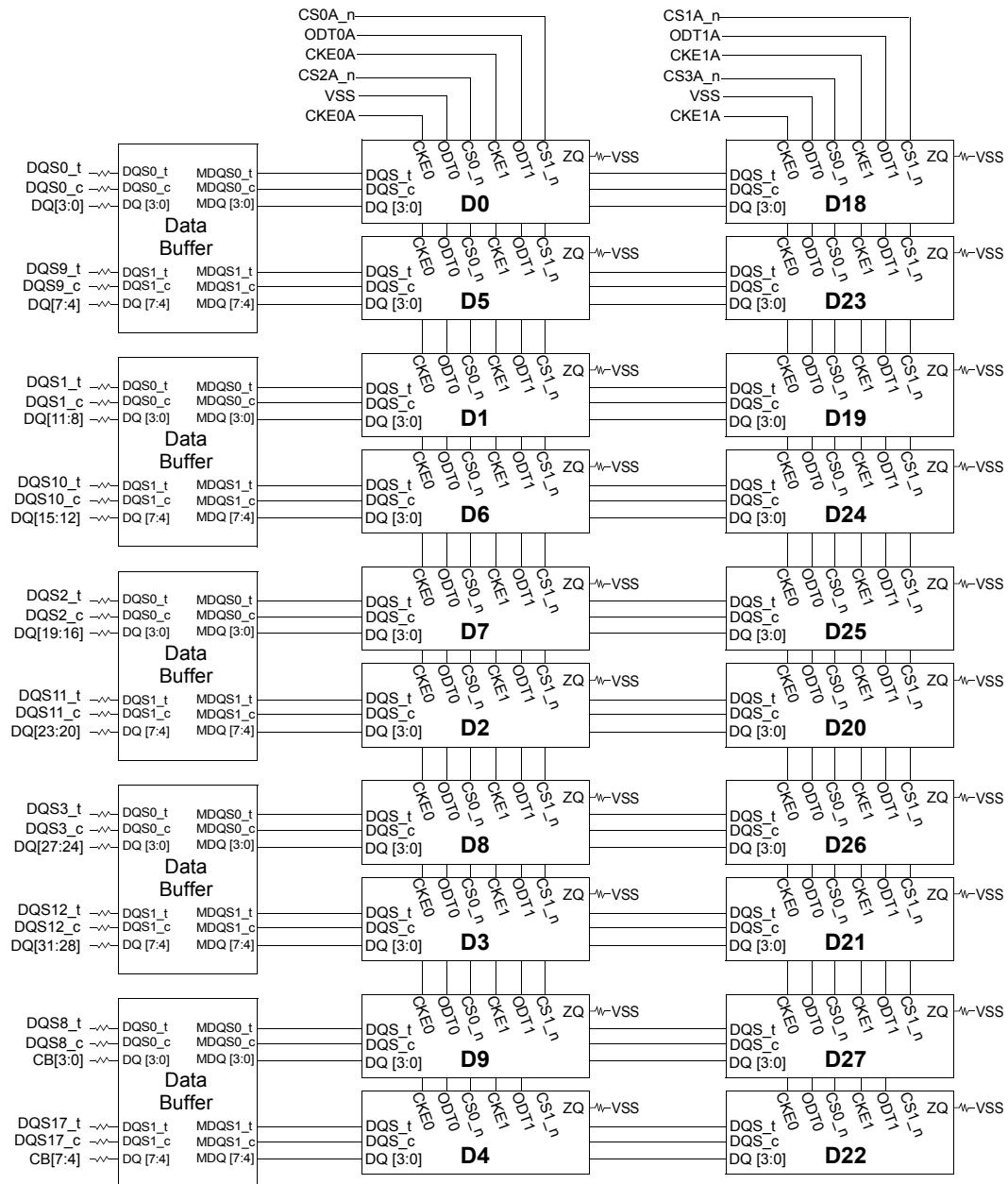
Note 2 CK1_t, CK1_c terminated with $120\ \Omega \pm 5\%$ resistor but not used.

Note 3 Unless otherwise noted resistors are $22\ \Omega \pm 5\%$.

Note 4 Register C2 input tied to GND.

Functional Block Diagram

x72 DIMM, populated as four package ranks of x4 DDR4 SDRAMs (Part 2 of 3)



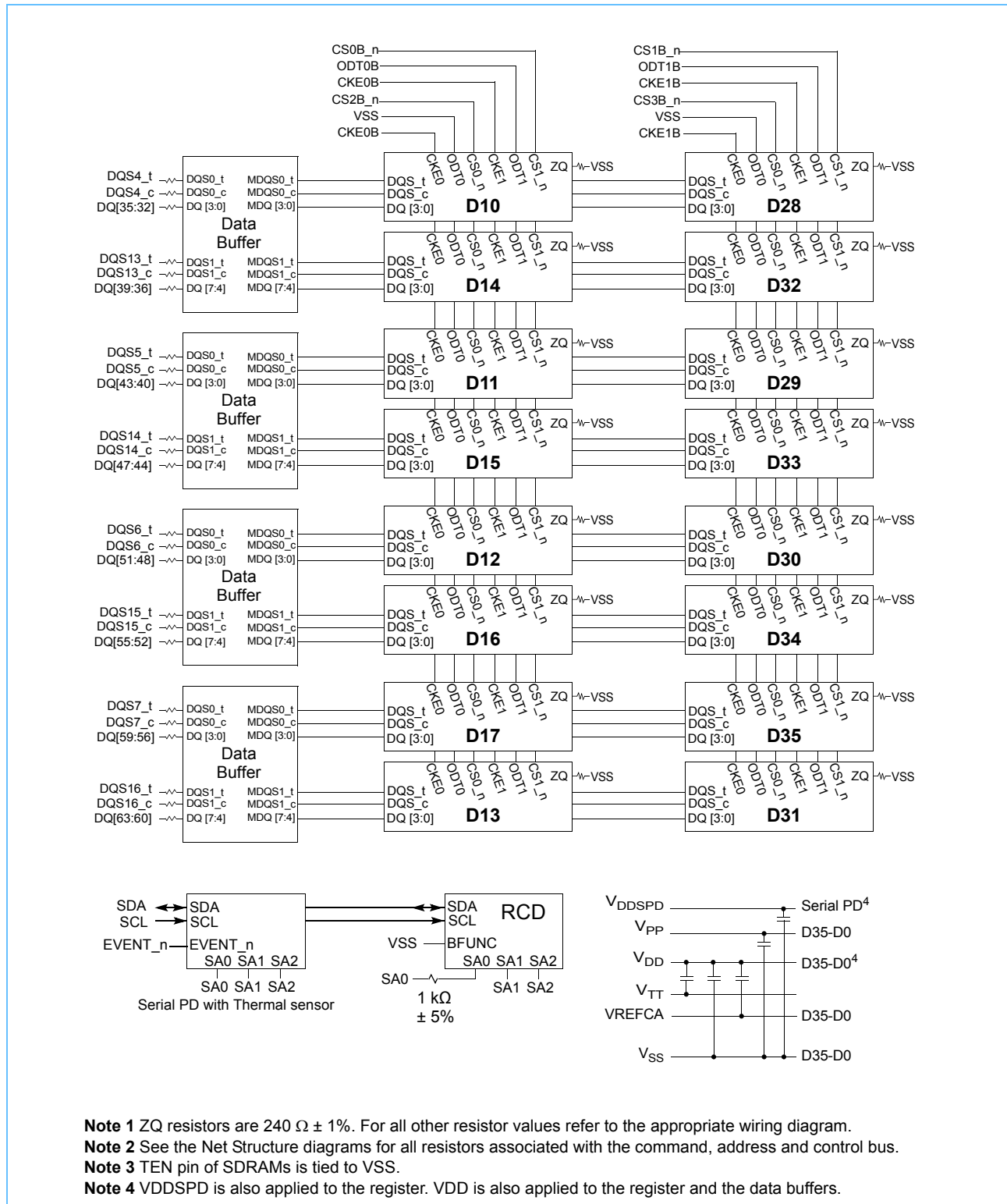
Note 1 ZQ resistors are $240 \Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.

Note 2 See the Net Structure diagrams for all resistors associated with the command, address and control bus.

Note 3 TEN pin of SDRAMs is tied to VSS.

Functional Block Diagram

x72 DIMM, populated as four package ranks of x4 DDR4 SDRAMs (Part 3 of 3)



Registered Clock Driver, Input Loading and Test Points

Refer to the DDR4RCDxx vendor data sheets for all technical specifications and requirements.
The DDR4RCDxx component will be referred to as the register throughout this document.

Loading

Signal Names	Connection to Device	Loads
CK0_t, CK0_c	Register	1
CK1_t, CK1_c ²	Termination Resistor Only	1 ²
RESET_n	Register	1
Ax, BAx, BGx, ACT_n, PARITY	Register	1 ¹
CS0_n, CS1_n, CS2_n, CS3_n, CKE0, CKE1, ODT0, ODT1	Register	1 ¹
DQ, CB, DQS_t, DQS_c	Data Buffer	1
SCL, SDA, SA[2:0]	SPD with Thermal Sensor, Register	2
EVENT_n	SPD with Thermal Sensor,	1
ALERT_n	Register	1
Note 1 Programmable resistive terminations are available on the Register. Note 2 Connected but not used.		

Test Point Locations

Signal Group	Signal Area	Signal locations
Address/Command/ Control/PARITY	Pre Register	22 Ω series resistor. Closer to the register provides better SI.
	Post Register	Termination resistors on the ends of the module.
DQ, CB	Pre Data Buffer	Front Side via for some DQ, CB.
MDQ, MCB	Post Data Buffer	No convenient test point
DQS_t, DQS_c	Pre Data Buffer	No convenient test point
MDQS_t, MDQS_c	Post Data Buffer	No convenient test point
Clock	Termination resistor	120 Ω termination resistor.
	Post Register	Termination resistors on the ends of the module.
Note 1 Refer to the registration package for additional test point information.		

Manufactured DIMM Improvement

Manufactured DIMMs may improve on the reference design as long as the skew is reduced relative to the reference design. It is a requirement that improvements not move the basic timing away from the reference design such that system integrity is jeopardized for systems defined to operate with the original reference design. The skew values reported in the tables only accounts for skew related to the DIMM PCB traces and vias of the reference design. No other error sources are included. The only exception is if the skew evaluation chose to use an actual SDRAM package or an idealized (uniform) package. This should be identified in a note below each table. The skew is only intended to document the design as a reference point if a manufacturer chooses to improve the design over the reference design. The skew is not a measurable value. Measured values of skew will always be greater than the values reported in the tables because other error sources will also be included.