

Annex B - Raw Card B

DDR4 Registered DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
B0	PC4-RDIMM_V081_RC_B0_20130731.brd	PC4-RDIMM_V081_RC_B0_20130731_bom.htm
B1	PC4-RDIMM_V200_RC_B1_20140801.brd	PC4-RDIMM_V200_RC_B1_20140926-BOM.docx
B2	PC4-RDIMM_RC_B2_R100_V300_20170120.brd ² PC4-RDIMM_RC_B2_R030_V250_20151007.brd	PC4-RDIMM_RC_B2_R100_V300_20170120-BOM.docx

Note 1 "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.

Note 2 This reference board file includes features to support a heat spreader. No other differences exist between the 2 board files. The BOM is valid for both.

Module Configuration

SDRAM					DIMM										
Die Density	Die Organization	Package Type	# of Logical Ranks ^{1,2} per Package Rank		# of Package Ranks ^{1,2} per DIMM	# of Logical Ranks per DIMM ³		# of SDRAM die per DIMM		Capacity per DIMM		Organization of DIMM		# of Address bits row/col	MO-309 variation
			Min.	Max.		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
2 Gb	512M x 4	SDP	-	-	2	2	-	36	-	8 GB	-	1G x72	-	15/10	AAxA
		3DS	2	8	2	-	16	-	288	-	64 GB	-	8G x72		
4 Gb	1G x 4	SDP	-	-	2	2	-	36	-	16 GB	-	2G x72	-	16/10	AAxA
		3DS	2	8	2	-	16	-	288	-	128 GB	-	16G x72		
8 Gb	2G x 4	SDP	-	-	2	2	-	36	-	32 GB	-	4G x72	-	17/10	AAxA
		3DS	2	8	2	-	16	-	288	-	256 GB	-	32G x72		
16 Gb	4G x 4	SDP	-	-	2	2	-	36	-	64 GB	-	8G x72	-	18/10	AAxA
		3DS	2	8	2	-	16	-	288	-	512 GB	-	64G x72		

Note 1 When populated with single die packages (SDP), package ranks per DIMM = 2.

Note 2 When populated with single load stack packages (3DS), logical ranks per package rank = 2-8. Logical ranks per package rank x package ranks per DIMM = 4-16

Note 3 DIMM capacity calculation purpose only because logical rank is not defined for non-3DS package

SDRAM Configuration

Raw Card	Supported DRAM Outline (Width x Length) nominal max.	# of Banks in SDRAM - BA/BG	SDRAM Package Type	Package Type	MO-207 variation
B0	9.5 x 13.0	2/2	78 Ball FBGA	SDP, 2H, 4H, 8H	DW-z
B1	9.0 x 13.0	2/2	78 Ball FBGA	SDP, 2H, 4H, 8H	DW-z
B2	8.0 x 12.0	2/2	78 Ball FBGA	SDP, 2H, 4H, 8H	DW-z

Note SDP is a Single Die per Package. 2H is 2 die stack, 4H is 4 die stack, 8H is 8 die stack. All these packages present a single load to the module.

Supported Speeds

Raw Card	PC4-1333	PC4-1600	PC4-1866	PC4-2133	PC4-2400	PC4-2666	PC4-2933	PC4-3200	Notes
B0	X	X	X	X					1, 2
B1	X	X	X	X	X				1, 2
B2	N	N	N	N	N	N			1, 2

Note 1 X reflects speed grades approved from previous ballots.

Note 2 N denotes new speed grades.

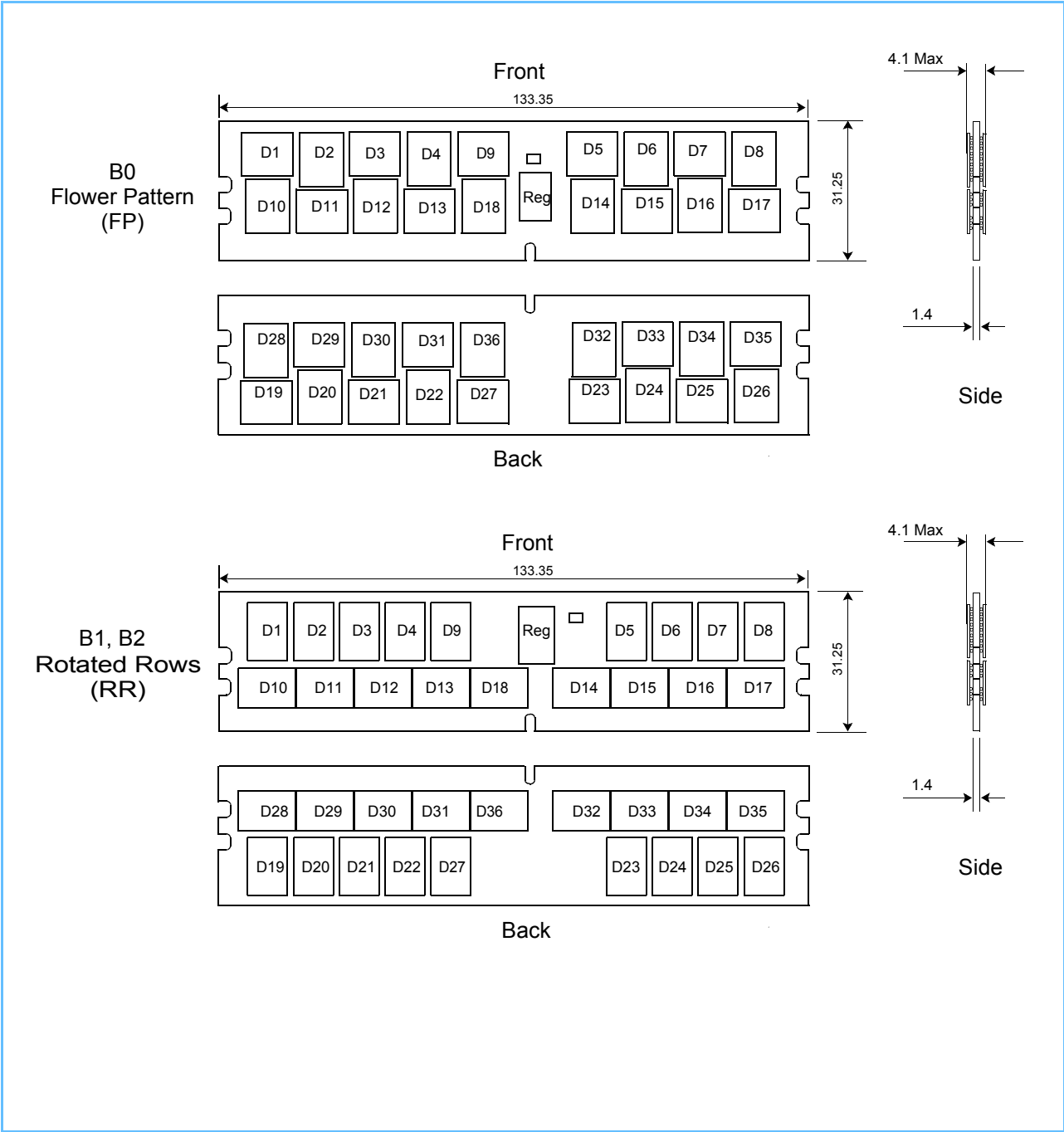
Design Deviations

Note 1 B0 - none.

Note 2 B1 - Stacked microvias are used. Microvias are used between layers 1-2, 2-3, 10-11 and 11-12.

Note 3 B2 - Uses 0.3 mm square pads for the 0201 discrete components. All vias are through vias.

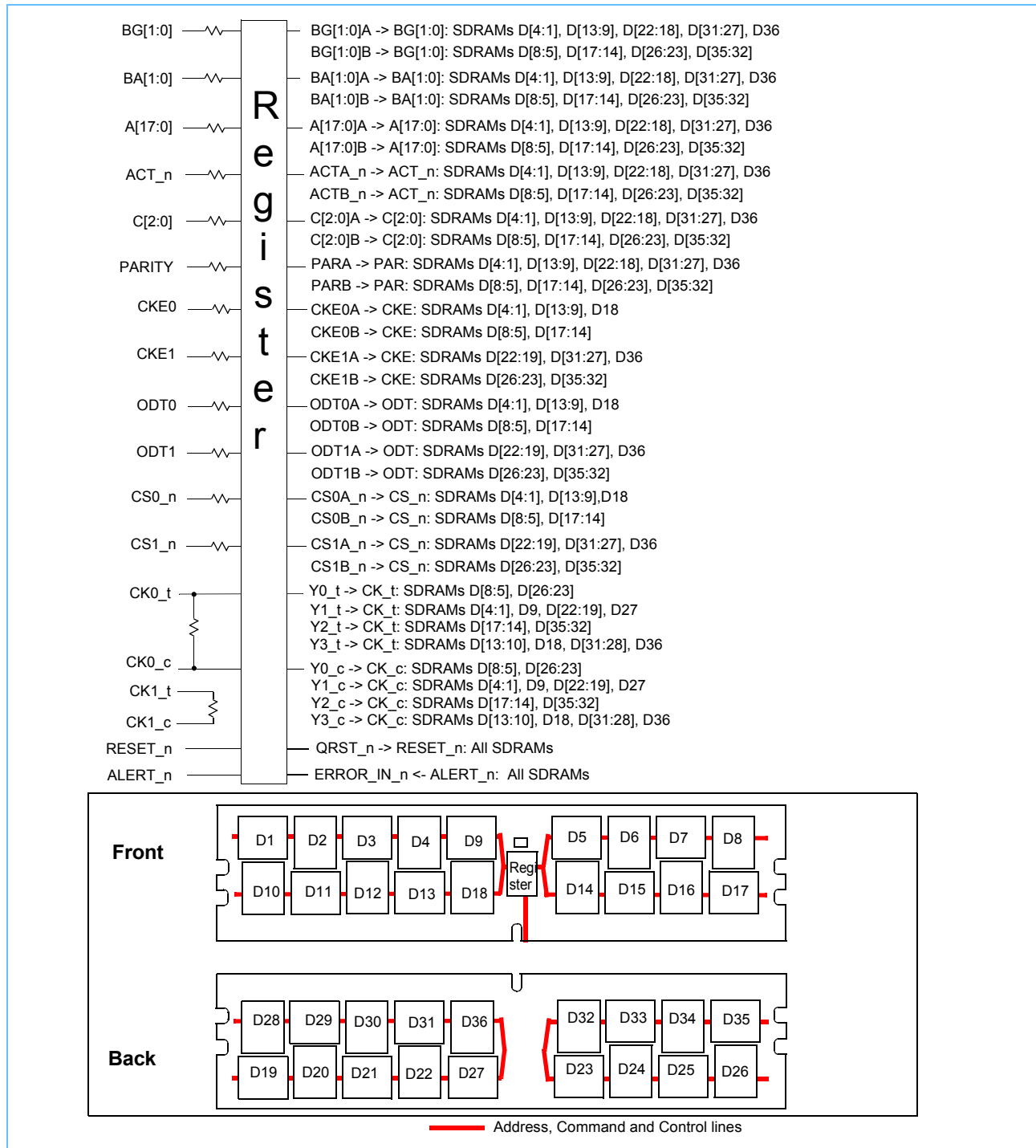
General Layout
General Layout



Note 1 Refer to MO-309 for more detailed information.
Note 2 Variation is AAxA (A Module height, A Module thickness, x plating, A Key Position).
Note 3 All dimensions are in mm.

Functional Block Diagram

R/C B0, B1 and B2 - x72 DIMM, two package ranks of x4 DDR4 SDRAMs (Part 1 of 5)



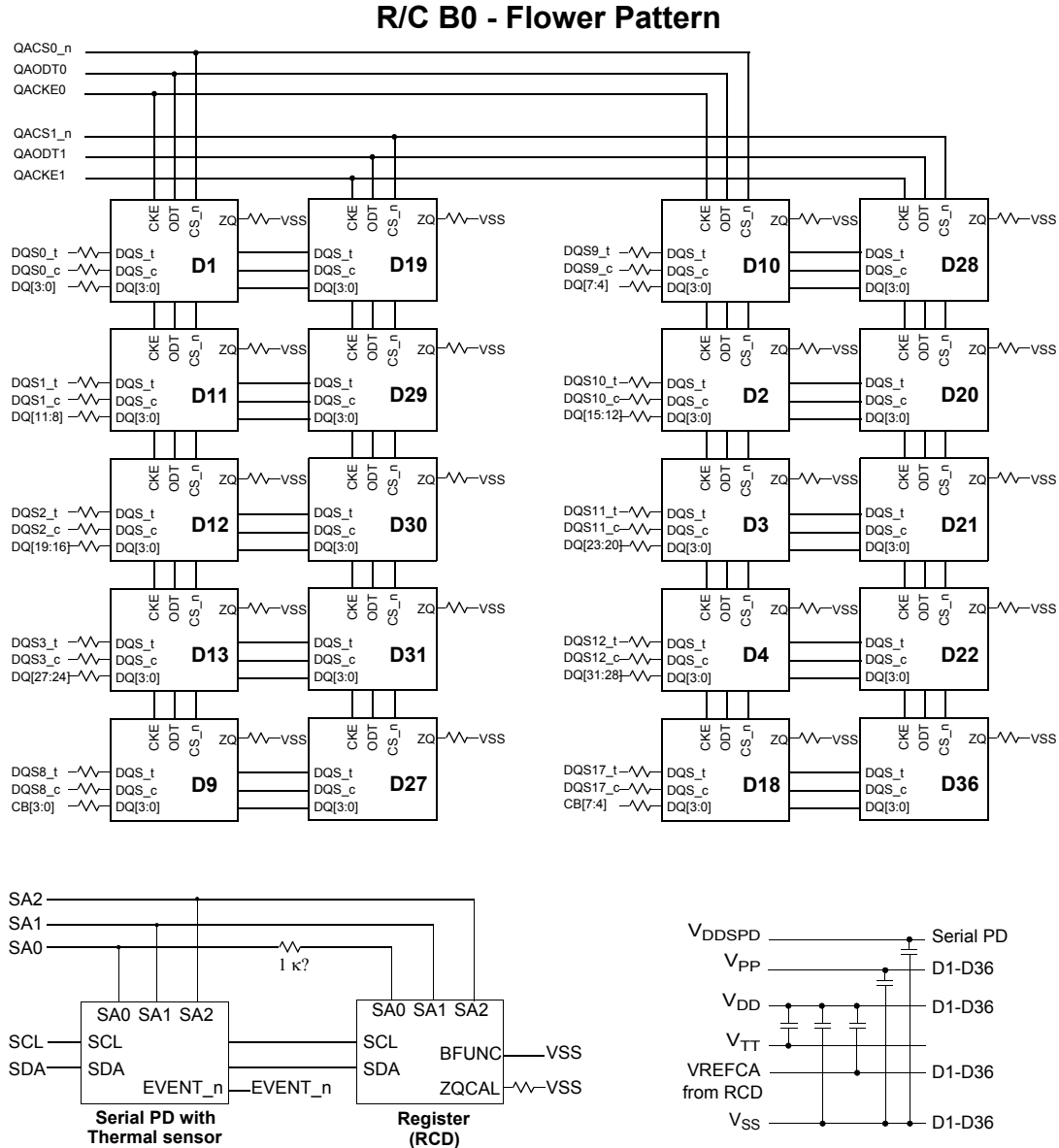
Note 1 CK0_t, CK0_c terminated with 120 $\Omega \pm 5\%$ resistor.

Note 2 CK1_t, CK1_c terminated with 120 $\Omega \pm 5\%$ resistor but not used.

Note 3 Unless otherwise noted resistors are 22 $\Omega \pm 5\%$.

Functional Block Diagram

R/C B0 - x72 DIMM, two package ranks of x4 DDR4 SDRAMs (Part 2 of 5)



Note 1 Unless otherwise noted, resistor values are $15\ \Omega \pm 5\%$.

Note 2 See the Net Structure diagrams for all resistors associated with the command, address and control bus.

Note 3 ZQ resistors are $240\ \Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.

Note 4 DRAM TEN pin must be tied to Vss.

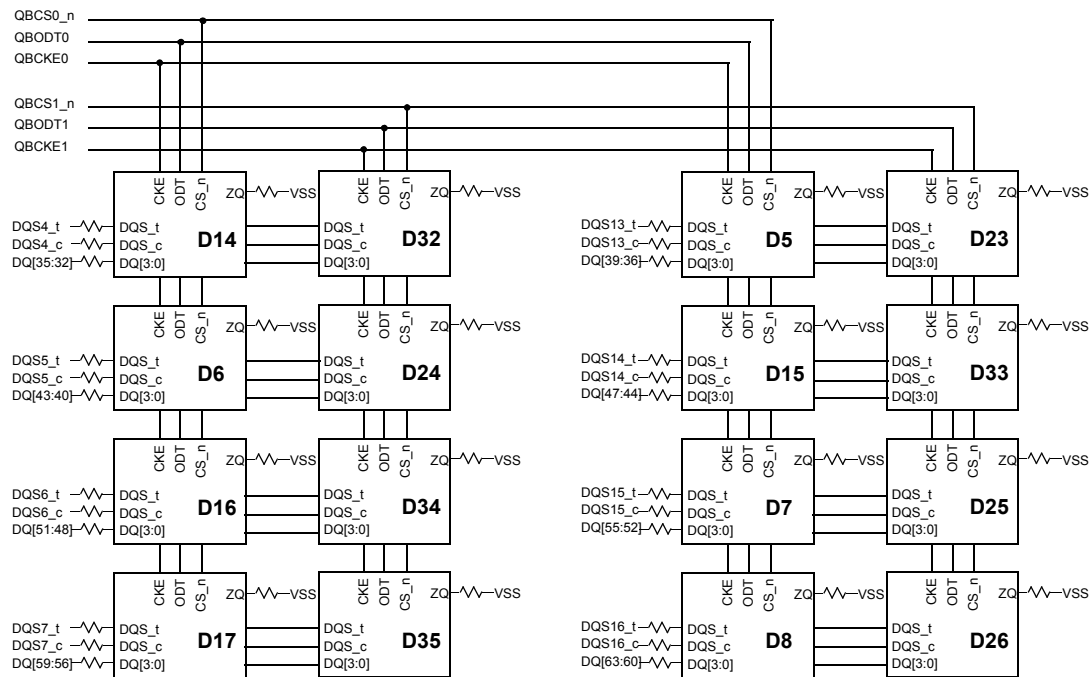
Note 5 VDDSPD also connects to the register (RCD).

Note 6 VREFCA from the edge connector only connects with the register (RCD). The RCD sources a separate VREFCA to all the SDRAMs.

Functional Block Diagram

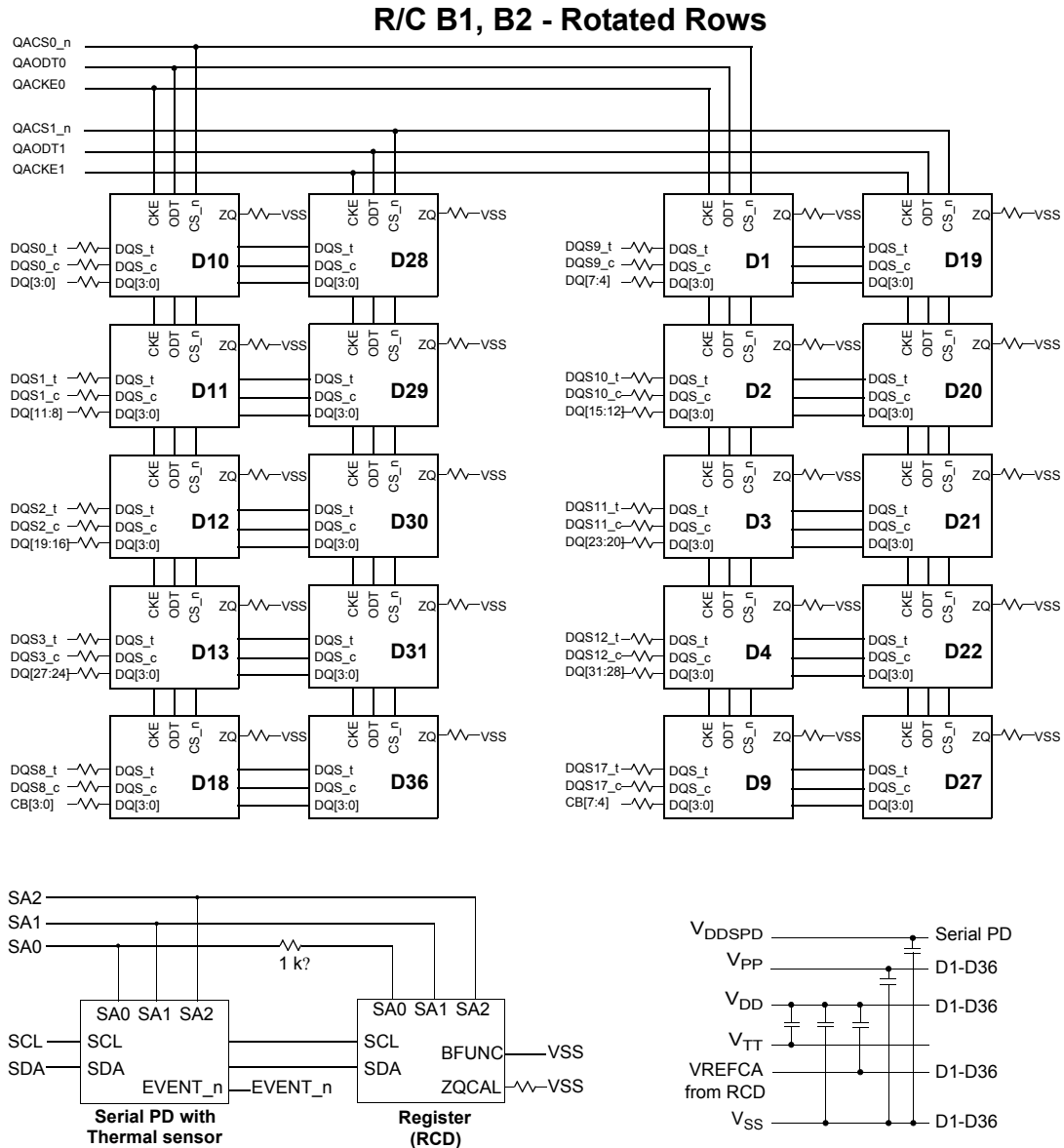
R/C B0 only - x72 DIMM, two package ranks of x4 DDR4 SDRAMs (Part 3 of 5)

R/C B0 - Flower Pattern



Functional Block Diagram

R/C B1, B2 - x72 DIMM, two package ranks of x4 DDR4 SDRAMs (Part 4 of 5)



Note 1 Unless otherwise noted, resistor values are $15\ \Omega \pm 5\%$.

Note 2 See the Net Structure diagrams for all resistors associated with the command, address and control bus.

Note 3 ZQ resistors are $240\ \Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.

Note 4 DRAM TEN must be tied to Vss.

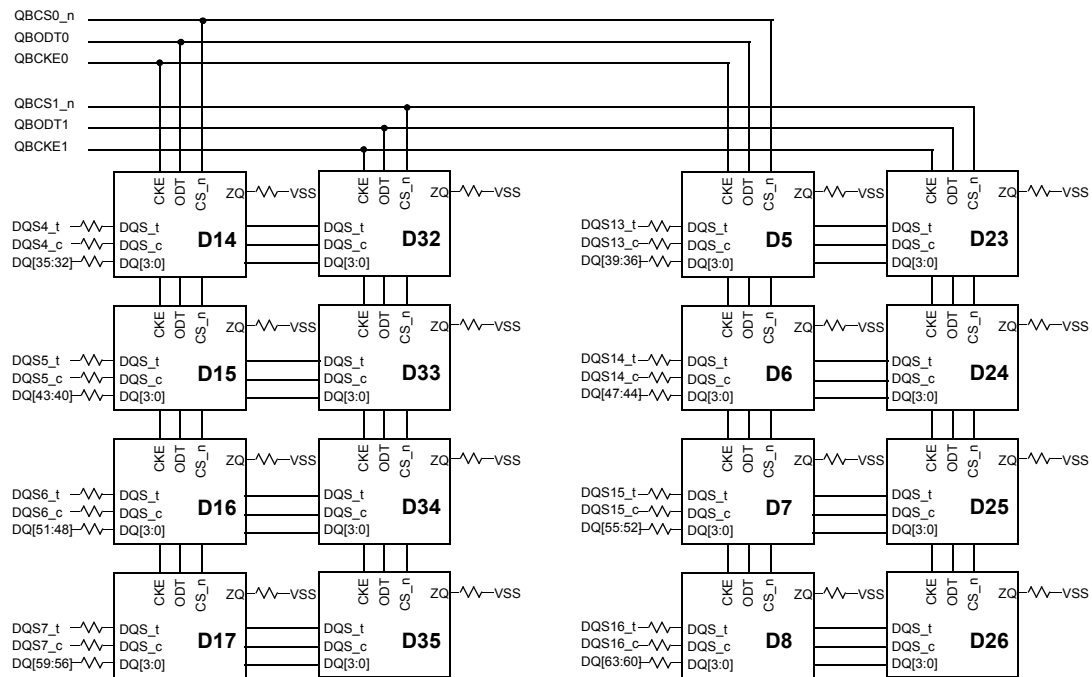
Note 5 VDDSPD also connects to the register (RCD).

Note 6 VREFCA from the edge connector only connects with the register (RCD). The RCD sources a separate VREFCA to all the SDRAMs.

Functional Block Diagram

R/C B1, B2 - x72 DIMM, two package ranks of x4 DDR4 SDRAMs (Part 5 of 5)

R/C B1, B2 - Rotated Rows



Registered Clock Driver, Input Loading and Test Points

Refer to the DDR4RCD0x vendor data sheets for all technical specifications and requirements.

The DDR4RCD0x component will be referred to as the register throughout this document.

Loading

Signal Names	Device	Loads
CK0_t, CK0_c	Input to Register	1
CK1_t, CK1_c ²	Termination Resistor Only	1 ²
RESET_n	Input to Register	1
CKE[1:0], ODT[1:0]	Input to Register	1 ¹
Ax, BAx, BGx, RAS_n, CAS_n, WE_n, PARITY, ACT_n	Input to Register	1 ¹
CS[1:0]_n, C[2:0]	Input to Register	1 ¹
DQ, CB, DQS_t, DQS_c	Input to SDRAM	2
SCL, SDA, SA[2:0]	I/O to SPD with Thermal Sensor, Register	2
EVENT_n	Output of SPD with Thermal Sensor	1
ALERT_n	Output of register	1
Note 1 Programmable resistive terminations are available on the Register.		
Note 2 Connected but not used.		

Test Point Locations

Signal Group	Signal	Signal locations
Address/Command/ Control/PARITY	Pre Register	22 Ω series resistor. Closer to the register provides better SI.
	Post Register	Termination resistors on the ends of the module.
DQ, CB	Series resistor	15 Ω resistors
DQS_t, DQS_c	Series resistor	15 Ω resistors
Clock	Termination resistor	120 Ω termination resistor.
	Post Register	Termination resistors on the ends of the module.
Note Refer to the registration package for additional test point information.		