

Annex C - Raw Card C

DDR4 Registered DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
C0	PC4-RDIMM_V080_RC_C0_20131107.brd	PC4-RDIMM_V080_RC_C0_20131107_BOM.xlsx
C1	PC4-RDIMM_V100_RC_C1_20150422.brd	PC4-RDIMM_V100_RC_C1_20150422_BOM.xlsx
C2	PC4-RDIMM_RC_C2_R050_V201_20160722.brd	PC4-RDIMM_RC_C2_R050_V201_20160722_BOM.html

Note "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.

Module Configuration

DIMM				SDRAM			# of SDRAM die		# of Logical Ranks per Package		# of Package Ranks per DIMM	# of Logical Ranks per DIMM		# of Address bits row/col	MO-309 variation
Maximum Capacity		Maximum Organization		Die Density	Maximum Organization		SDP	3DS ²	SDP	3DS ²	DIMM	SDP	3DS ²		
SDP	3DS ²	SDP	3DS ²		SDP	3DS ²									
4 GB	32 GB	512M x72	4G x72	2 Gb	512M x 4	4G x4	18	144	-	8	1	1	8	15/10 ¹	AAxA
8 GB	64 GB	1G x72	8G x72	4 Gb	1G x 4	8G x4	18	144	-	8	1	1	8	16/10 ¹	AAxA
16 GB	128 GB	2G x72	16G x72	8 Gb	2G x 4	16G x4	18	144	-	8	1	1	8	17/10	AAxA
32 GB	256 GB	4G x72	32G x72	16 Gb	4G x 4	32G x4	18	144	-	8	1	1	8	18/10	AAxA

Note 1 Address A16 is the highest address bit used based on it being multiplexed with RAS_n

Note 2 When populated with 3DS, Single load stack packages are available from 2 to 8 High. 3DS SDRAM package option supported by C1 and C2 but not supported by C0.

SDRAM Configuration

R/C	Supported DRAM Outline (Width x Length) Nom. (mm)	# of Banks in SDRAM BA/BG	SDRAM Package Type	Package Type	MO-207 variation
C0	11.0 x 13.0	2/2	78 Ball FBGA	SDP	DW-z
C1	9.0 x 13.0	2/2	78 Ball FBGA	SDP, 3DS	DW-z
C2	9.0 x 13.0	2/2	78 Ball FBGA	SDP, 3DS	DW-z

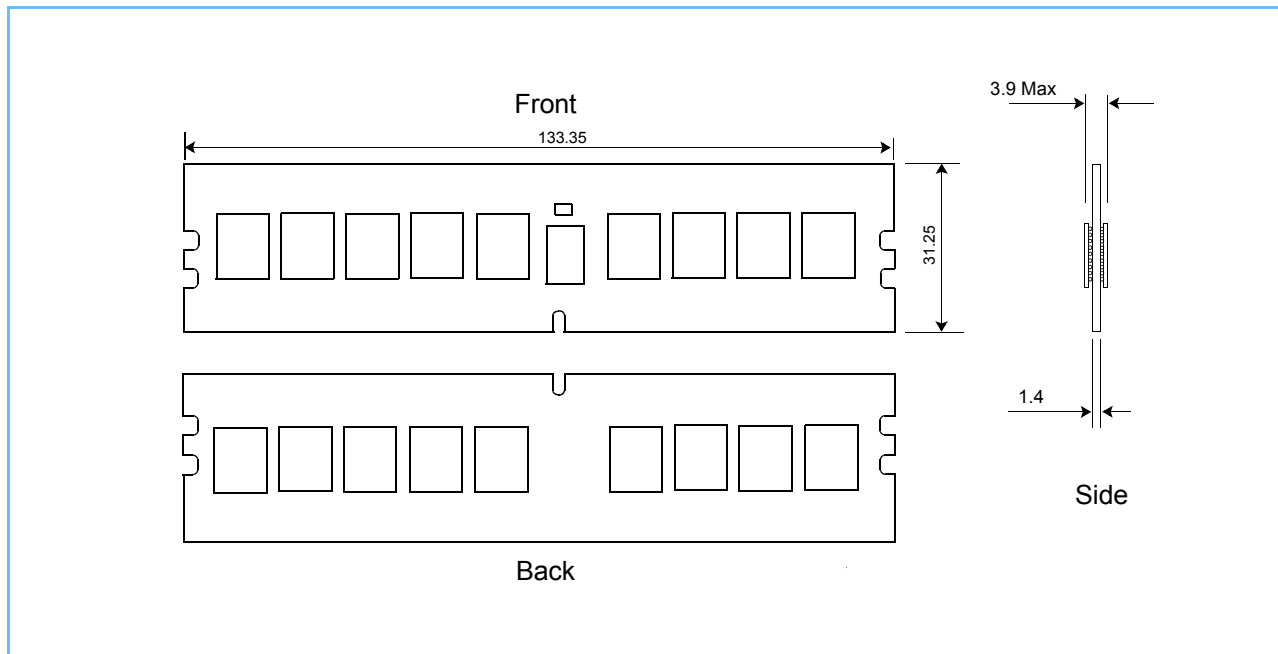
Note SDP is a Single Die per Package. 3DS are multi-die stacks using through silicon vias.

Supported Speeds

Raw Card	Speed	PC4-1333	PC4-1600	PC4-1866	PC4-2133	PC4-2400	PC4-2666	PC4-3200	Notes
C0	DDR4	X	X	X	X				1
C1	DDR4	X	X	X	X	X			1
C2	DDR4	N	N	N	N	N	N		1

Note 1 X reflects speed grades approved from previous ballots. N denotes speed grades being proposed for this most recent ballot

General Layout



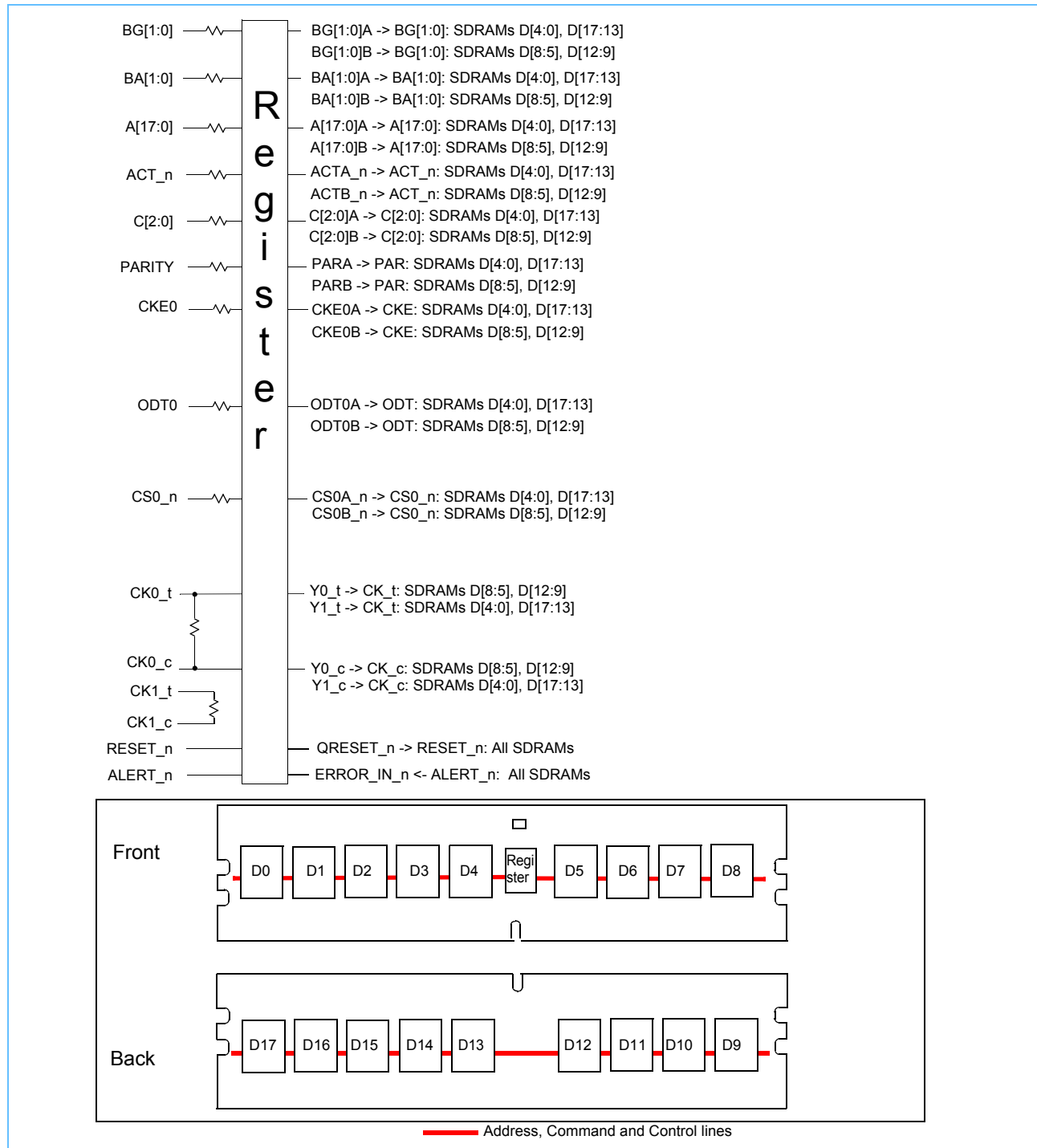
Note 1 Refer to MO-309 for more detailed information. All dimensions are in mm.

Note 2 Variation is AAxA (**A** Module height, **A** Module thickness, **x** plating, **A** Key Position).

Note 3 Module thickness may vary with DRAM thickness and passive components.

Functional Block Diagram

x72 DIMM, populated as one package rank of x4 DDR4 SDRAMs (Part 1 of 2)



Note 1 CK0_t, CK0_c terminated with $120\ \Omega \pm 5\%$ resistor.

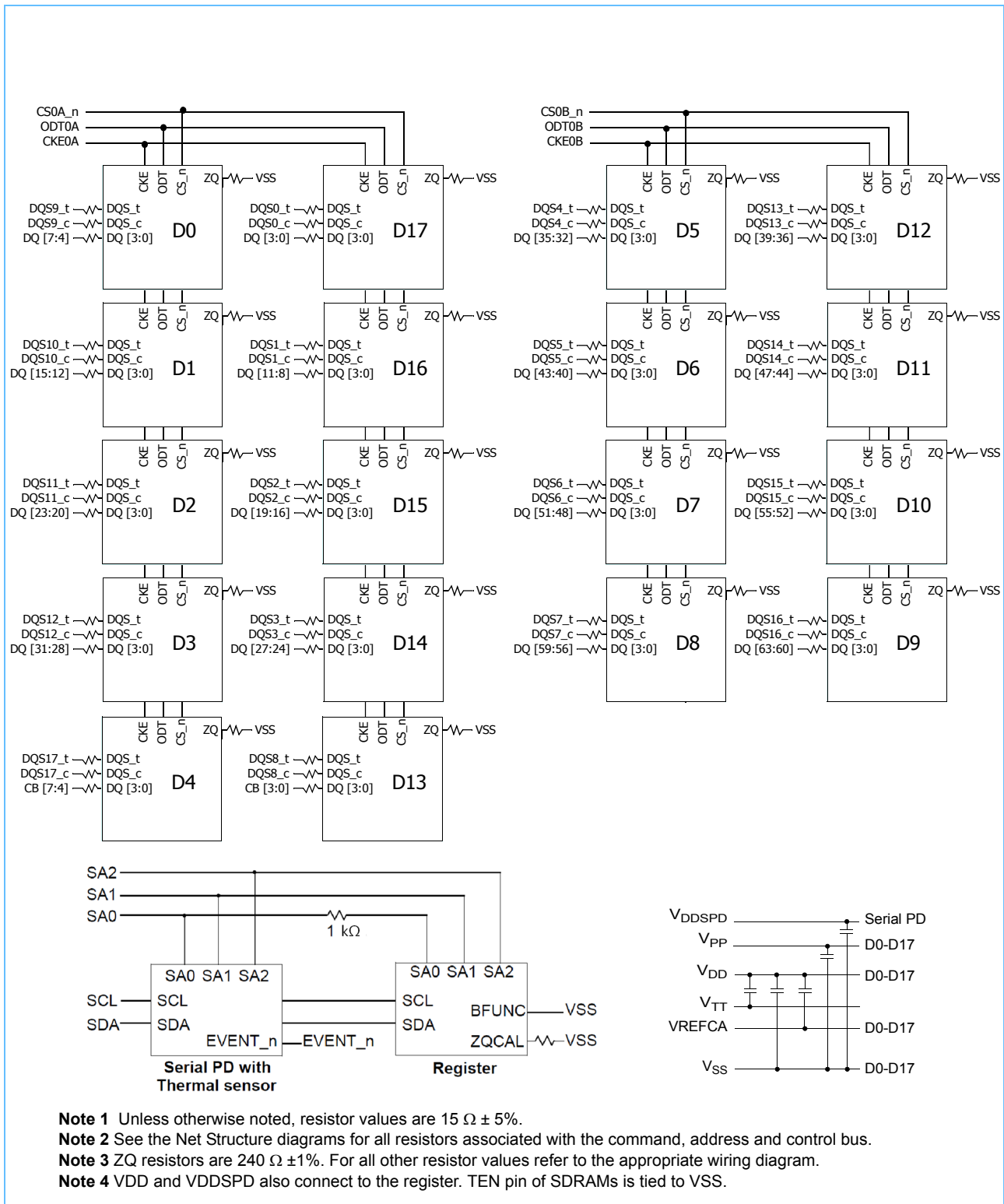
Note 2 CK1_t, CK1_c terminated with $120\ \Omega \pm 5\%$ resistor but not used.

Note 3 Unless otherwise noted, resistors are $22\ \Omega \pm 5\%$.

Note 4 Register input CS1_n is tied to VDD. Register inputs ODT1 and CKE1 are tied to VSS.

Functional Block Diagram

x72 DIMM, populated as one package rank of x4 DDR4 SDRAMs (Part 2 of 2)



Registered Clock Driver, Loading and Test Points

Refer to the DDR4RCDxx vendor data sheets for all technical specifications and requirements.
The DDR4RCDxx component will be referred to as the register throughout this document.

Loading

Signal Names	Input to Device	Loads
CK0_t, CK0_c	Register	1
CK1_t, CK1_c	Termination Resistor Only	1 ^a
RESET_n	Register	1
CKE[0], ODT[0]	Register	1 ^b
Ax, BAx, BGx, RAS_n, CAS_n, WE_n, PARITY, ACT_n	Register	1 ^b
CS[0]_n	Register	1 ^b
C[2:0]	Register	1 ^b
DQ, CB, DQS_t, DQS_c	SDRAM	1
SCL, SDA, SA[2:0]	SPD with Thermal Sensor, Register	1
EVENT_n	SPD with Thermal Sensor	1
ALERT_n	Register	1

a. Connected but not used.

b. Programmable resistive terminations are available on the Register.

Test Point Locations

Signal Group	Signal	Signal locations
Address/Command/ Control/PARITY	Pre Register	22 Ω series resistor. Closer to the register provides better SI.
	Post Register	Termination resistors on the ends of the module.
DQ,CB	Series resistor	15 Ω resistors
DQS_t, DQS_c	Series resistor	15 Ω resistors
Clock	Termination resistor	120 Ω termination resistor.
	Post Register	Termination resistors on the ends of the module.
Note 1 Refer to the registration package for additional test point information.		

DQ Map for CRC

See Common section of the DDR4 RDIMM Design Specification for information on interpreting the DQ Mapping table.

SPD Values for DQ Mapping

DQ Bits as defined by connector	SPD Byte	SPD Value (Hex)			DQ Bits as defined by connector	SPD Byte	SPD Value (Hex)		
R/C		C0	C1	C2	R/C		C0	C1	C2
DQ0, DQ1, DQ2, DQ3	60	15	15	16	DQ32, DQ33, DQ34, DQ35	70	15	15	16
DQ4, DQ5, DQ6, DQ7	61	0D	0D	03	DQ36, DQ37, DQ38, DQ39	71	0D	0D	03
DQ8, DQ9, DQ10, DQ11	62	15	15	16	DQ40, DQ41, DQ42, DQ43	72	15	15	16
DQ12, DQ13, DQ14, DQ15	63	0D	0D	03	DQ44, DQ45, DQ46, DQ47	73	0D	0D	03
DQ16, DQ17, DQ18, DQ19	64	15	15	16	DQ48, DQ49, DQ50, DQ51	74	15	15	16
DQ20, DQ21, DQ22, DQ23	65	0D	0D	03	DQ52, DQ53, DQ54, DQ55	75	0D	0D	03
DQ24, DQ25, DQ26, DQ27	66	15	15	16	DQ56, DQ57, DQ58, DQ59	76	15	15	16
DQ28, DQ29, DQ30, DQ31	67	0D	0D	03	DQ60, DQ61, DQ62, DQ63	77	0D	0D	03
CB0, CB1, CB2, CB3	68	15	15	16					
CB4, CB5, CB6, CB7	69	0D	0D	03					

Manufactured DIMM Improvement

Manufactured DIMMs may improve on the reference design as long as the skew is reduced relative to the reference design. It is a requirement that improvements not move the basic timing away from the reference design such that system integrity is jeopardized for systems defined to operate with the original reference design. The skew values reported in the tables only accounts for skew related to the DIMM PCB traces and vias of the reference design. No other error sources are included. The only exception is if the skew evaluation chose to use an actual SDRAM package or an idealized (uniform) package. This should be identified in a note below each table. The skew is only intended to document the design as a reference point if a manufacturer chooses to improve the design over the reference design. The skew is not a measurable value. Measured values of skew will always be greater than the values reported in the tables because other error sources will also be included.