

Annex F - Raw Card F

DDR4 Registered DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
F0	PC4-RDIMM_V090_RC_F0_20131106.zip	PC4-RDIMM_V090_RC_F0_20131106-BOM.xlsx

Note "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.

Module Configuration

Die Density	Die Organization	Pkg. Type	Logical Ranks per DIMM		Pkg. Ranks per DIMM	SDRAM die per DIMM		Capacity per DIMM (GB)		DIMM Organization		Address bits row/col	MO-309 variation
			Min.	Max.		Min.	Max.	Min.	Max.	Min.	Max.		
2Gbit	512M x 4	SDP	-	-	1	18	18	4	4	512Mx72	512Mx72	15/10	BAxA
		3DS	2	8	1	36	144	8	32	1Gx72	4Gx72		
4Gbit	1G x 4	SDP	-	-	1	18	18	8	8	1Gx72	1Gx72	16/10	BAxA
		3DS	2	8	1	36	144	16	64	2Gx72	8Gx72		
8Gbit	2G x 4	SDP	-	-	1	18	18	16	16	2Gx72	2Gx72	17/10	BAxA
		3DS	2	8	1	36	144	32	128	4Gx72	16Gx72		
16Gbit	4G x 4	SDP	-	-	1	18	18	32	32	4Gx72	4Gx72	18/10	BAxA
		3DS	2	8	1	36	144	64	256	8Gx72	32Gx72		

SDRAM Configuration

Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM BA/BG	SDRAM Package Type	Package Type	MO-207 variation
10.0 x 13.0	2/2	78 Ball FBGA	SDP, 3DS	DW-z

Note SDP is a single die per package. 3DS is a stacked die package presenting a single load.

Supported Speeds

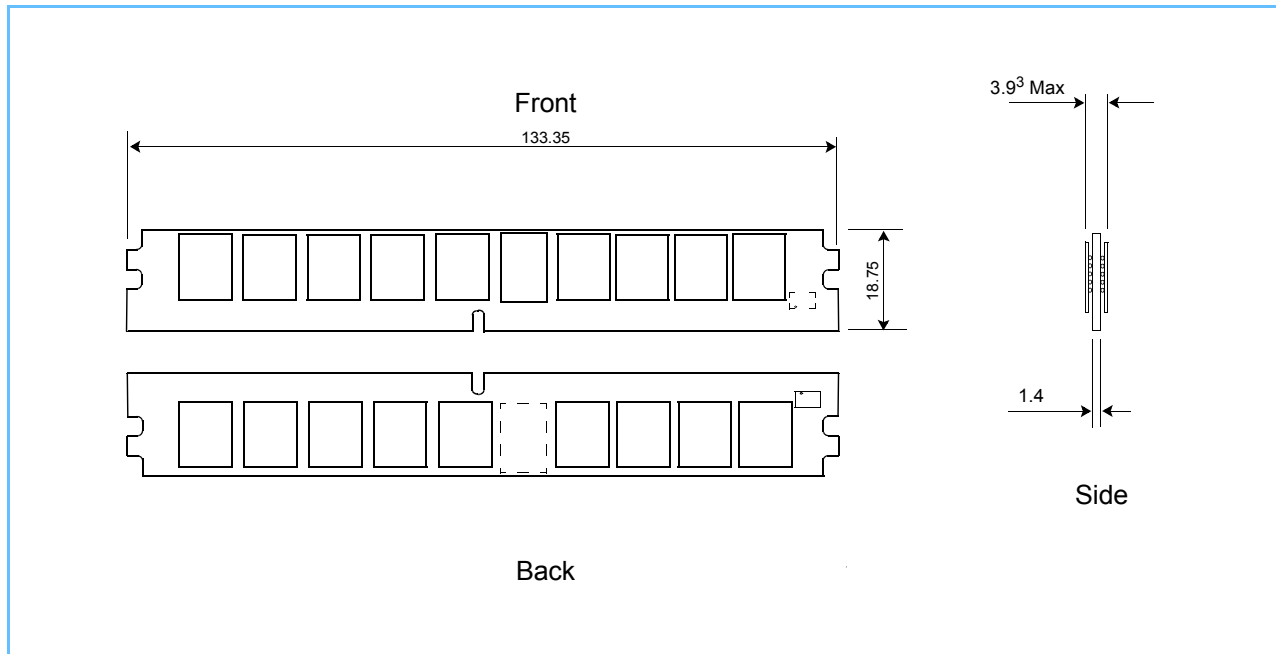
Raw Card	Speed	PC4-1333	PC4-1600	PC4-1866	PC4-2133	PC4-2400	PC4-2666	PC4-3200	Notes
F0	DDR4	P	P	P	P				1, 2
F0	DDR4L								1, 2

Note 1 X reflects speed grades approved from previous ballots.
Note 2 P denotes speed grades being proposed for this most recent ballot

Design Deviations

Note This design uses micro-via technology.
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General Layout



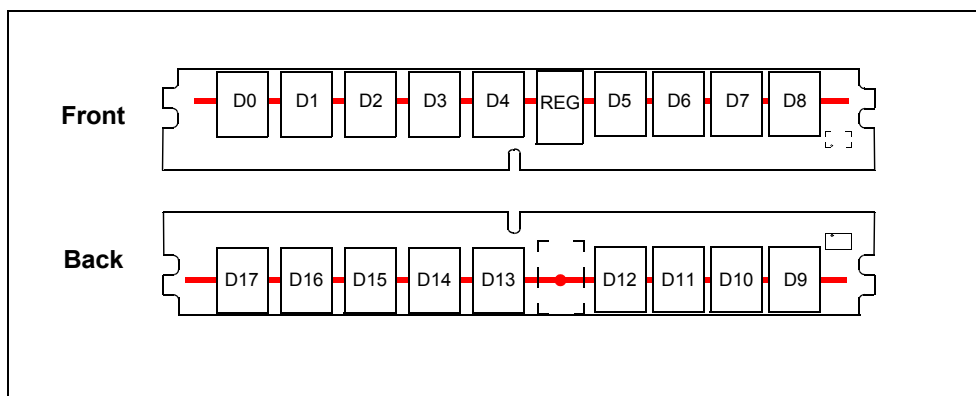
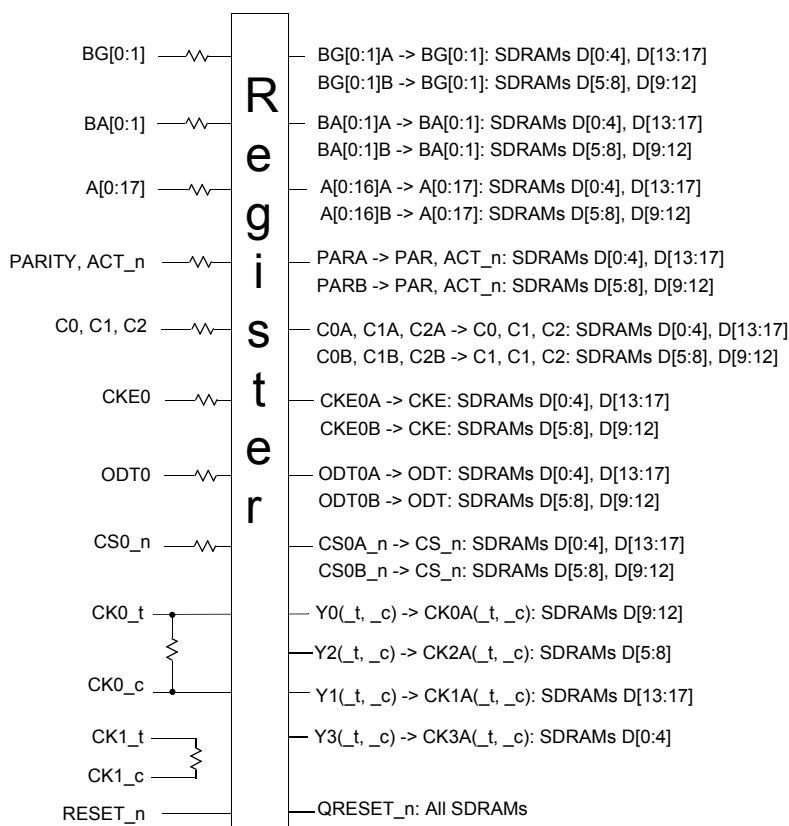
Note 1 Refer to MO-309 for more detailed information.

Note 2 Variation is BAxA (B-Module height, A-Module thickness, x-plating, A-DDR4 Key Position).

Note 3 Module thickness varies with DRAM thickness. Variation A is valid for DRAMs less than or equal to 1.2 mm maximum and there is not a heat spreader attached.

Functional Block Diagram

x72 DIMM, populated as one package rank of x4 DDR4 SDRAMs (Part 1 of 2)



Address, Command and Control lines

Note 1 CK0_t, CK0_c terminated with $120\Omega \pm 5\%$ resistor.

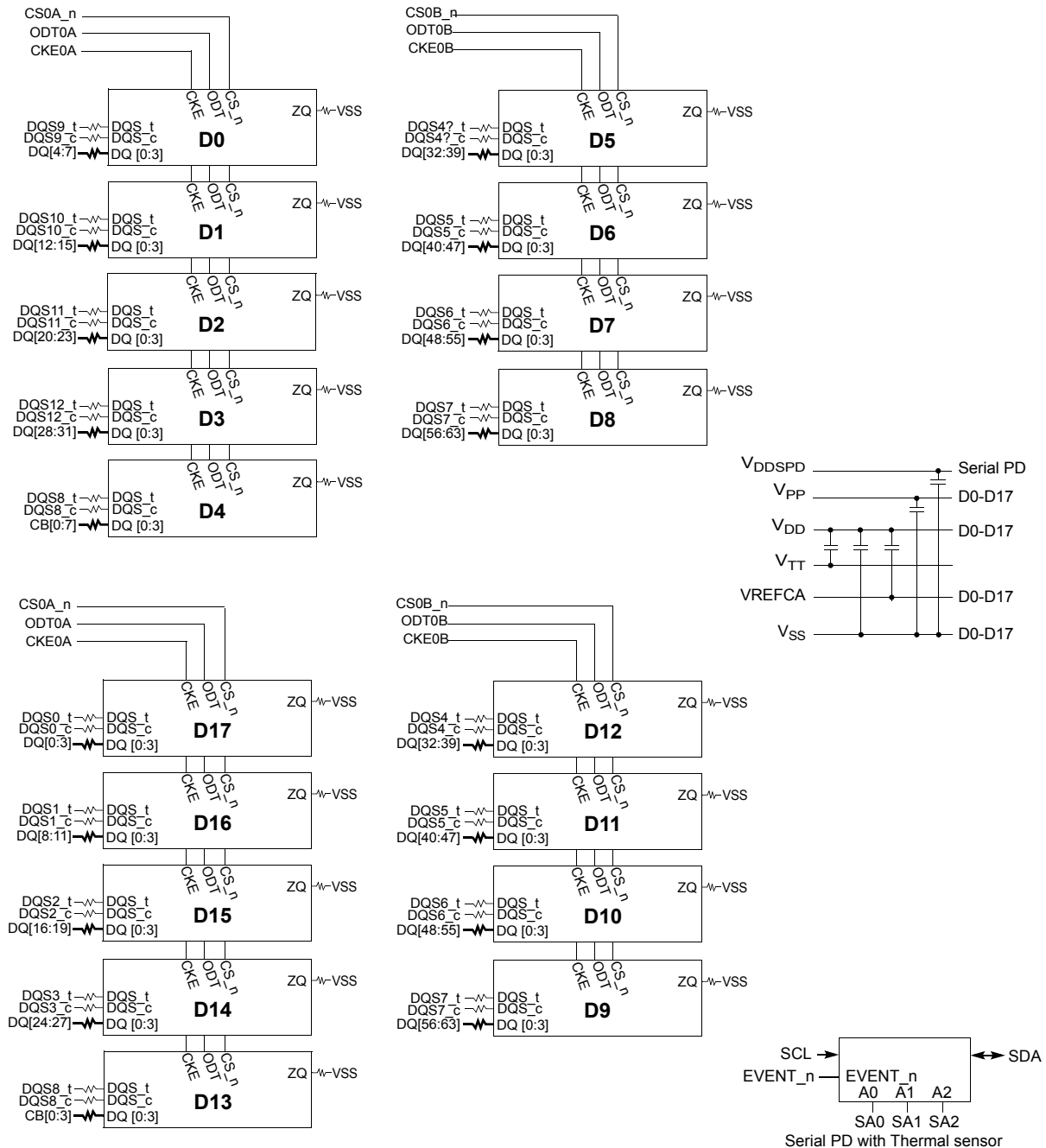
Note 2 CK1_t, CK1_c terminated with $120\Omega \pm 5\%$ resistor but not used.

Note 3 Unless otherwise noted resistors are $22\Omega \pm 5\%$.

Note 4 Register input CS1_n is tied to VDD. Register inputs BFUNC, ODT1 and CKE1 are tied to VSS.

Functional Block Diagram

x72 DIMM, populated as one package rank of x4 DDR4 SDRAMs (Part 2 of 2)



Note 1 Unless otherwise noted, resistor values are $15\Omega \pm 5\%$.

Note 2 See the Net Structure diagrams for all resistors associated with the command, address and control bus.

Note 3 ZQ resistors are $240\Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.

Registered Clock Driver, Input Loading and Test Points

Refer to the DDR4RCD01 vendor data sheets for all technical specifications and requirements.
The DDR4RCD01 component will be referred to as the register throughout this document.

Loading

Signal Names	Input to Device	Loads
CK0_t, CK0_c	Register	1
CK1_t, CK1_c ²	Termination Resistor Only	1 ²
RESET_n	Register	1
CKE0, ODT0	Register	1 ¹
Ax, BAx, BGx, ACT_n, PARITY	Register	1 ¹
C0, C1, C2	Register	1
CS0_n	Register	1 ¹
DQ, CB, DQS_t, DQS_c	SDRAM	1
SCL, SDA, SA[2:0]	SPD with Thermal Sensor, Register	2
EVENT_n	Output of SPD with Thermal Sensor	1
ALERT_n	Output of Register	1

Note 1 Programmable resistive terminations are available on the Register.
Note 2 Connected but not used.

Test Point Locations

Signal Group	Signal Area	Signal locations
Address/Command/ Control/parity	Pre Register	22 Ohm series resistor. Closer to the register provides better SI.
	Post Register	Termination resistors on the ends of the module.
Die Select (C0, C1, C2)	Pre Register	22 Ohm series resistor. Closer to the register provides better SI.
	Post Register	Termination resistors on the ends of the module.
DQ,CB	Series resistor	15 Ohm resistors
DQS_t, DQS_c	Series resistor	15 Ohm resistors
Clock	Termination resistor	120 Ohm termination resistor.
	Post Register	Termination resistors on the ends of the module.

Note Refer to the registration package for additional test point information.

Manufactured DIMM Improvement

Manufactured DIMMs may improve on the reference design as long as the skew is reduced relative to the reference design. It is a requirement that improvements not move the basic timing away from the reference design such that system integrity is jeopardized for systems defined to operate with the original reference design. The skew values reported in the tables only accounts for skew related to the DIMM PCB traces and vias of the reference design. No other error sources are included. The only exception is if the skew evaluation chose to use an actual SDRAM package or an idealized (uniform) package. This should be identified in a note below each table. The skew is only intended to document the design as a reference point if a manufacturer chooses to improve the design over the reference design. The skew is not a measurable value. Measured values of skew will always be greater than the values reported in the tables because other error sources will also be included.