

Annex G - Raw Card G

DDR4 Registered DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
G0	PC4-RDIMM_V080_RC_G0_20130408.brd	PC4-RDIMM_V080_RC_G0_20130408_bom.htm

Note 1 "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.

Module Configuration

SDRAM			DIMM					
Die Density	Die Organization	Package Type	# of Package Ranks per DIMM	# of SDRAM die per DIMM	Capacity per DIMM	Organization of DIMM	# of Address bits row/col	MO-309 variation
2 Gb	256 M x 8	SDP	1	9	2 GB	256 M x72	14/10	BAxA
4 Gb	512 M x 8	SDP	1	9	4 GB	512 M x72	15/10	BAxA
8 Gb	1 G x 8	SDP	1	9	8 GB	1 G x72	16/10	BAxA
16 Gb	2 G x 8	SDP	1	9	16 GB	2 G x72	17/10	BAxA

SDRAM Configuration

Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM BA/BG	SDRAM Package Type	Package Type	MO-207 variation
11.0 mm x 13.0 mm	2/2	78 Ball FBGA	SDP	DT-z

Note 1 SDP is a single die per package.

Supported Speeds

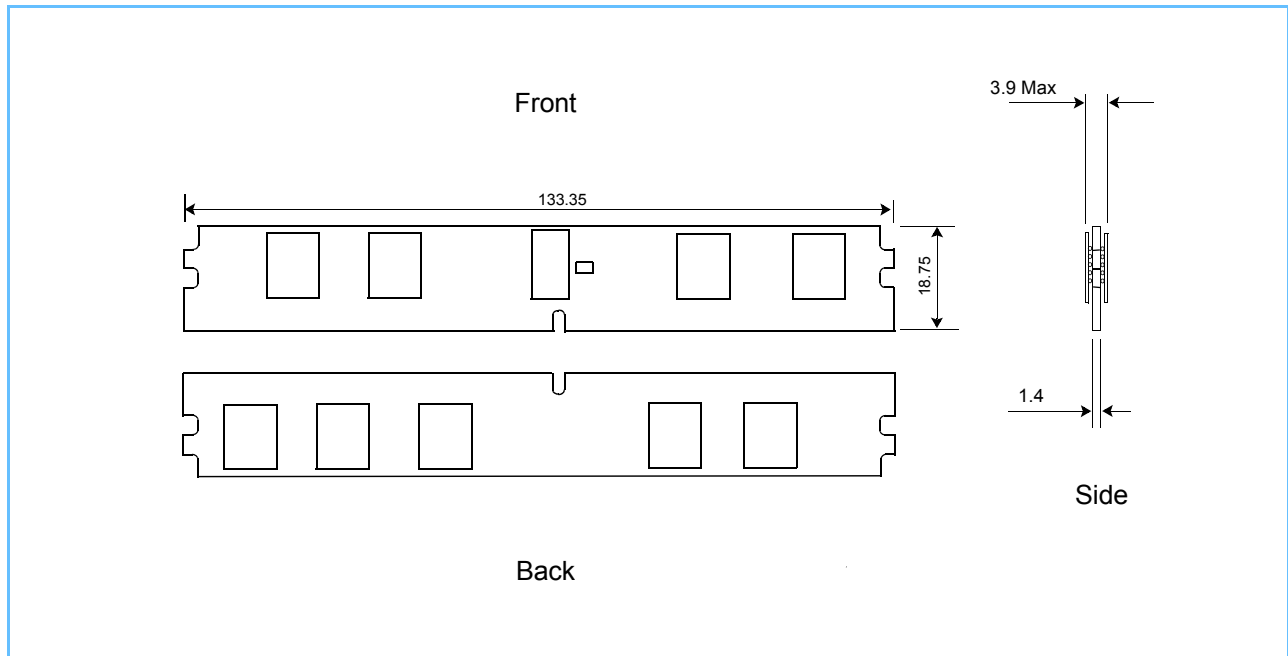
Raw Card	PC4-1333	PC4-1600	PC4-1866	PC4-2133	PC4-2400	PC4-2666	PC4-3200	Notes
G0	X	X	X	X	P			1, 2

Note 1 X reflects speed grades approved from previous ballots.
Note 2 P denotes speed grades being proposed for this most recent ballot

Design Deviations

Note 1 None.

General Layout

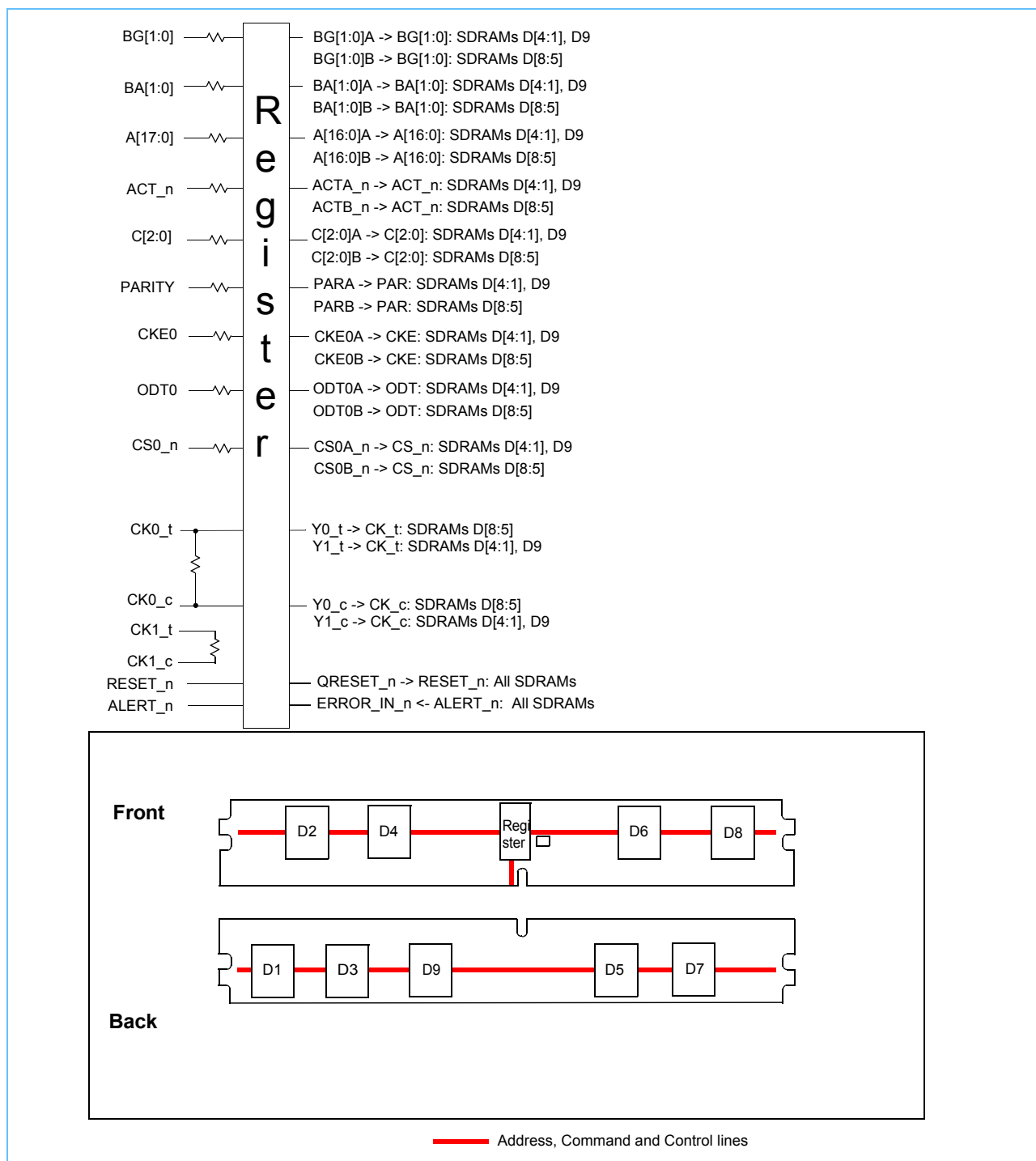


Note 1 Refer to MO-309 for more detailed information (mm).

Note 2 Variation is BAxA (B Module height, A Module thickness, x plating, A DDR4 Key Position).

Functional Block Diagram

x72 DIMM, populated as one package rank of x8 DDR4 SDRAMs (Part 1 of 2)



Note 1 CK0_t, CK0_c terminated with 120 $\Omega \pm 5\%$ resistor.

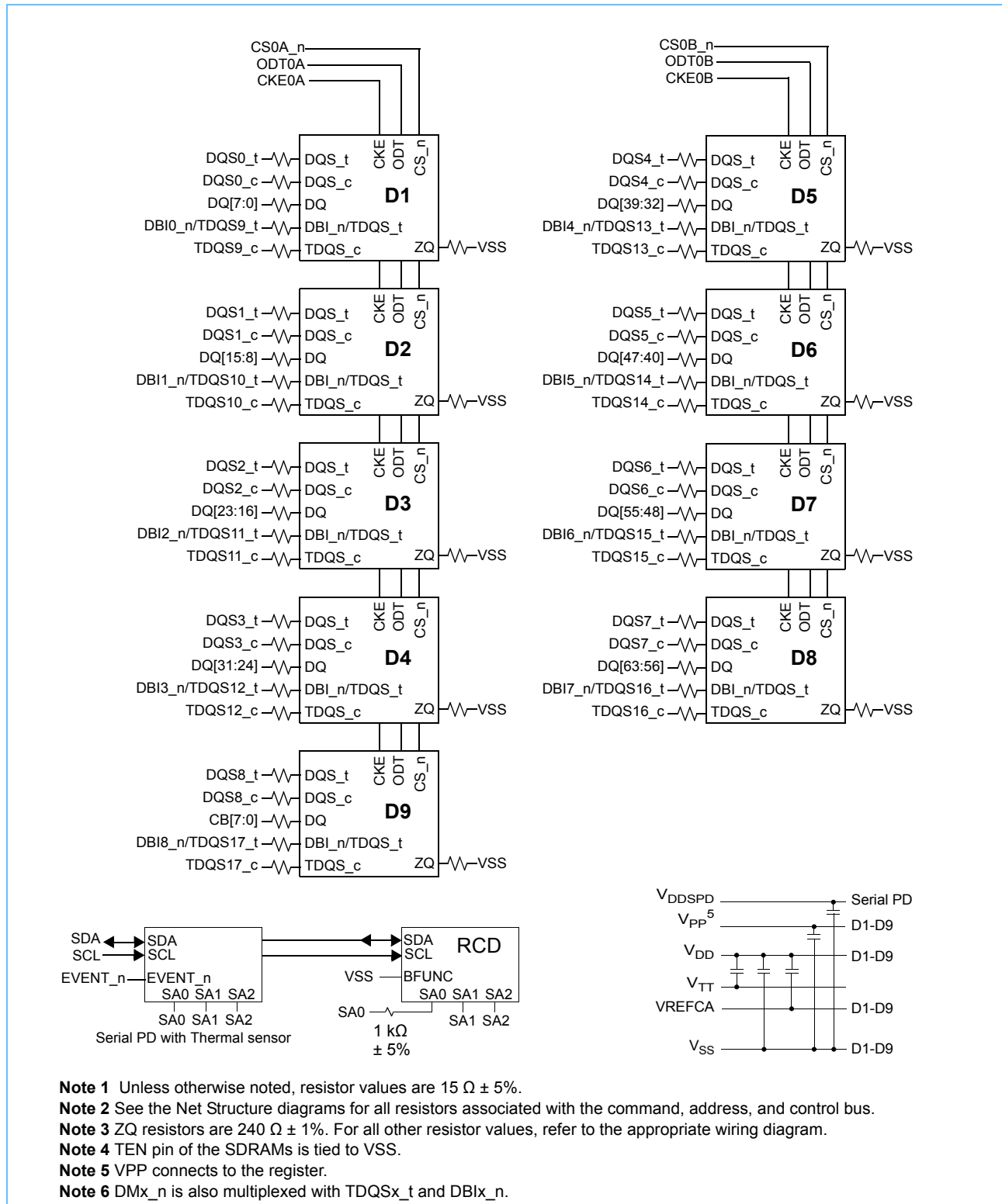
Note 2 CK1_t, CK1_c terminated with 120 $\Omega \pm 5\%$ resistor but not used.

Note 3 Unless otherwise noted resistors are 22 $\Omega \pm 5\%$.

Note 4 Register input CS1_n is tied to VDD. Register inputs ODT1 and CKE1 are tied to VSS.

Functional Block Diagram

x72 DIMM, populated as one package rank of x8 DDR4 SDRAMs (Part 2 of 2)



Registered Clock Driver, Input Loading and Test Points

Refer to the DDR4RCD01 vendor data sheets for all technical specifications and requirements.
The DDR4RCD01 component will be referred to as the register throughout this document.

Loading

Signal Names	Input to Device	Loads
CK0_t, CK0_c	Register	1
CK1_t, CK1_c ²	Termination Resistor Only	1 ²
RESET_n	Register	1
CKE0, ODT0	Register	1 ¹
Ax, BAx, BGx, PARITY, ACT_n	Register	1 ¹
CS0_n, C[2:0]	Register	1 ¹
DQ, CB, DQSx_t, DQSx_c, TDQSx_t ³ , TDQSx_c	SDRAM	1
SCL, SDA, SA[2:0]	SPD with Thermal Sensor, Register	2
ALERT_n	Register	1
EVENT_n	SPD with Thermal Sensor	1
Note 1 Programmable resistive terminations are available on the Register. Note 2 Connected but not used. Note 3 TDQS_t is multiplexed with DBI_n and DM_n.		

Test Point Locations

Signal Group	Signal	Signal locations
Address/Command/ Control/PARITY	Pre Register	22 Ω series resistor. Closer to the register provides better SI.
	Post Register	Termination resistors on the ends of the module.
DQ,CB	Series resistor	15 Ω resistors
DQS_t, DQS_c	Series resistor	15 Ω resistors
Clock	Termination resistor	120 Ω termination resistor.
	Post Register	Termination resistors on the ends of the module.
Note 1 Refer to the registration package for additional test point information.		

Manufactured DIMM Improvement

Manufactured DIMMs may improve on the reference design as long as the skew is reduced relative to the reference design. It is a requirement that improvements not move the basic timing away from the reference design such that system integrity is jeopardized for systems defined to operate with the original reference design. The skew values reported in the tables only accounts for skew related to the DIMM PCB traces and vias of the reference design. No other error sources are included. The only exception is if the skew evaluation chose to use an actual SDRAM package or an idealized (uniform) package. This should be identified in a note below each table. The skew is only intended to document the design as a reference point if a manufacturer chooses to improve the design over the reference design. The skew is not a measurable value. Measured values of skew will always be greater than the values reported in the tables because other error sources will also be included.