

Annex J - Raw Card J

DDR4 Registered DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
J0	PC4-RDIMM_V090_RC_J0_20130725.brd	PC4-RDIMM_V090_RC_J0_20130725-BOM.txt
J1	PC4-RDIMM_V200_RC_J1_20150212.brd	PC4-RDIMM_V200_RC_J1_20150212-BOM.docx

Note 1 "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.

Module Configuration

DIMM Maximum Capacity	DIMM Organization	Die Density	SDRAM Organization	SDRAM die per DIMM	Package Ranks per DIMM	# of Address bits row/col	MO-309 variation ²
8 GB	2 x 512M x72	2 Gb	512M x 4	36	2	15 / 10 ¹	BAxA
16 GB	2 x 1G x72	4 Gb	1G x 4	36	2	16 / 10 ¹	BAxA
32 GB	2 x 2G x72	8 Gb	2G x 4	36	2	17 / 10	BAxA
64 GB	2 x 4G x72	16 Gb	4G x 4	36	2	18 / 10	BAxA

Note 1 Address A16 is the highest address bit used for this density based on it being multiplexed with RAS_n.

Note 2 BAxA assumes there is not a heat spreader.

SDRAM Configuration

Raw Card	Supported DRAM Outline (Width x Length) nominal (mm)	# of Banks in SDRAM BA / BG	SDRAM Package Type	Package Type	MO-207 variation
J0	10.0 x 13.0	2 / 2	78 Ball FBGA	DDP	DW-z
J1	9.0 x 13.0	2 / 2	78 Ball FBGA	DDP	DW-z

Note 1 DDP is a two die per package using conventional stacking, not 3DS.

Supported Speeds

Raw Card		PC4-1333	PC4-1600	PC4-1866	PC4-2133	PC4-2400	PC4-2666	PC4-2933	PC4-3200	Notes
J0		X	X	X	X					1, 2
J1		N	N	N	N	N				1, 2

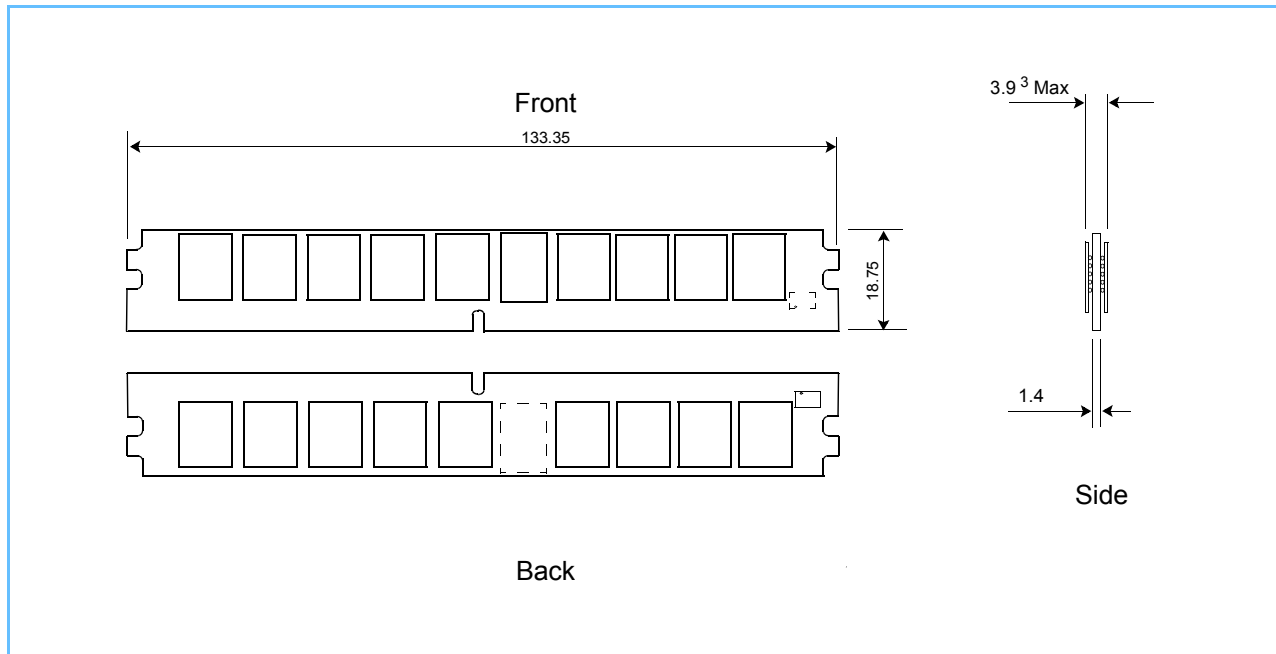
Note 1 X reflects speed grades approved previously.

Note 2 N denotes NEW speed grades.

Design Deviations

Note 1 Microvias are between layers 1 and 2 and between layers 11 and 12 are used in the R/C J0 and R/C J1 designs.

General Layout



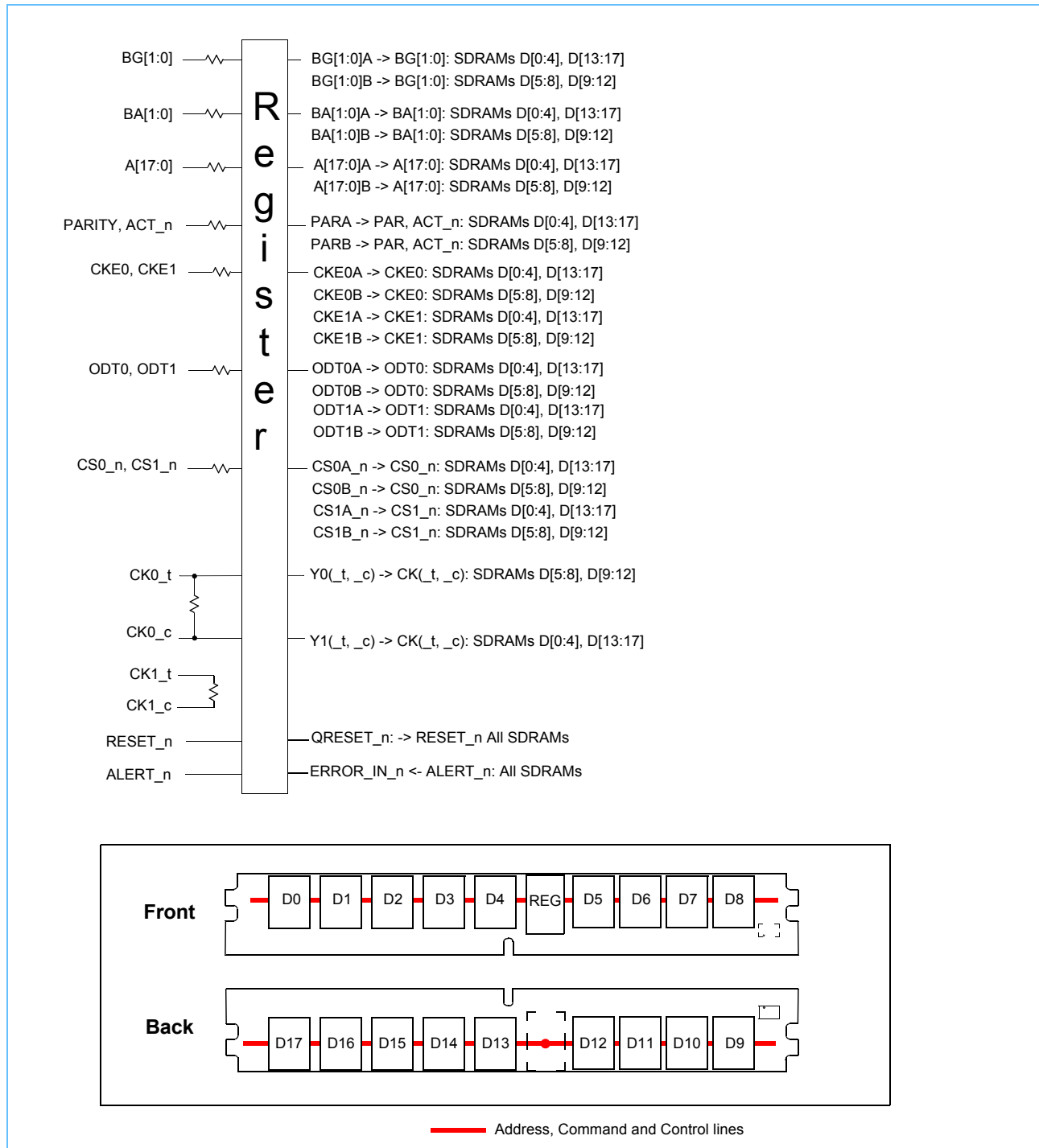
Note 1 Refer to MO-309 for more detailed information. All dimensions are in mm.

Note 2 Variation is BAxA (B-Module height, A-Module thickness, x-plating, A-DDR4 Key Position).

Note 3 Module thickness varies with SDRAM thickness and whether a heat spreader is present or not. Variation A is valid for DRAMs less than or equal to 1.2 mm maximum with no heat spreader attached.

Functional Block Diagram

x72 DIMM, populated as two package ranks of x4 DDR4 SDRAMs (Part 1 of 3)



Note 1 CK0_t, CK0_c terminated with 120 $\Omega \pm 5\%$ resistor.

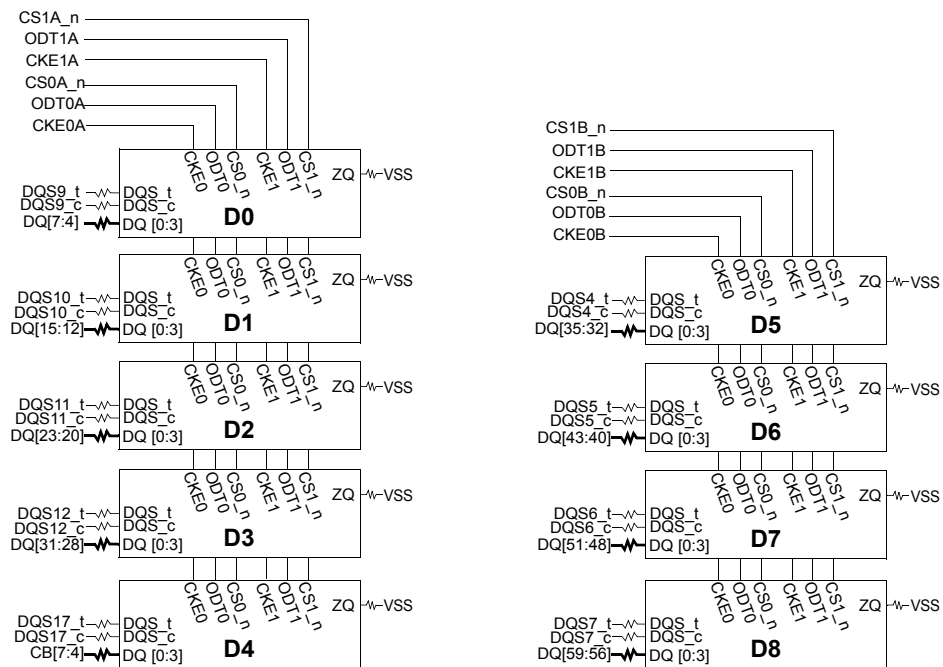
Note 2 CK1_t, CK1_c terminated with 120 $\Omega \pm 5\%$ resistor but not used.

Note 3 Unless otherwise noted resistors are 22 $\Omega \pm 5\%$.

Note 4 Register inputs BFUNC and C2 are tied to VSS. Inputs C0/CS2_n and C1/CS3_n are tied to VDD.

Functional Block Diagram

x72 DIMM, populated as two package ranks of x4 DDR4 SDRAMs (Part 2 of 3)



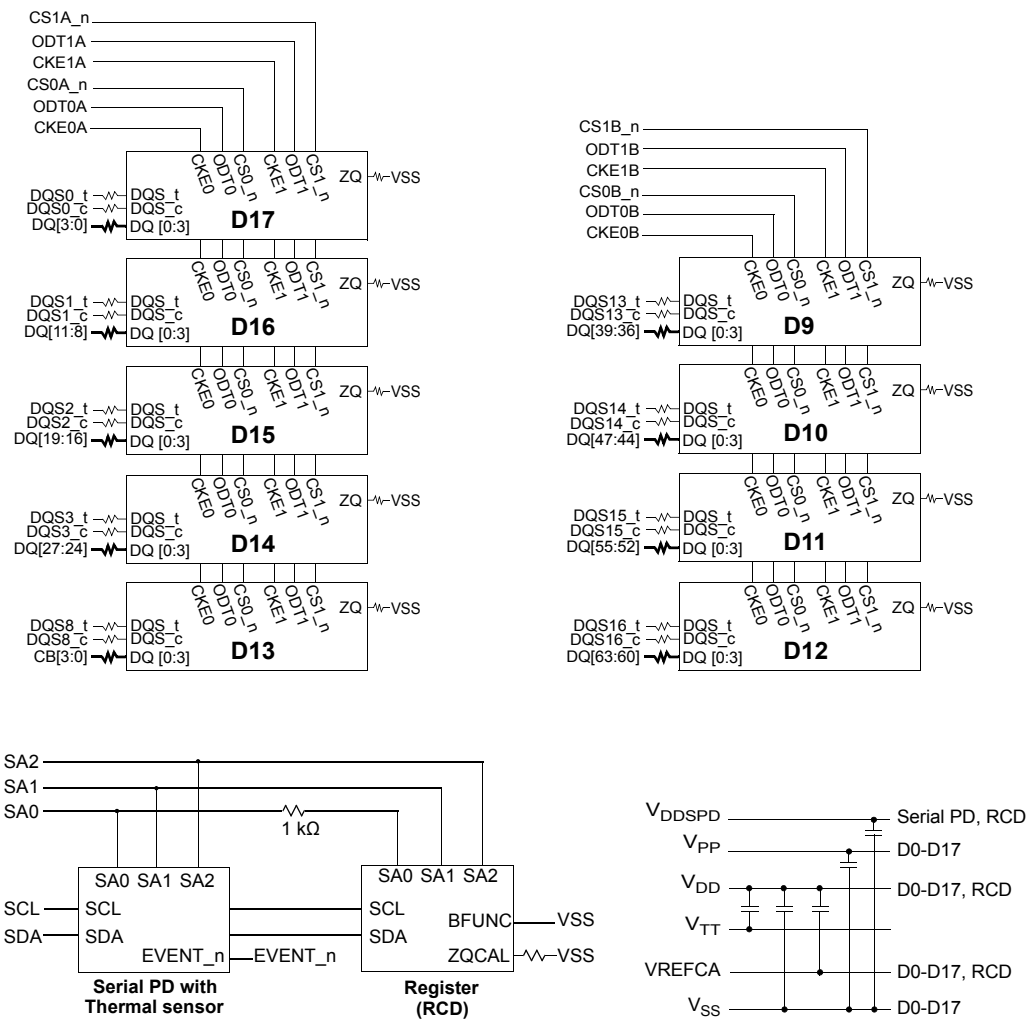
Note 1 Unless otherwise noted, resistor values are $15\ \Omega \pm 5\%$.

Note 2 See the Net Structure diagrams for all resistors associated with the command, address and control bus.

Note 3 ZQ resistors are $240\ \Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.

Note 4 TEN pin of SDRAMs is tied to VSS.

x72 DIMM, populated as two package ranks of x4 DDR4 SDRAMs (Part 3 of 3)



Note 1 Unless otherwise noted, resistor values are $15\ \Omega \pm 5\%$.

Note 2 See the Net Structure diagrams for all resistors associated with the command, address and control bus.

Note 3 ZQ resistors are $240\ \Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.

Note 4 TEN pin of SDRAMs is tied to VSS.

Registered Clock Driver, Input Loading and Test Points

Refer to the DDR4RCDxx vendor data sheets for all technical specifications and requirements.
The DDR4RCDxx component will be referred to as the register throughout this document.

Loading

Signal Names	Input to Device	Loads
CK0_t, CK0_c	Register	1
CK1_t, CK1_c ²	Termination Resistor Only	1 ²
RESET_n	Register	1
CKE0, CKE1, ODT0, ODT1	Register	1 ¹
Ax, BAx, BGx, ACT_n, PARITY	Register	1 ¹
CS0_n, CS1_n	Register	1 ¹
DQ, CB, DQS_t, DQS_c	SDRAM	1 ³
SCL, SDA, SA[2:0]	SPD with Thermal Sensor, Register	2
EVENT_n	SPD with Thermal Sensor	1
ALERT_n	Register	1

Note 1 Programmable resistive terminations are available on the Register.

Note 2 Connected but not used.

Note 3 Connected to 2 die within SDRAM package

Test Point Locations

Signal Group	Signal Area	Signal locations
Address / Command / Control / PARITY	Pre Register	22 Ω series resistor. Closer to the register provides better SI.
	Post Register	Termination resistors on the ends of the module.
DQ, CB	Series resistor	15 Ω resistors
DQS_t, DQS_c	Series resistor	15 Ω resistors
Clock	Termination resistor	120 Ω termination resistor.
	Post Register	Termination resistors on the ends of the module.

Note 1 Refer to the registration package for additional test point information.

Manufactured DIMM Improvement

Manufactured DIMMs may improve on the reference design as long as the skew is reduced relative to the reference design. It is a requirement that improvements not move the basic timing away from the reference design such that system integrity is jeopardized for systems defined to operate with the original reference design. The skew values reported in the tables only accounts for skew related to the DIMM PCB traces and vias of the reference design. No other error sources are included. The only exception is if the skew evaluation chose to use an actual SDRAM package or an idealized (uniform) package. This should be identified in a note below each table. The skew is only intended to document the design as a reference point if a manufacturer chooses to improve the design over the reference design. The skew is not a measurable value. Measured values of skew will always be greater than the values reported in the tables because other error sources will also be included.