

**4.20.3 – 144 Pin, PC133 SDRAM Unbuffered SO-DIMM, Reference Design
Specification**

**PC133 SDRAM Unbuffered SO-DIMM
Reference Design Specification
Revision 1.02**

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1. Product Description

This reference specification defines the electrical and mechanical requirements for 144-pin, 3.3 Volt, 133 MHz, 64-bit wide, Unbuffered Synchronous DRAM Small Outline Dual In-Line Memory Modules (SDRAM SO-DIMMs). These SDRAM SO-DIMMs are intended for use as main memory when installed in systems such as mobile personal computers.

Reference design examples are included which provide an initial basis for Unbuffered SO-DIMM designs. Modifications to these reference designs are required to meet all system timing, signal integrity and thermal requirements for 133 MHz support. Other designs are acceptable, and all Unbuffered SO-DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

This specification largely follows the JEDEC defined 144-pin 8-Byte Unbuffered SDRAM SO-DIMM product. (Refer to JEDEC standard 21-C, Section 4.5.6, at www.jedec.org).

Product Family Attributes

SO-DIMM Organization	x 64
SO-DIMM Dimensions (nominal)	67.6 mm (2.66") x 25.40 mm (1.0") to x 31.75 mm (1.25")
Pin Count	144
SDRAMs Supported	64 Mb, 128 Mb, 256 Mb
Capacity	32 MB, 64 MB, 128 MB, 256 MB
Serial PD	Consistent with JEDEC Rev. 2.0
Voltage Options	3.3 volt (V_{DD}/V_{DDQ})
Interface	LVTTL

2. Environmental Requirements

PC133 SDRAM Unbuffered SO-DIMMs are intended for use in mobile computing environments that have limited capacity for heat dissipation.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
T _{OPR}	Operating Temperature (ambient)	0 to +65	°C	1
H _{OPR}	Operating Humidity (relative)	10 to 90	%	1
T _{STG}	Storage Temperature	-50 to +100	°C	1
H _{STG}	Storage Humidity (without condensation)	5 to 95	%	1
	Barometric Pressure (operating & storage)	105 to 69	kPa	1, 2
1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. 2. Up to 9850 ft.				

3. Architecture

Pin Description

CK(0:1)	Clock Inputs	2	DQ(0:63)	Data Input/Output	64
CKE(0:1)	Clock Enables	2	DQMB(0:7)	Data Mask	8
RAS	Row Address Strobe	1	V _{DD}	Power (3.3 V)	18
CAS	Column Address Strobe	1	V _{SS}	Ground	18
WE	Write Enable	1	SCL	Serial Presence Detect Clock Input	1
$\bar{S}$ (0:1)	Chip Selects	2	SDA	Serial Presence Detect Data Input/Output	1
A(0:9,11:13)	Address Inputs	13	NC	No Connect	8
A10/AP	Address Input/Autoprecharge	1	DU	Don't Use - leave as NC	1
BA0-BA1	SDRAM Bank Address	2		Total:	144

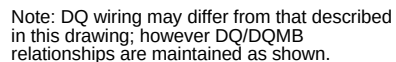
Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0 - CK1	Input	Positive Edge	The system clock inputs. All of the SDRAM inputs are sampled on the rising edge of their associated clock.
CKE0,1	Input	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{S0} - \overline{S1}$	Input	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Physical Bank 0 is selected by $\overline{S0}$; Bank 1 is selected by $\overline{S1}$.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA0, BA1	Input	—	Selects which SDRAM bank of four is activated.
A0 - A9, A11-A13 A10/AP	Input	—	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A11 defines the column address (CA0-CA11) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, then BA0 and BA1 are used to define which bank to precharge.
DQ0 - DQ63	Input Output	—	Data Bit Input/Output pins.
DQMB0 - DQMB7	Input	Active High	The Data Input/Output masks, associated with one data byte, place the DQ buffers in a high impedance state when sampled high. In Read mode, DQMB controls the output buffers like an output enable. In Write mode, DQMB operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high.
V _{DD} , V _{SS}	Supply		Power and ground for the module.
SDA	Input Output	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected to V _{DD} to act as a pull up.
SCL	Input	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to V _{DD} to act as a pull up.

Unbuffered SDRAM SO-DIMM Pinout

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	V _{SS}	2	V _{SS}	37	DQ8	38	DQ40	73	NU	74	CK1	109	A9	110	BA1
3	DQ0	4	DQ32	39	DQ9	40	DQ41	75	V _{SS}	76	V _{SS}	111	A10/AP	112	A11
5	DQ1	6	DQ33	41	DQ10	42	DQ42	77	NC	78	NC	113	V _{DD}	114	V _{DD}
7	DQ2	8	DQ34	43	DQ11	44	DQ43	79	NC	80	NC	115	DQMB2	116	DQMB6
9	DQ3	10	DQ35	45	V _{DD}	46	V _{DD}	81	V _{DD}	82	V _{DD}	117	DQMB3	118	DQMB7
11	V _{DD}	12	V _{DD}	47	DQ12	48	DQ44	83	DQ16	84	DQ48	119	V _{SS}	120	V _{SS}
13	DQ4	14	DQ36	49	DQ13	50	DQ45	85	DQ17	86	DQ49	121	DQ24	122	DQ56
15	DQ5	16	DQ37	51	DQ14	52	DQ46	87	DQ18	88	DQ50	123	DQ25	124	DQ57
17	DQ6	18	DQ38	53	DQ15	54	DQ47	89	DQ19	90	DQ51	125	DQ26	126	DQ58
19	DQ7	20	DQ39	55	V _{SS}	56	V _{SS}	91	V _{SS}	92	V _{SS}	127	DQ27	128	DQ59
21	V _{SS}	22	V _{SS}	57	NC	58	NC	93	DQ20	94	DQ52	129	V _{DD}	130	V _{DD}
23	DQMB0	24	DQMB4	59	NC	60	NC	95	DQ21	96	DQ53	131	DQ28	132	DQ60
25	DQMB1	26	DQMB5	61	CK0	62	CKE0	97	DQ22	98	DQ54	133	DQ29	134	DQ61
27	V _{DD}	28	V _{DD}	63	V _{DD}	64	V _{DD}	99	DQ23	100	DQ55	135	DQ30	136	DQ62
29	A0	30	A3	65	RAS	66	CAS	101	V _{DD}	102	V _{DD}	137	DQ31	138	DQ63
31	A1	32	A4	67	WE	68	CKE1	103	A6	104	A7	139	V _{SS}	140	V _{SS}
33	A2	34	A5	69	S0	70	A12	105	A8	106	BA0	141	SDA	142	SCL
35	V _{SS}	36	V _{SS}	71	S1	72	A13	107	V _{SS}	108	V _{SS}	143	V _{DD}	144	V _{DD}
Note:															

(Populated as 1 physical bank of x16 SDRAMs)



Block Diagram: Raw Card Version B

(Populated as 2 physical banks of x16 SDRAMs)

