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PC3200/PC2700/PC2100/PC1600 DDR SDRAM Unbuffered SO-DIMM

Reference Design Specification

Revision 1.4

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Unbuffered PC3200/PC2700/PC2100/PC1600 DDR SDRAM SO-DIMM

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1. Product Description

This reference specification defines the electrical and mechanical requirements for the PC3200 module, a 200-pin, 200 MHz clock (400 MT/s data rate), 64-bit wide, Unbuffered Synchronous Double Data Rate (DDR) DRAM Small Outline Dual In-Line Memory Module (DDR SDRAM SO-DIMMs). It also defines a slower version, PC2700, using 167 MHz clock (333 MT/s data rate) or PC2100, using 133 MHz clock (266 MT/s data rate) or PC1600, using 100 MHz clock (200 MT/s data rate) DDR SDRAMs. These DDR SDRAM SO-DIMMs are intended for use as main memory when installed in systems such as mobile personal computers or small form factor PCs. PC3200 DIMM modules use DDR400 devices.

Reference design examples are included which provide an initial basis for Unbuffered SO-DIMM designs. Any modifications to these reference designs must meet all system timing, signal integrity and thermal requirements for the supported maximum clock rate. Other designs are acceptable, and all Unbuffered SO-DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

Product Family Attributes

Attribute:	Values:	Notes:
SO-DIMM Organization	x 64, x 72	
SO-DIMM Dimensions (nominal)	31.75 mm high, 67.60 mm wide	
SO-DIMM Types Supported	Unbuffered, Unbuffered with PLL, Registered with PLL	
Pin Count	200	
SDRAMs Supported	64 Mb, 128 Mb, 256 Mb, 512 Mb, 1 Gb	
SDRAMs Device Widths Supported	x8, x16	
Capacity	32 MB, 64 MB, 128 MB, 256 MB, 512 MB, 1 GB	
Serial Presence Detect	Consistent with JEDEC Rev. 1.0	
Voltage Options	2.5 V V_{DD} 2.5 V V_{DDQ} 2.6 V for V_{DD} PC3200 module only 2.6 V for V_{DDQ} PC3200 module only 2.5 V to 3.3 V V_{DDSPD}	1
Interface	SSTL_2	
Note 1: V_{DDSPD} is not tied to V_{DD} or V_{DDQ} on the DDR SO-DIMM.		

Product Family Variations (Raw Cards)

Raw Card	Device Type	Module Bus Width	Device Width	Number of Devices	Physical Banks	Capacity
A	TSOP-II	x64	x16	8	2	256 MB to 1 GB
B	TSOP-II	x64	x8	8	1	256 MB to 1 GB
C	TSOP-II	x64	x16	4	1	128 to 512 MB
C	TSOP-II	x72	x16	5	1	128 to 512 MB

2. Environmental Requirements

Unbuffered PC3200/PC2700/PC2100/PC1600 DDR SDRAM SO-DIMM

2. Environmental Requirements

PC3200/PC2700/PC2100/PC1600 DDR SDRAM Unbuffered SO-DIMMs are intended for use in mobile computing environments that have limited capacity for heat dissipation.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
T _{OPR}	Operating Temperature (ambient)	0 to +65	°C	1
H _{OPR}	Operating Humidity (relative)	10 to 90	%	1
T _{STG}	Storage Temperature	-50 to +100	°C	1
H _{STG}	Storage Humidity (without condensation)	5 to 95	%	1
	Barometric Pressure (operating & storage)	105 to 69	kPa	1, 2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.

3. Architecture

Pin Description

CK(0:2)	Clock Inputs, positive line	3	DQ(0:63)	Data Input/Output	64
$\overline{\text{CK}}$ (0:2)	Clock inputs, negative line	3	CB(7:0)	Data check bits Input/Output	8
CKE(0:1)	Clock Enables	2	DM(0:8)	Data Masks	9
$\overline{\text{RAS}}$	Row Address Strobe	1	DQS(0:8)	Data strobes	9
$\overline{\text{CAS}}$	Column Address Strobe	1			
$\overline{\text{WE}}$	Write Enable	1	V _{DD}	Core and I/O Power	33
$\overline{\text{S}}$ (0:1)	Chip Selects	2	V _{SS}	Ground	33
A(0:9,11:13)	Address Inputs	13	V _{REF}	Input/Output Reference	2
A10/AP	Address Input/Autoprecharge	1	V _{DD} SPD	SPD Power	1
BA(0:1)	SDRAM Bank Address	2	V _{DD} ID	V _{DD} , V _{DD} Q level detection	1
SCL	Serial Presence Detect (SPD) Clock Input	1			
SDA	SPD Data Input/Output	1	TEST	Reserved for test equipment use	1
SA(0:2)	SPD address	3	DU	Reserved for future use	5
Total:					200

Input/Output Functional Description

Symbol	Type	Polarity	Function
$\overline{\text{CK0}} - \overline{\text{CK2}}, \overline{\text{CK0}} - \overline{\text{CK2}}$	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE0, CKE1	Input	Active High	Activates the DDR SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{\text{S0}}, \overline{\text{S1}}$	Input	Active Low	Enables the associated DDR SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Physical Bank 0 is selected by $\overline{\text{S0}}$; Bank 1 is selected by $\overline{\text{S1}}$.
$\overline{\text{RAS}}, \overline{\text{CAS}}, \overline{\text{WE}}$	Input	Active Low	When sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, and $\overline{\text{WE}}$ define the operation to be executed by the SDRAM.
BA0 - BA1	Input	—	Selects which DDR SDRAM bank of four is activated.
A0 - A9, A11-A13, A10/AP	Input	—	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, then BA0 and BA1 are used to define which bank to precharge.
DQ0 - DQ63	In/Out	—	Data Bit Input/Output pins.
CB0 - CB7	In/Out	—	Data Check Bit Input/Output pins. Not used on x64 modules.
DM0 - DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
DQS0 - DQS8	In/Out	—	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR SDRAMs and is sent at the leading edge of the data window. DQS8 is associated with check bits CB0-CB7, and is not used on x64 modules.
$V_{\text{DD}}, V_{\text{DDSPD}}, V_{\text{SS}}$	Supply	—	Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
V_{DDID}	Out	—	Defines relationship of V_{DD} and V_{DDQ} . If V_{DDID} is open, $V_{\text{DD}} = V_{\text{DDQ}}$; if V_{DDID} is pulled to V_{SS} , $V_{\text{DD}} \neq V_{\text{DDQ}}$. This line should be pulled high through 10 K Ω on the host board.
SDA	In/Out	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected to V_{DD} to act as a pull up.
SCL	Input	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to V_{DD} to act as a pull up.
SA0 - SA2	Input	—	Address pins used to select the Serial Presence Detect.
TEST	In/Out	—	The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules (SO-DIMMs).

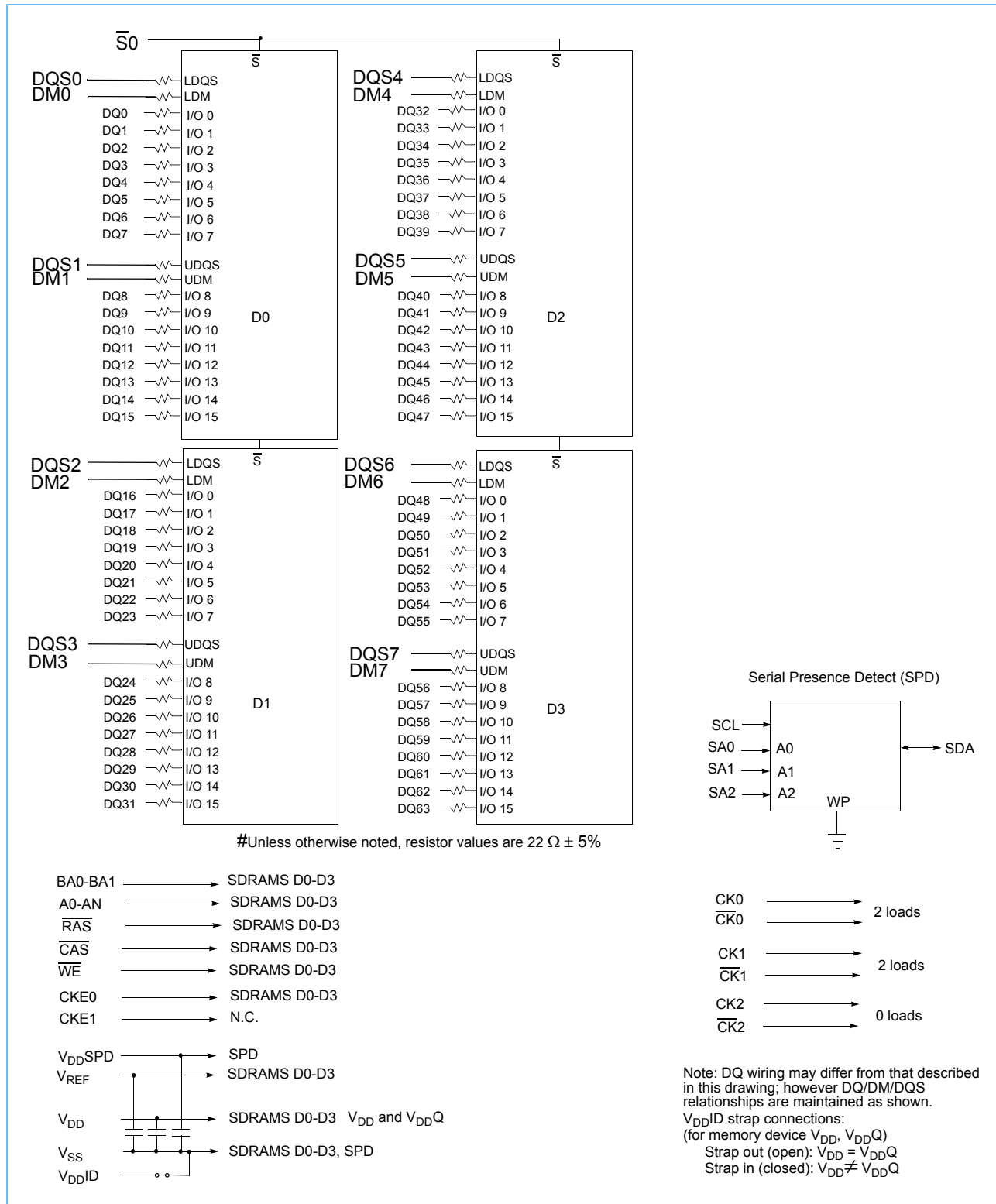
DDR SDRAM SO-DIMM Pinout

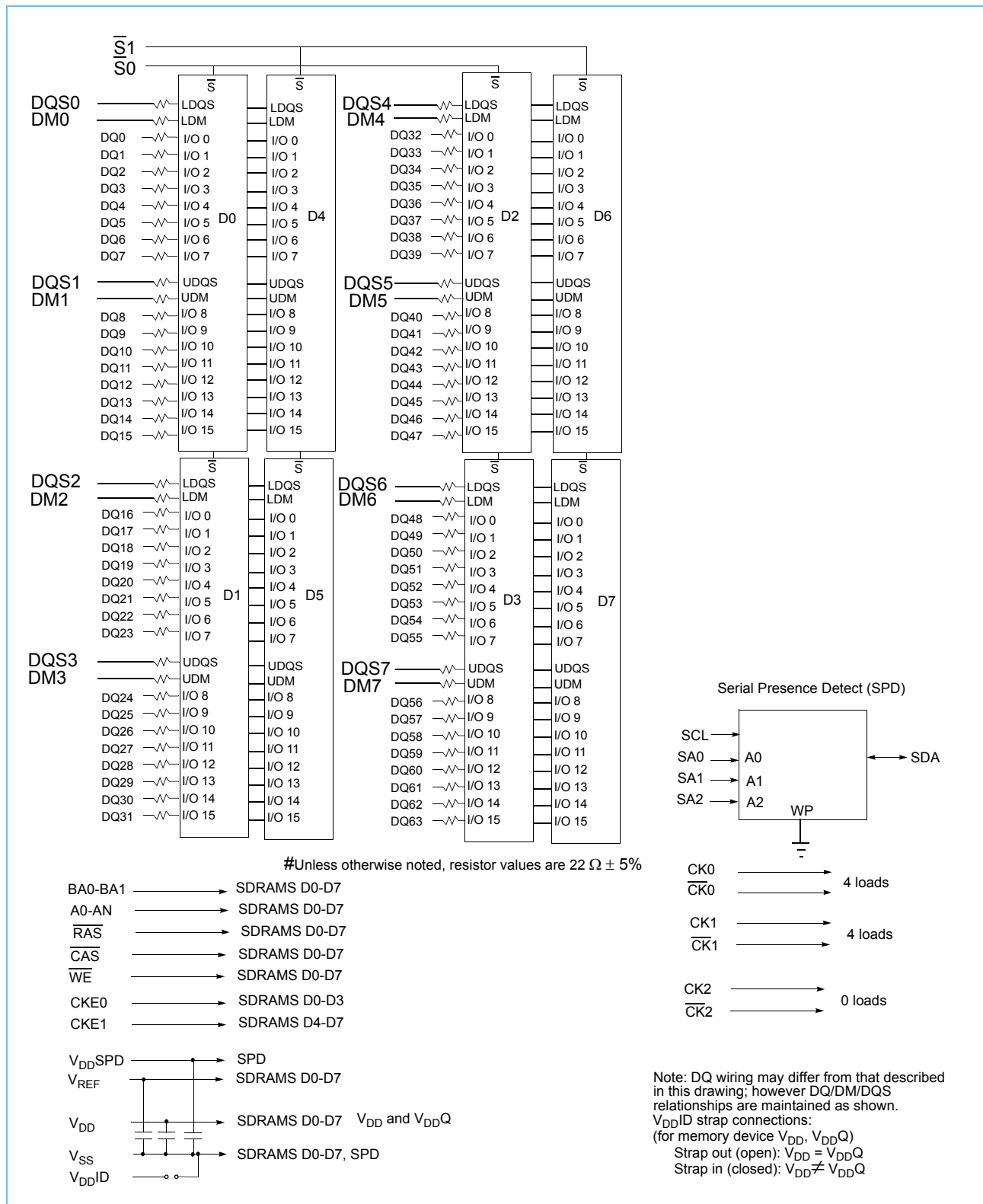
Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	V _{REF}	2	V _{REF}	51	V _{SS}	52	V _{SS}	101	A9	102	A8	151	DQ42	152	DQ46
3	V _{SS}	4	V _{SS}	53	DQ19	54	DQ23	103	V _{SS}	104	V _{SS}	153	DQ43	154	DQ47
5	DQ0	6	DQ4	55	DQ24	56	DQ28	105	A7	106	A6	155	V _{DD}	156	V _{DD}
7	DQ1	8	DQ5	57	V _{DD}	58	V _{DD}	107	A5	108	A4	157	V _{DD}	158	$\overline{\text{CK}}1$
9	V _{DD}	10	V _{DD}	59	DQ25	60	DQ29	109	A3	110	A2	159	V _{SS}	160	CK1
11	DQS0	12	DM0	61	DQS3	62	DM3	111	A1	112	A0	161	V _{SS}	162	V _{SS}
13	DQ2	14	DQ6	63	V _{SS}	64	V _{SS}	113	V _{DD}	114	V _{DD}	163	DQ48	164	DQ52
15	V _{SS}	16	V _{SS}	65	DQ26	66	DQ30	115	A10/AP	116	BA1	165	DQ49	166	DQ53
17	DQ3	18	DQ7	67	DQ27	68	DQ31	117	BA0	118	$\overline{\text{RAS}}$	167	V _{DD}	168	V _{DD}
19	DQ8	20	DQ12	69	V _{DD}	70	V _{DD}	119	$\overline{\text{WE}}$	120	$\overline{\text{CAS}}$	169	DQS6	170	DM6
21	V _{DD}	22	V _{DD}	71	CB0	72	CB4	121	$\overline{\text{S}}0$	122	$\overline{\text{S}}1$	171	DQ50	172	DQ54
23	DQ9	24	DQ13	73	CB1	74	CB5	123	A13	124	DU	173	V _{SS}	174	V _{SS}
25	DQS1	26	DM1	75	V _{SS}	76	V _{SS}	125	V _{SS}	126	V _{SS}	175	DQ51	176	DQ55
27	V _{SS}	28	V _{SS}	77	DQS8	78	DM8	127	DQ32	128	DQ36	177	DQ56	178	DQ60
29	DQ10	30	DQ14	79	CB2	80	CB6	129	DQ33	130	DQ37	179	V _{DD}	180	V _{DD}
31	DQ11	32	DQ15	81	V _{DD}	82	V _{DD}	131	V _{DD}	132	V _{DD}	181	DQ57	182	DQ61
33	V _{DD}	34	V _{DD}	83	CB3	84	CB7	133	DQS4	134	DM4	183	DQS7	184	DM7
35	CK0	36	V _{DD}	85	DU	86	$\overline{\text{DU}}$ (RESET)	135	DQ34	136	DQ38	185	V _{SS}	186	V _{SS}
37	$\overline{\text{CK}}0$	38	V _{SS}	87	V _{SS}	88	V _{SS}	137	V _{SS}	138	V _{SS}	187	DQ58	188	DQ62
39	V _{SS}	40	V _{SS}	89	CK2	90	V _{SS}	139	DQ35	140	DQ39	189	DQ59	190	DQ63
41	DQ16	42	DQ20	91	$\overline{\text{CK}}2$	92	V _{DD}	141	DQ40	142	DQ44	191	V _{DD}	192	V _{DD}
43	DQ17	44	DQ21	93	V _{DD}	94	V _{DD}	143	V _{DD}	144	V _{DD}	193	SDA	194	SA0
45	V _{DD}	46	V _{DD}	95	CKE1	96	CKE0	145	DQ41	146	DQ45	195	SCL	196	SA1
47	DQS2	48	DM2	97	DU	98	DU	147	DQS5	148	DM5	197	V _{DD} SPD	198	SA2
49	DQ18	50	DQ22	99	A12	100	A11	149	V _{SS}	150	V _{SS}	199	V _{DD} ID	200	NC, TEST

Note: Pins 71, 72, 73, 74, 77, 78, 79, 80, 83, 84 are reserved for x72 variants of this module and are not used on the x64 versions.

Note: Pin 86 is reserved for a registered variant of this module and is not used on the unbuffered version.

Note: Pins 89, 91 are reserved for x72 modules or registered modules.

Block Diagram: Raw Card Version C (Populated as 1 physical bank of x16 SDRAMs)

Block Diagram: Raw Card Version A (Populated as 2 physical banks of x16 SDRAMs)

Block Diagram: Raw Card Version B (Populated as 1 physical bank of x8 SDRAMs)