
PC3200/PC2700 DDR SDRAM Unbuffered DIMM - TSOP- Based DRAMs

Design Specification

Revision 1.2

January 10, 2003

Contents

1. Product Description	4
1.1 Product Family Attributes	4
2. Environmental Requirements	5
2.1 Absolute Maximum Ratings	5
3. Architecture	5
3.1 Pin Description	5
3.2 Input/Output Functional Description	6
3.3 184-Pin DDR SDRAM DIMM Pin Assignments	7
3.4 Block Diagram: Raw Card Version A, x72	8
3.5 Block Diagram: Raw Card Version A, x64	9
3.6 Block Diagram: Raw Card Version B, x64	10
3.7 Block Diagram: Raw Card Version B, x72	11
3.8 Block Diagram: Raw Card Version C, x64	12
3.9 Block Diagram: Raw Card Version C, x72	13
3.10 Logical Clock Net Structures	14
4. Component Details	15
4.1 Pin Assignments for 64 Mb, 128 Mb, 256 Mb, 512 Mb and 1 Gb DDR SDRAM Planar Components	15
4.2 DDR SDRAM Component Specifications	16
5. Unbuffered DIMM Details	16
5.1 SDRAM Module Configurations (Reference Designs)	16
5.2 Input Loading Matrix	18
5.3 DDR Unbuffered Design File Releases	18
5.4 Component Types and Placement	19
5.5 Example Raw Card A Component Placement	19
5.6 Example Raw Card B Component Placement	20
5.7 Example Raw Card C Component Placement	20
6. DIMM Wiring Details	21
6.1 Signal Groups	21
6.2 General Net Structure Routing Guidelines	21
6.3 Explanation of Net Structure Diagrams	22
6.4 Net Structure Example	22
6.5 Clock Net Structures	23
6.6 Signal Net Structures	24
6.7 Cross Section Recommendations	35
6.8 Decoupling	35
7. Design Target	36
7.1 Address setup/hold flight times	36
7.2 Clock Skew Contributions (tSKEW)	36

PC3200/PC2700 DDR SDRAM Unbuffered DIMM Design Specification

Contents

8. Serial PD Definition 37

 8.1 Serial Presence Detect Example Raw Card Version 'B' 37

 8.2 Serial Presence Detect Component Specification..... 39

9. Product Label 40

10. DIMM Mechanical Specifications 41

 10.1 Simplified Mechanical Drawing with Keying Positions 41

11. Clocking Timing Methodology 42

 11.1 Unbuffered DIMM Differential Clock Reference Net..... 42

12. Revision Log 43

1. Product Description

This specification defines the electrical and mechanical requirements for 184-pin, TSOP-based, 2.5 volt (V_{DD})/ 2.5 volt (V_{DDQ}) (DC voltage range 2.3 - 2.7 V) for PC2700 & 2.6 volt (V_{DD})/ 2.6 volt (V_{DDQ}) (DC voltage range 2.5 - 2.7 V) for PC3200, Unbuffered, Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR SDRAM DIMMs). These DDR DIMMs are intended for use as main memory when installed in PCs. The DDR DIMMs must permit operation with a new address every clock cycle in PC3200/PC2700 environments. PC3200 DIMM modules use DDR400 devices.

Reference design examples are included which provide an initial basis for Unbuffered DDR DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity and thermal requirements for PC3200/PC2700 support. All Unbuffered DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

This specification largely follows the JEDEC defined 184-pin Unbuffered DDR SDRAM DIMM product. (Refer to JEDEC standard JESD21-C, Section 4.5.10, at www.jedec.org).

1.1 Product Family Attributes

DIMM Organization	x64, x72 ECC	Notes
DIMM Dimensions (max)	133.50 mm x 31.90 mm x 4.00 mm (5.256" x 1.256" x 0.157")	MO-206 Variation BA
Pin Count	184	
Pin Pitch	1.27 mm	
DDR SDRAMs Supported	64 Mb, 128 Mb, 256 Mb, 512 Mb, 1 Gb	
Capacity	32 MB - 2 GB	
Serial PD	Consistent with JEDEC JC 42.5 Item 849A	
Voltage Options	2.5 volt V_{DD}/V_{DDQ} 2.3 volt to 3.6 volt V_{DD} SPD 2.6 volt V_{DD}/V_{DDQ} for PC3200 only	All DDR modules use a common V_{DD} - V_{DDQ} power plane. They are tied together on the DIMM, but by standard definition are supported on the pinout to accommodate future enhancements.
Interface	SSTL_2	
Note 1: V_{DD} SPD is not tied to V_{DD} or V_{DDQ} on the DDR DIMM.		

2. Environmental Requirements

184-pin Unbuffered DDR SDRAM DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

2.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
T _{OPR}	Operating Temperature (ambient)	0 to +55	°C	1
H _{OPR}	Operating Humidity (relative)	10 to 90	%	1
T _{STG}	Storage Temperature	-50 to +100	°C	1
H _{STG}	Storage Humidity (without condensation)	5 to 95	%	1
	Barometric Pressure (operating & storage)	105 to 69	KPa	1, 2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.

3. Architecture

3.1 Pin Description

Pin Name	Description
A0 - A13	SDRAM address bus
BA0 - BA1	SDRAM bank select
DQ0 - DQ63	DIMM memory data bus
CB0 - CB7	DIMM ECC check bits
$\overline{\text{RAS}}$	SDRAM row address strobe
$\overline{\text{CAS}}$	SDRAM column address strobe
$\overline{\text{WE}}$	SDRAM write strobe
$\overline{\text{S}}_0 - \overline{\text{S}}_1$	SDRAM chip select lines (Phys. banks 0 and 1)
CKE0 - CKE1	SDRAM clock enable lines
DQS0 - DQS8	SDRAM low data strobes
DM(0-8), DQS(9-17)	SDRAM low data masks, high data strobes (x4, 2 Phys. banks)
VDDID	VDD identification flag

Pin Name	Description
CK0 - CK2	SDRAM clock (positive lines of 3 differential pairs)
$\overline{\text{CK}}_0 - \overline{\text{CK}}_2$	SDRAM clock (negative lines of these three pairs)
SCL	IIC serial bus clock for EEPROM
SDA	IIC serial bus data line for EEPROM
SA0 - SA2	IIC slave address select for EEPROM
VDD*	SDRAM positive power supply
VDDQ*	SDRAM I/O Driver positive power supply
VREF	SDRAM I/O reference supply
VSS	Power supply return (ground)
VDDSPD	Serial EEPROM positive power supply (2.3 volts to 3.6 volts)--VDDSPD is not connected to VDD or VDDQ
NC	Spare pins (no connect)
TEST	Used by memory bus analysis tools (unused on memory DIMM)

*The VDD and VDDQ pins are tied to the single power-plane on these designs. See page 35.

3.2 Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0 - CK2	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs. All the DDR SDRAM addr/cntl inputs are sampled on the rising edge of their associated clocks.
$\overline{\text{CK0}} - \overline{\text{CK2}}$	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{\text{S0}}, \overline{\text{S1}}$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{\text{RAS}}, \overline{\text{CAS}}, \overline{\text{WE}}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, and $\overline{\text{WE}}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL2 inputs.
V_{DDQ}	Supply		Power supply for the DDR SDRAM output buffers to provide improved noise immunity. For all current DDR unbuffered DIMM designs, V_{DDQ} shares the same power plane as V_{DD} pins.
BA0,1	(SSTL)	—	Selects which SDRAM bank of four is activated.
A0 - A9 A10/AP, A11-A13	(SSTL)	—	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-12 defines the column address (CA0-CA12) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to precharge.
DQ0 - DQ63, CB0 - CB7	(SSTL)	—	Data and Check Bit Input/Output pins.
DM0-DM8	(SSTL)	Active High	Masks write data when high, issued concurrently with input data. Both DM and DQ have a write latency of one clock once the write command is registered into the SDRAM.
$V_{\text{DD}}, V_{\text{SS}}$	Supply		Power and ground for the DDR SDRAM input buffers, and core logic. V_{DD} and V_{DDQ} pins are tied to a single combined $V_{\text{DD}}/V_{\text{DDQ}}$ plane on these modules.
DQS0-DQS8	(SSTL)	Negative and Positive Edge	Data strobe for input and output data. For the x16, LDQS corresponds to the data on DQ0-7, UDQS corresponds to the data on DQ8-15.
SA0 - 2		—	These signals are tied at the system planar to either V_{SS} or V_{DD} to configure the serial SPD EEPROM address range.
SDA		—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pullup.
SCL		—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus line to V_{DD} to act as a pullup.
$V_{\text{DD SPD}}$	Supply		Power supply for SPD EEPROM. This supply is separate from the $V_{\text{DD}}/V_{\text{DDQ}}$ power plane. EEPROM supply is operable from 2.3 V to 3.6 V.

PC3200/PC2700 DDR SDRAM Unbuffered DIMM Design Specification

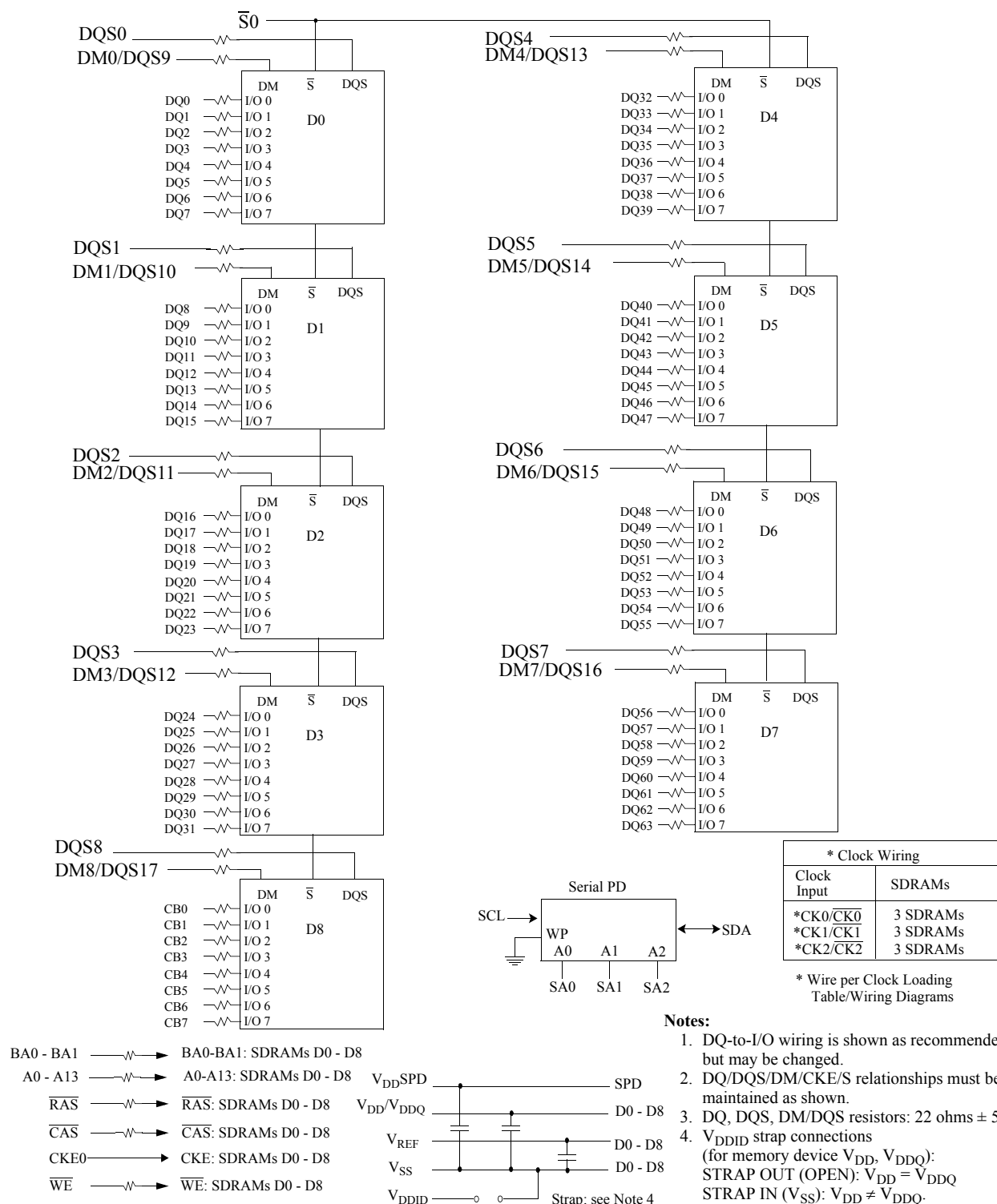
3. Architecture

3.3 184-Pin DDR SDRAM DIMM Pin Assignments

Front Side (left side 1 - 52, right side 53 - 92)			Back Side (left side 93 -144, right side 145 -184)			Front Side (left side 1 - 52, right side 53 - 92)			Back Side (left side 93 -144, right side 145 -184)		
Pin #	x64 Nonparity	x72 ECC	Pin #	x64 Nonparity	x72 ECC	Pin #	x64 Nonparity	x72 ECC	Pin #	x64 Nonparity	x72 ECC
1	VREF	VREF	93	VSS	VSS	48	A0	A0	140	NC	DM8, DQS17
2	DQ0	DQ0	94	DQ4	DQ4	49	NC	CB2	141	A10/AP	A10/AP
3	VSS	VSS	95	DQ5	DQ5	50	VSS	VSS	142	NC	CB6
4	DQ1	DQ1	96	VDDQ	VDDQ	51	NC	CB3	143	VDDQ	VDDQ
5	DQS0	DQS0	97	DM0, DQS9	DM0, DQS9	52	BA1	BA1	144	NC	CB7
6	DQ2	DQ2	98	DQ6	DQ6	KEY			KEY		
7	VDD	VDD	99	DQ7	DQ7	53	DQ32	DQ32	145	VSS	VSS
8	DQ3	DQ3	100	VSS	VSS	54	VDDQ	VDDQ	146	DQ36	DQ36
9	NC	NC	101	NC	NC	55	DQ33	DQ33	147	DQ37	DQ37
10	NC	NC	102	NC, TEST	NC, TEST	56	DQS4	DQS4	148	VDD	VDD
11	VSS	VSS	103	NC (FETEN)	NC (FETEN)	57	DQ34	DQ34	149	DM4, DQS13	DM4, DQS13
12	DQ8	DQ8	104	VDDQ	VDDQ	58	VSS	VSS	150	DQ38	DQ38
13	DQ9	DQ9	105	DQ12	DQ12	59	BA0	BA0	151	DQ39	DQ39
14	DQS1	DQS1	106	DQ13	DQ13	60	DQ35	DQ35	152	VSS	VSS
15	VDDQ	VDDQ	107	DM1, DQS10	DM1, DQS10	61	DQ40	DQ40	153	DQ44	DQ44
16	CK1	CK1	108	VDD	VDD	62	VDDQ	VDDQ	154	/RAS	/RAS
17	/CK1	/CK1	109	DQ14	DQ14	63	/WE	/WE	155	DQ45	DQ45
18	VSS	VSS	110	DQ15	DQ15	64	DQ41	DQ41	156	VDDQ	VDDQ
19	DQ10	DQ10	111	CKE1	CKE1	65	/CAS	/CAS	157	/S0	/S0
20	DQ11	DQ11	112	VDDQ	VDDQ	66	VSS	VSS	158	/S1	/S1
21	CKE0	CKE0	113	BA2	BA2	67	DQS5	DQS5	159	DM5, DQS14	DM5, DQS14
22	VDDQ	VDDQ	114	DQ20	DQ20	68	DQ42	DQ42	160	VSS	VSS
23	DQ16	DQ16	115	A12	A12	69	DQ43	DQ43	161	DQ46	DQ46
24	DQ17	DQ17	116	VSS	VSS	70	VDD	VDD	162	DQ47	DQ47
25	DQS2	DQS2	117	DQ21	DQ21	71	NC, /S2	NC, /S2	163	NC, /S3	NC, /S3
26	VSS	VSS	118	A11	A11	72	DQ48	DQ48	164	VDDQ	VDDQ
27	A9	A9	119	DM2, DQS11	DM2, DQS11	73	DQ49	DQ49	165	DQ52	DQ52
28	DQ18	DQ18	120	VDD	VDD	74	VSS	VSS	166	DQ53	DQ53
29	A7	A7	121	DQ22	DQ22	75	/CK2	/CK2	167	A13	A13
30	VDDQ	VDDQ	122	A8	A8	76	CK2	CK2	168	VDD	VDD
31	DQ19	DQ19	123	DQ23	DQ23	77	VDDQ	VDDQ	169	DM6, DQS15	DM6, DQS15
32	A5	A5	124	VSS	VSS	78	DQS6	DQS6	170	DQ54	DQ54
33	DQ24	DQ24	125	A6	A6	79	DQ50	DQ50	171	DQ55	DQ55
34	VSS	VSS	126	DQ28	DQ28	80	DQ51	DQ51	172	VDDQ	VDDQ
35	DQ25	DQ25	127	DQ29	DQ29	81	VSS	VSS	173	NC	NC
36	DQS3	DQS3	128	VDDQ	VDDQ	82	VDDID	VDDID	174	DQ60	DQ60
37	A4	A4	129	DM3, DQS12	DM3, DQS12	83	DQ56	DQ56	175	DQ61	DQ61
38	VDD	VDD	130	A3	A3	84	DQ57	DQ57	176	VSS	VSS
39	DQ26	DQ26	131	DQ30	DQ30	85	VDD	VDD	177	DM7, DQS16	DM7, DQS16
40	DQ27	DQ27	132	VSS	VSS	86	DQS7	DQS7	178	DQ62	DQ62
41	A2	A2	133	DQ31	DQ31	87	DQ58	DQ58	179	DQ63	DQ63
42	VSS	VSS	134	NC	CB4	88	DQ59	DQ59	180	VDDQ	VDDQ
43	A1	A1	135	NC	CB5	89	VSS	VSS	181	SA0	SA0
44	NC	CB0	136	VDDQ	VDDQ	90	NC	NC	182	SA1	SA1
45	NC	CB1	137	CK0	CK0	91	SDA	SDA	183	SA2	SA2
46	VDD	VDD	138	/CK0	/CK0	92	SCL	SCL	184	VDDSPD	VDDSPD
47	NC	DQS8	139	VSS	VSS						

NC = No Connect NU = Not Useable
 Note: The TEST pin is reserved for bus analysis probes and is not connected on normal memory module (DIMMs)

3.4 Block Diagram: Raw Card Version A, x72 (Populated as 1 physical bank of x8 DDR SDRAMs)

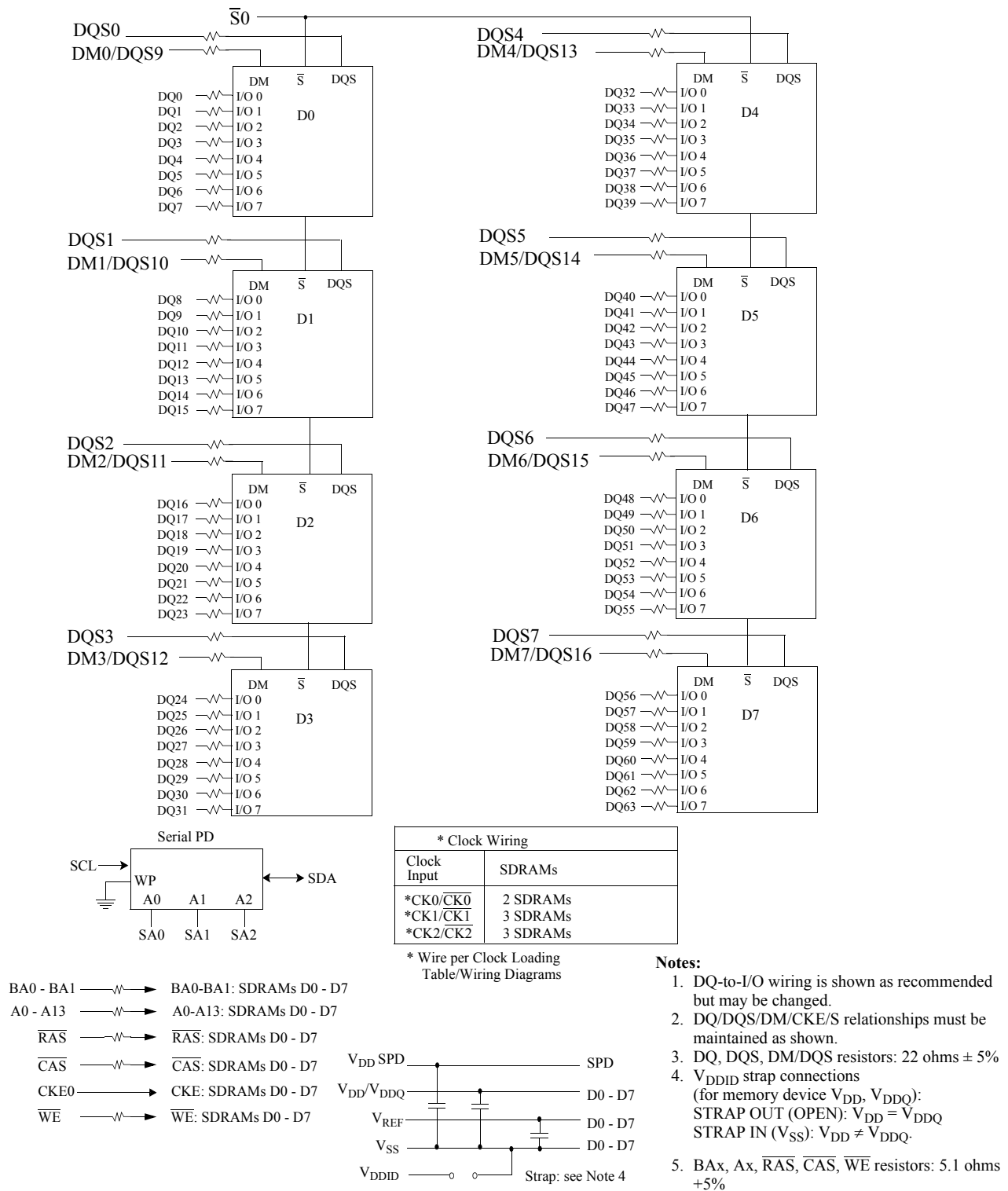


- Notes:**
1. DQ-to-I/O wiring is shown as recommended but may be changed.
 2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
 3. DQ, DQS, DM/DQS resistors: $22\ \text{ohms} \pm 5\%$.
 4. V_{DDID} strap connections
(for memory device V_{DD} , V_{DDQ}):
STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$.
 5. BA_x , A_x , $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors: $5.1\ \text{ohm} \pm 5\%$

PC3200/PC2700 DDR SDRAM Unbuffered DIMM Design Specification

3. Architecture

3.5 Block Diagram: Raw Card Version A, x64 (Populated as 1 physical bank of x8 DDR SDRAMs)



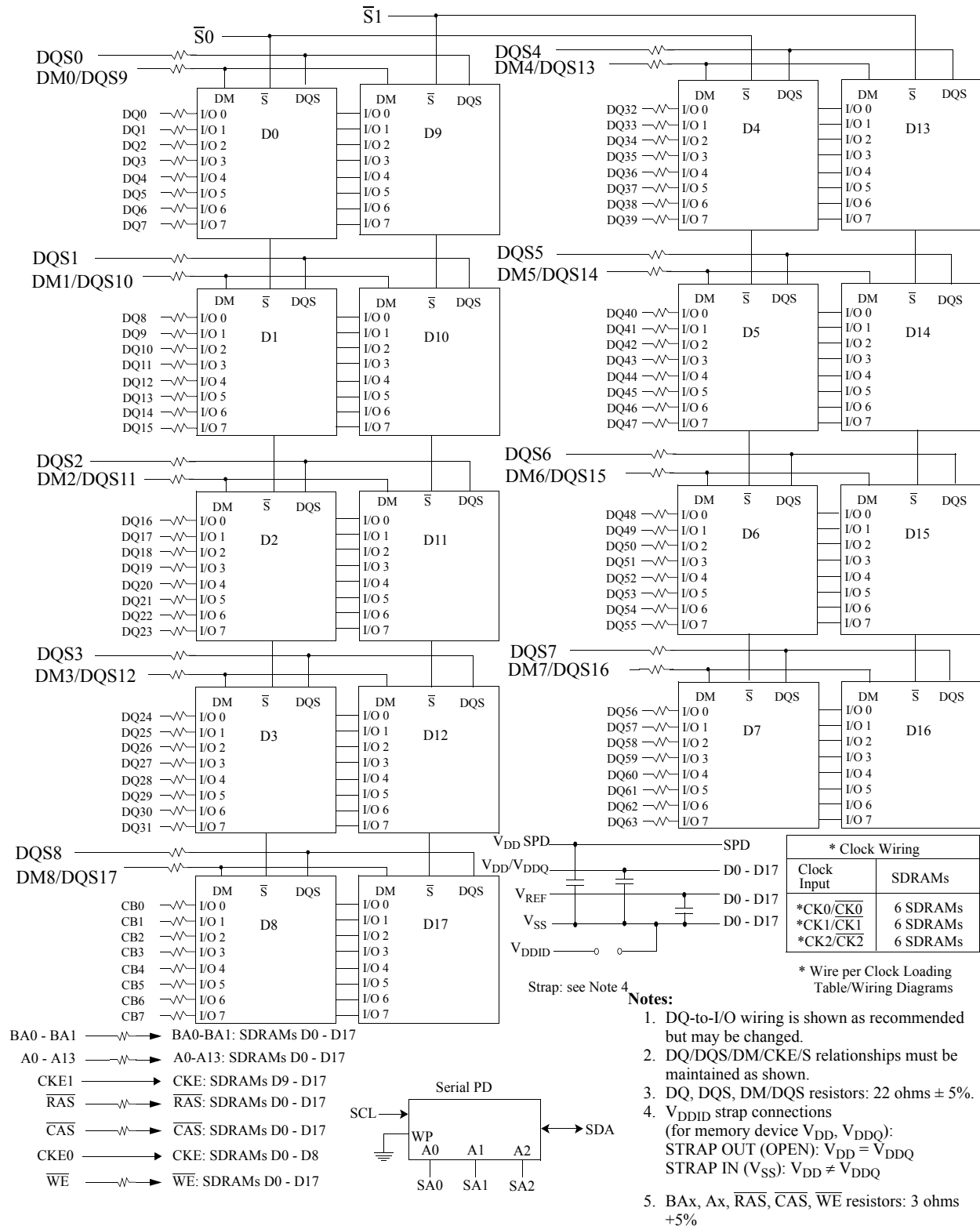
The diagram illustrates the DO-to-I/O wiring for the AD9080. It shows 16 differential pairs (DQ0-DQ15) connected to 32 I/O pins. Each pair is connected to a differential input/output (DM) and a single-ended input/output (DQS) pin. The wiring is organized into four groups of four pairs each, labeled DQ0-DQ7, DQ8-DQ15, DQ16-DQ23, and DQ24-DQ31. The diagram also shows the connection of VDD SPD, VDD/VDDQ, VREF, VSS, and VDDID to the device pins. A Serial PD block is shown with SCL and SDA pins, and a strap connection to VDDID. Notes indicate that the DO-to-I/O wiring is shown as recommended.

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: $22\ \text{ohms} \pm 5\%$.
4. V_{DDID} strap connections
(for memory device V_{DD} , V_{DDQ}):
STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$
5. BAx , Ax , $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors: $3\ \text{ohms} \pm 5\%$

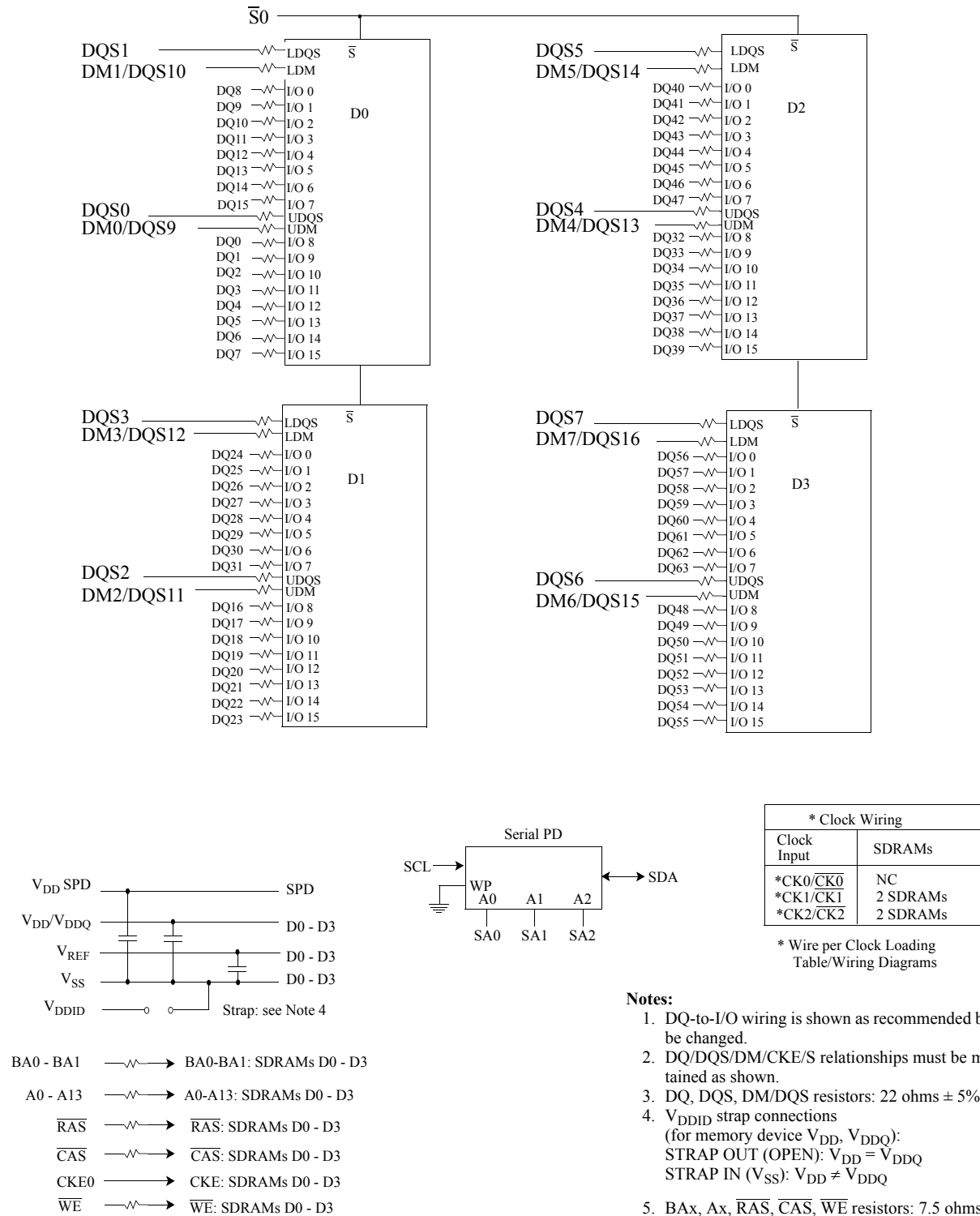
* Clock Wiring	
Clock Input	SDRAMs
*CK0/ $\overline{\text{CK0}}$	4 SDRAMs
*CK1/ $\overline{\text{CK1}}$	6 SDRAMs
*CK2/ $\overline{\text{CK2}}$	6 SDRAMs

* Wire per Clock Loading
Table/Wiring Diagrams

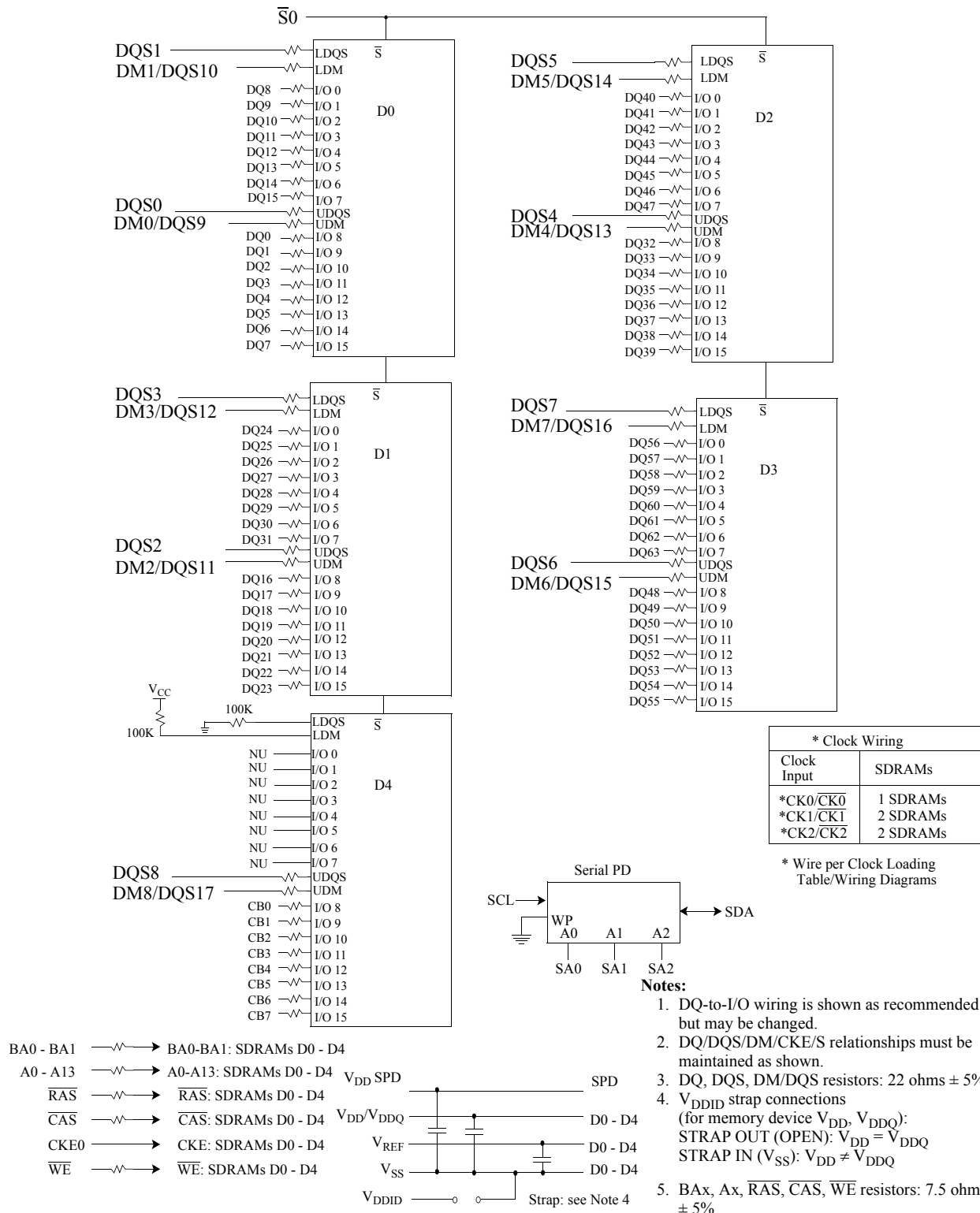
3.7 Block Diagram: Raw Card Version B, x72 (Populated as 2 physical banks of x8 DDR SDRAMs)



3.8 Block Diagram: Raw Card Version C, x64 (Populated as 1 physical bank of x16 DDR SDRAMs)



3.9 Block Diagram: Raw Card Version C, x72 (Populated as 1 physical bank of x16 DDR SDRAMs)



3.10 Logical Clock Net Structures

