

**4.20.9 - 100-Pin DDR SDRAM Unbuffered 32b-DIMM Design
Specification**

**DDR SDRAM Unbuffered 32b-DIMM
Reference Design Specification**

Revision 1.1

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1. Product Description

This reference specification defines the electrical and mechanical requirements for the 32b-DIMM DDR module. This is a 100-pin module supporting 100MHz, 133MHz, and 167Mhz clock (200, 266, 333 MT/s data rate) Double Data Rate (DDR) Synchronous DRAM. The data bus is 32-bits wide with no ECC support and the address is unbuffered. The 32b-DIMM DDR module is intended for use in embedded applications.

Reference design examples are included which provide an initial basis for 32b-DIMM designs. Any modifications to these reference designs must meet all system timing, signal integrity and thermal requirements for 167 MHz clock rate support. Other designs are acceptable, and all 32b-DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

Product Family Attributes

Attribute:	Values:	Notes:
32b-DIMM Organization	x 32,	
32b-DIMM Dimensions (nominal)	30.48 mm high, 90.19 mm wide for raw card B, C and E 25.4 mm high, 90.19 mm wide for raw card A and D	
32b-DIMM Types Supported	Unbuffered	
Pin Count	100	
DDR SDRAMs Supported	64 Mb, 128 Mb, 256 Mb, 512 Mb	
Capacity	32 MB, 64 MB, 128 MB, 256 MB, 512 MB	
Serial Presence Detect	Consistent with JEDEC 21-C Appendix D Release 11	
Voltage Options	2.5 V V_{DD} 2.5 V V_{DDQ}	1
Interface	SSTL_2	
Note 1: $V_{DD}SPD$ is tied to V_{DD} or V_{DDQ} on the DDR 32b-DIMM .		

2. Environmental Requirements

DDR SDRAM unbuffered 32b-DIMMs are intended for standard office environments that have limited capability for heating and air conditioning.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
T _{OPR}	Operating Temperature (ambient)	0 to +65	°C	1
H _{OPR}	Operating Humidity (relative)	10 to 90	%	1
T _{STG}	Storage Temperature	-50 to +100	°C	1
H _{STG}	Storage Humidity (without condensation)	5 to 95	%	1
	Barometric Pressure (operating & storage)	105 to 69	kPa	1, 2
1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. 2. Up to 9850 ft.				

3. Architecture

Pin Description

CK(0:1)	Clock Inputs, positive line	2	DQ(0:31)	Data Input/Output	32
$\overline{\text{CK}}$ (0:1)	Clock inputs, negative line	2			
CKE(0:1)	Clock Enables	2	DM(0:3)	Data Masks	4
$\overline{\text{RAS}}$	Row Address Strobe	1	DQS(0:3)	Data strobes	4
$\overline{\text{CAS}}$	Column Address Strobe	1			
$\overline{\text{WE}}$	Write Enable	1			
$\overline{\text{S}}$ (0:1)	Chip Selects	2	V _{DD}	Core and I/O Power	14
A(0:9,11:13)	Address Inputs	13	V _{SS}	Ground	14
A10/AP	Address Input/Autoprecharge	1	V _{REF}	Input/Output Reference	1
BA(0:1)	SDRAM Bank Address	2			
SCL	Serial Presence Detect (SPD) Clock Input	1			
SDA	SPD Data Input/Output	1			
SA0	SPD address	1	DU	Reserved for future use	1
				Total:	100

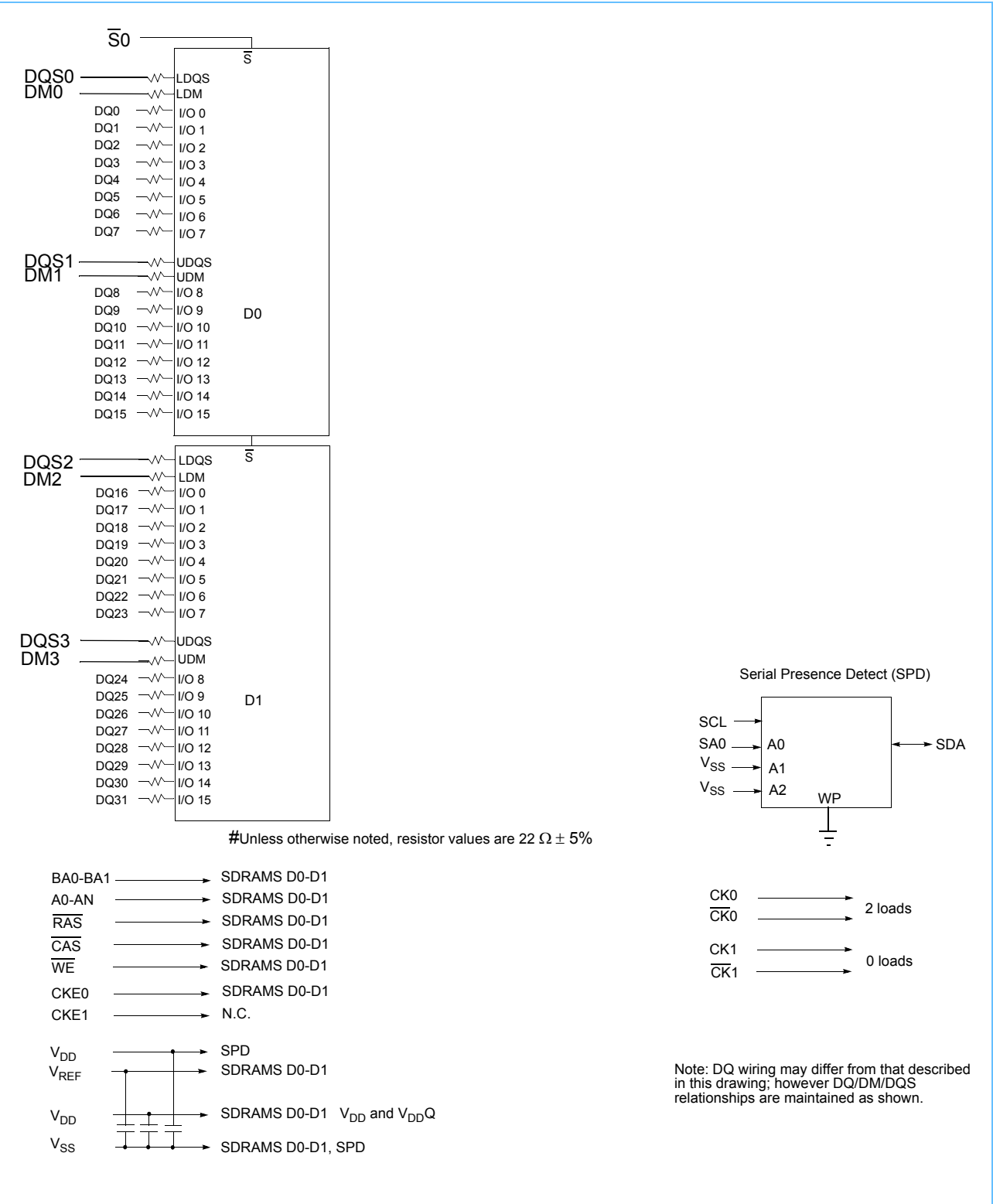
Input/Output Functional Description

Symbol	Type	Polarity	Function
$\overline{CK0} - \overline{CK1}, \overline{CK0} - \overline{CK1}$	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of CK. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE0, CKE1	Input	Active High	Activates the DDR SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S0}, \overline{S1}$	Input	Active Low	Enables the associated DDR SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Physical Bank 0 is selected by $\overline{S0}$; Bank 1 is selected by $\overline{S1}$.
$\overline{RAS}, \overline{CAS}, \overline{WE}$	Input	Active Low	When sampled at the cross point of the rising edge of CK and falling edge of CK, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the DDR SDRAM.
BA0 - BA1	Input	—	Selects which DDR SDRAM bank of four is activated.
A0 - A9, A11-A13, A10/AP	Input	—	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of CK. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of CK. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, then BA0 and BA1 are used to define which bank to precharge.
DQ0 - DQ31	In/Out	—	Data Bit Input/Output pins.
DM0 - DM3	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS0 - DQS3	In/Out	—	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR SDRAMs and is sent at the leading edge of the data window.
V_{DD}, V_{SS}	Supply	—	Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
SDA	In/Out	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected to V_{DD} to act as a pull up.
SCL	Input	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to V_{DD} to act as a pull up.
SA0	Input	—	Address pin used to select the Serial Presence Detect.

DDR SDRAM 32b-DIMM Pinout

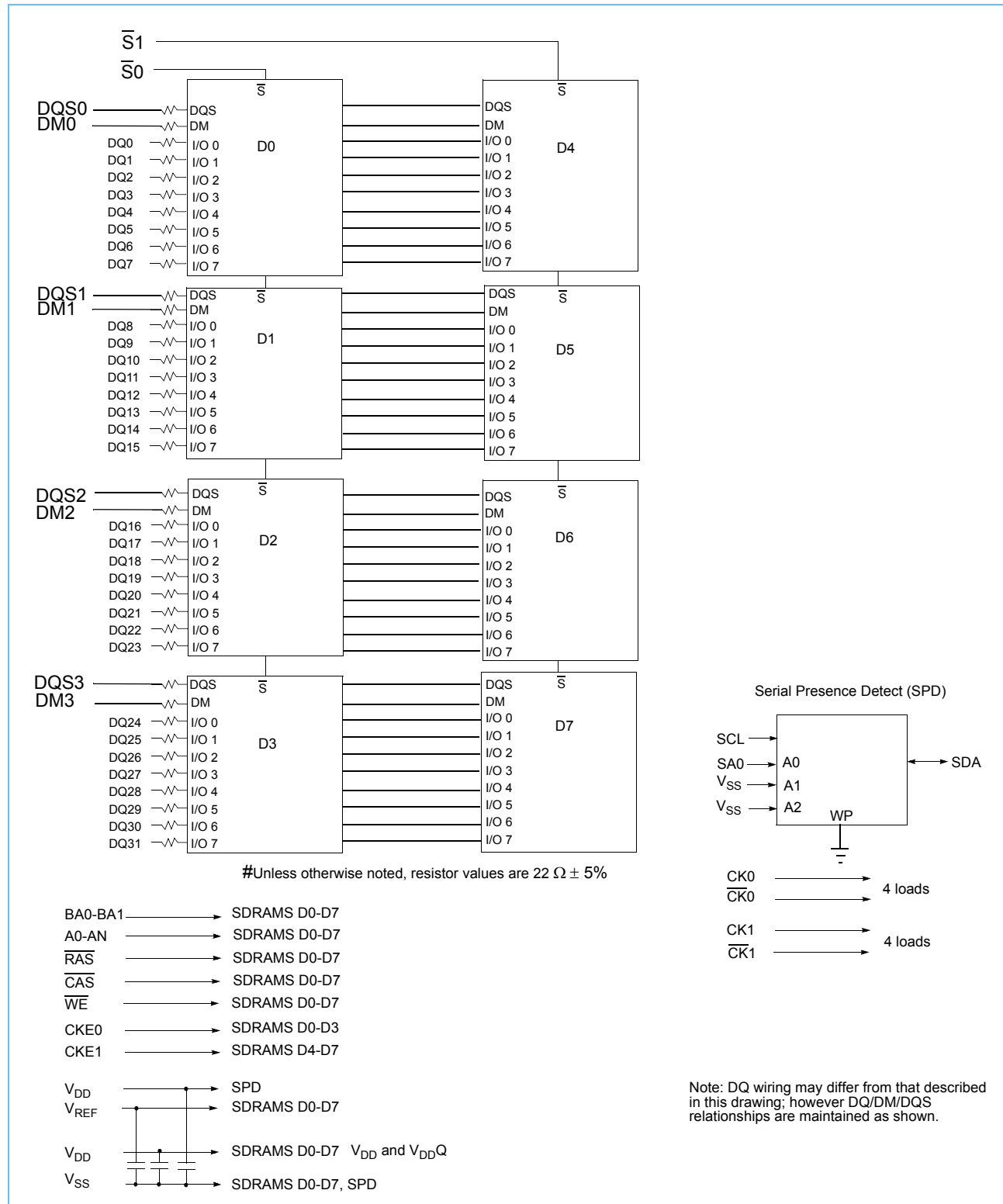
Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	DQ0	51	DQ4	26	A5	76	A2
2	V _{SS}	52	V _{SS}	27	A3	77	A0
3	DQ1	53	DQ5	28	A1	78	BA1
4	DQS0	54	DM0	29	A10	79	$\overline{\text{RAS}}$
5	V _{DD}	55	V _{DD}	30	V _{DD}	80	V _{DD}
6	DQ2	56	DQ6	31	BA0	81	$\overline{\text{CAS}}$
7	DQ3	57	DQ7	32	$\overline{\text{WE}}$	82	$\overline{\text{S1}}$
8	V _{DD}	58	V _{DD}	33	$\overline{\text{S0}}$	83	A13
9	DQ8	59	DQ12	34	DQ16	84	DQ20
10	DQ9	60	DQ13	35	V _{SS}	85	V _{SS}
11	V _{SS}	61	V _{SS}	36	DQ17	86	DQ21
12	DQS1	62	DM1	37	DQS2	87	DM2
13	DQ10	63	DQ14	38	V _{DD}	88	V _{DD}
14	V _{DD}	64	V _{DD}	39	DQ18	89	DQ22
15	DQ11	65	DQ15	40	DQ19	90	DQ23
16	V _{SS}	66	V _{SS}	41	V _{DD}	91	V _{DD}
17	CK0	67	CK1	42	DQ24	92	DQ28
18	$\overline{\text{CK0}}$	68	$\overline{\text{CK1}}$	43	DQ25	93	DQ29
19	V _{DD}	69	V _{DD}	44	V _{SS}	94	V _{SS}
20	CKE1	70	CKE0	45	DQS3	95	DM3
21	A12	71	A11	46	DQ26	96	DQ30
22	NC	72	A8	47	V _{SS}	97	V _{SS}
23	A9	73	A6	48	DQ27	98	DQ31
24	A7	74	A4	49	SA0	99	SDA
25	V _{SS}	75	V _{SS}	50	V _{REF}	100	SCL

Block Diagram: Raw Card Version A
(Populated as 1 physical bank of x16 DDR SDRAMs on a 6 layered PCB)



Block Diagram: Raw Card Version B

(Populated as 2 physical banks of x8 DDR SDRAMs on a 6 layered PCB)



Block Diagram: Raw Card Version C

(Populated as 1 physical bank of x8 DDR SDRAMs on a 6 layered PCB)

