

4.3 Two Byte Modules & Cards

4.3.1 – 76 PIN ZIP/SIMM SRAM MODULE

CAPACITY—2 X 64K, 2 X 256K, 2 X 1M WORDS OF 9 BITS
CONFIGURATION—DUAL BANK MODULE USING DEVICES WITH 64K, 256K, OR 1M WORDS—
SELECTABLE AS 64K, 256K, OR 1M BY 18
128K, 512K, OR 2M BY 9
LOGIC FEATURE—2 SEPARATELY CONTROLLABLE BITS FOR USE AS PARITY BITS
PACKAGE—76 PIN SIP MODULE WITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4.3-1

4.3.2 – 40 PIN SIP/SIMM DRAM MODULE FAMILY

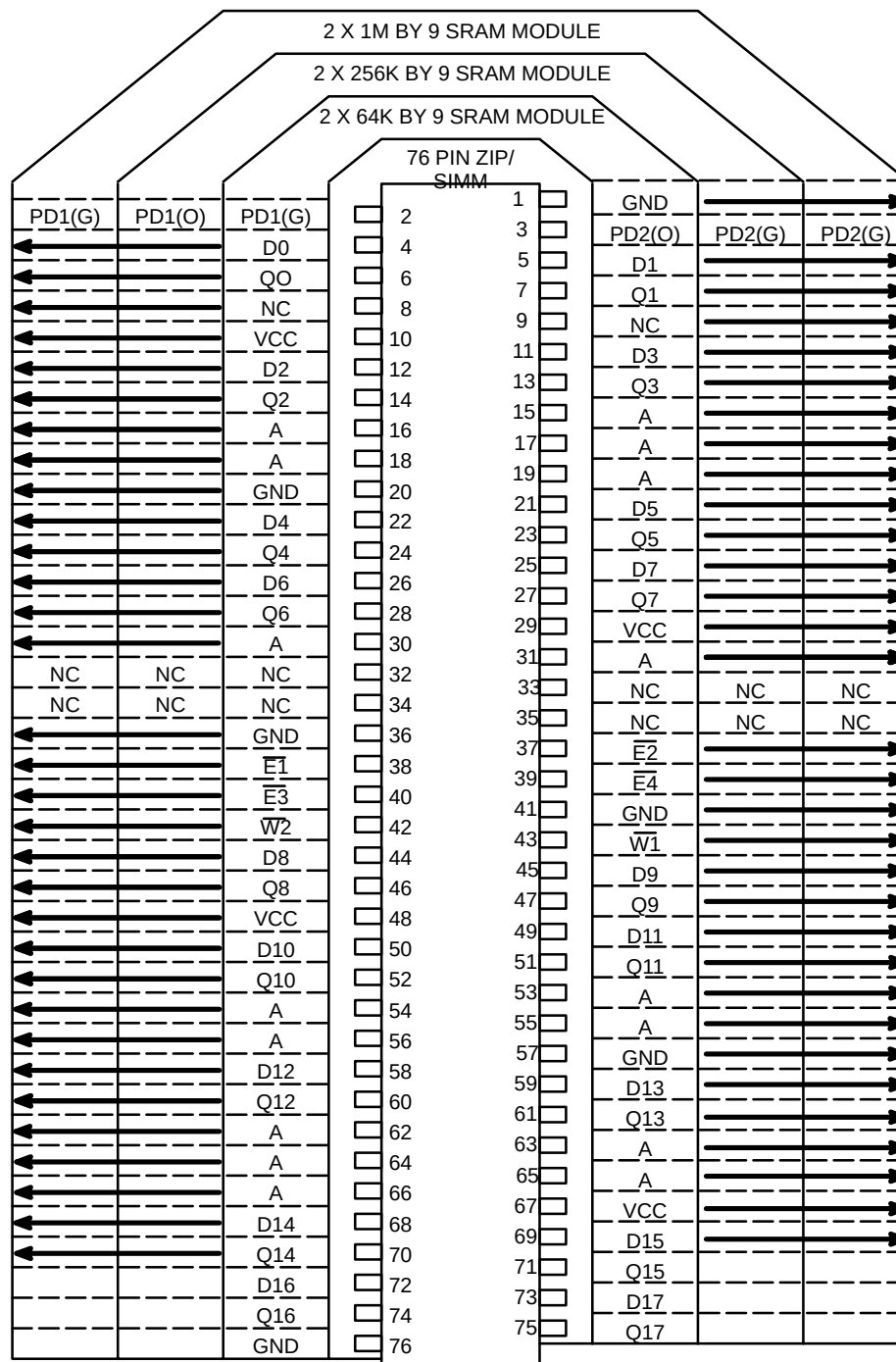
CAPACITY —64K TO 4M WORDS OF 16 OR 18 BITS
—64K TO 8M WORDS OF 8 OR 9 BITS
—128K TO 16M WORDS OF 4 BITS
—256K TO 32M WORDS OF 2 BITS
—512K TO 64M WORDS OF 1 BIT
CONFIGURATION—ONE OR TWO SIDED,
—USING 64K, 256K, 1M, OR 4M DEVICES
PACKAGE—40 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4.3-2

4.3.3 – 60 PIN DRAM CARD FAMILY

CAPACITY—512K, 1M, 2M, 4M, & 8M WORDS OF 16 OR 18 BITS
CONFIGURATION—SEVEN DIFFERENT CONFIGURATIONS
—USING 1Mb & 4Mb DEVICES AND WITH 1, 2, OR 4 RE CLOCKS.
LOGIC FEATURES, The cards contain a “PRESENCE DETECT” feature which consists of output pins which supply an encoded value which defines the storage capacity, configuration, and speed of the card.
PACKAGE—60 PIN JEDEC MEMORY CARD
PIN ASSIGNMENTS—Fig. 4.3-3A
CONFIGURATION BLOCK DIAGRAMS—Fig. 4.3-3B

4.3.4 – 68 PIN MULTIPLE TECHNOLOGY MEMORY CARD FAMILY

CAPACITY—UP TO 32M WORDS OF 16 BITS
CONFIGURATION—ONE BASIC CONFIGURATION that allows the use of SRAM, EEPROM, EPROM, or ROM memory devices with software or firmware control to accommodate the device characteristic differences.
LOGIC FEATURES,
—The card contains an internal MEMORY called the “ATTRIBUTE MEMORY”; the contents describe the hardware and software characteristics, and use of the card.
—The card contains a “PRESENCE DETECT” feature which consists of output pins which supply an encoded value which defines the storage capacity, configuration, and speed of the card.
PACKAGE—68 PIN JEDEC MEMORY CARD
PIN ASSIGNMENTS—Fig. 4.3-4A
MEMORY CARD OPERATION TRUTH TABLE— Page 4.3-4B
MEMORY CARD SPECIFIC TERMINOLOGY— Sec. 2.8, Page 2-13



The PD(n) pins are connected to GND (G) or left optn (O).

E1 & W1 CONTROL Q0, Q2, Q4, Q6, Q10, Q12, Q14, Q16
E2 & W1 CONTROL Q1, Q3, Q5, Q7, Q11, Q13, Q15, Q17
E3 & W2 CONTROL Q8
E4 & W2 CONTROL Q9

FIGURE 4.3-1

2 X 64K TO 1M BY 9, 76 PIN SRAM MODULE FAMILY

Release 1-7