

4.4.3 – 88 PIN DRAM CARD FAMILIES

NOTE: There are two versions of this Card, shown in Figure 4.4.3-1 describing X 32 & 36/39 configurations, & 4.4.3-2 describing a X 40 configuration. They are similar but not fully compatible. Caution should be exercised in using these standards.

CAPACITY—256K TO 128M WORDS OF 32, 36, 39 OR 40 BITS

CONFIGURATION—16 Different Configurations Using 1mb, 4mb, 16mb, 64mb, & 256mb Devices
And With 2, Or 4 $\overline{R_e}$ Clocks.

LOGIC FEATURES—The cards may be used with DATA BUS widths of X16/18 or X32/36 or X39— The cards contain a “PRESENCE DETECT” feature which consists of output pins which supply an encoded value which defines the storage capacity, configuration, and speed of the card.

PIN ASSIGNMENTS, 32, 36, & 39 bit—Fig. 4.4.3-1 A

PRESENCE DETECT TABLE 32, 36, & 39 bit—Fig. 4.4.3-1 B

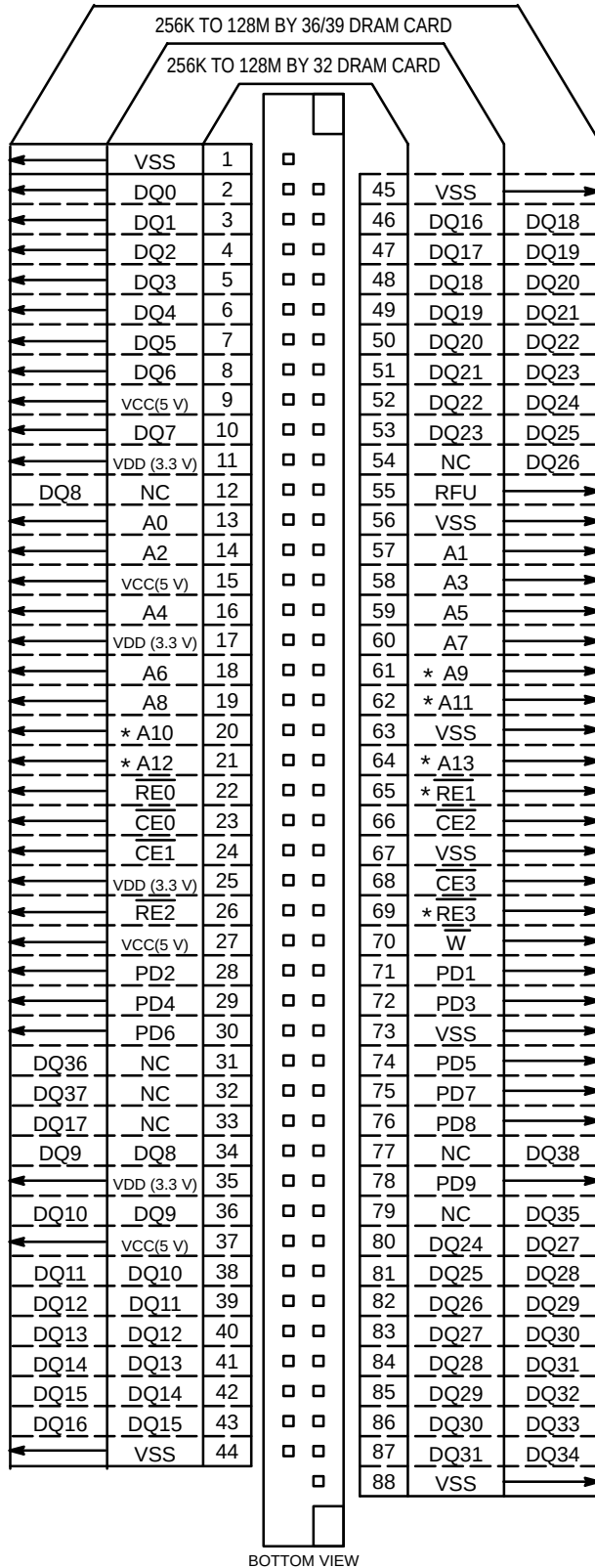
CONFIGURATION BLOCK DIAGRAMS 32, 36, & 39 bit—Figs. 4.4.3-1 C, 4.4.3-1 D, 4.4.3-1 E, & 4.4.3-1 F

PIN ASSIGNMENTS, 40 bit—Fig. 4.4.3-2 A

PRESENCE DETECT TABLE 40 bit—Fig. 4.4.3-2 B

CONFIGURATION BLOCK DIAGRAMS 40 bit—Figs. 4.4.3-2 C, 4.4.3-2 D, 4.4.3-2 E, & 4.4.3-2 F

PACKAGE—88 PIN JEDEC MEMORY CARD



	PD7	PD6
SPEED (tRAC)	75	30
100 nS	VSS	VSS
80 nS	VSS	NC
70 nS	NC	VSS
60 nS	NC	NC
50 nS	VSS	VSS

PD SPEED TABLE

	PIN NUMBER						
CONFIGURATION	20	21	61	62	64	65	69
256K X 36, 2 RE	NC	NC	NC	NC	NC	NC	NC
512K X 36, 4 RE	NC	NC	NC	NC	NC	RE1	RE3
1M X 36, 2 RE	NC	NC	A9	NC	NC	NC	NC
2M X 36, 4 RE	NC	NC	A9	NC	NC	RE1	RE3
4M X 36, 2 RE	A10	NC	A9	A11	NC	NC	NC
8M X 36, 4 RE	A10	NC	A9	A11	NC	RE1	RE3
16M X 36, 2 RE	A10	A12	A9	A11	NC	NC	NC
32M X 36, 4 RE	A10	A12	A9	A11	NC	RE1	RE3
64M X 36, 2 RE	A10	A12	A9	A11	A13	NC	NC
128M X 36, 4 RE	A10	A12	A9	A11	A13	RE1	RE3

ADDRESS AND CLOCK PIN ASSIGNMENTS

Data Access Mode	PD9
FAST PAGE	NC
EDO	VSS

* SEE TABLE FOR FUNCTION ASSIGNMENTS FOR THESE PINS
AS A FUNCTION OF CARD CAPACITY AND CONFIGURATION

FIGURE 4.4.3-1 A
88 PIN, BY 32 and 36/39 DRAM CARD PINOUT

PD BITS 5 4 3 2 1	CARD DENSITY	DRAM ORGANIZATION	CARD ADDR. REQ'D	RE ADDR.	CE ADDR.	AVAIL. PAGE DEPTH	AVERAGE REFRESH INTERVAL	NOTES
1 1 1 1 1	NO CARD							NO CARD INSTALLED
1 0 0 0 0 0 0 0 0 0	1 MB 2 MB	256K X 1, 4, 16, 18 256K X 1, 4, 16, 18	18 18	9 9	9 9	512 512	125 ms 125 ms	
1 0 0 0 1 0 0 0 0 1	2 MB 4 MB	512K X 8, 9 512K X 8, 9	19 19	10 10	9 9	512 512	125 ms 125 ms	
1 0 0 1 0 0 0 0 1 0 1 1 0 1 0 0 1 0 1 0	4 MB 8 MB 4 MB 8 MB	1M X 1, 4, 16, 18 1M X 1, 4, 16, 18 1M X 16, 18 1M X 16, 18	20 20 20 20	10 10 12 12	10 10 8 8	1024 1024 256 256	125 ms 125 ms 62 ms 62 ms	
1 0 0 1 1 0 0 0 1 1	8 MB 16 MB	2M X 8, 9 2M X 8, 9	21 21	11 11	10 10	1024 1024	125 ms 125 ms	
1 0 1 0 0 0 0 1 0 0	16 MB 32 MB	4M X 1, 4, 16, 18 4M X 1, 4, 16, 18	22 22	12 12	*11 *11	**1024 **1024	62 ms 62 ms	SUPPORT 12/10 AND 11/11 ADDRESS SUPPORT 12/10 AND 11/11 ADDRESS
1 0 1 0 1 0 0 1 0 1	32 MB 64 MB	8M X 8, 9 8M X 8, 9	23 23	13 13	*11 *11	**1024 **1024	62 ms 62 ms	SUPPORT 13/10 AND 12/11 ADDRESS SUPPORT 13/10 AND 12/11 ADDRESS
1 0 1 1 0 0 0 1 1 0	64 MB 128MB	16M X 1, 4, 16, 18 16M X 1, 4, 16, 18	24 24	14 14	*11 *11	**1024 **1024	31 ms 31 ms	SUPPORT 13/11 AND 14/10 ADDRESS SUPPORT 13/11 AND 14/10 ADDRESS

* INDICATES REDUNDANT ADDRESS THAT MUST BE PROVIDED AT CE1 TIME (TO ALLOW USE OF MIXED DRAM ADDRESSING)

** PAGE DEPTH DETERMINED BY THE SMALLEST CE1 ADDRESS DRAM

*** ALL DENSITIES ASSUME 4 BYTE CARD DATA WIDTH (32 OR 36 BITS)
FOR THE PDn PINS, 1 = NC, 0 = VSS

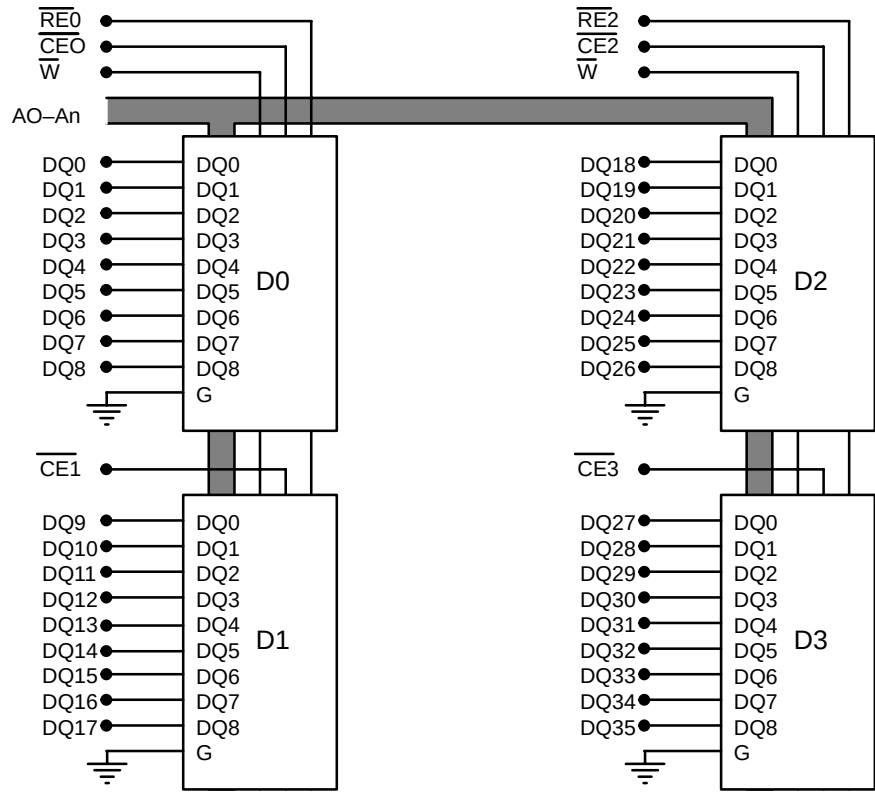
MEMORY CARD ORGANIZATION AND ADDRESS STRUCTURE

BASE DEVICE	CONFIG'N	PIN NUMBER							
		9	11	15	17	25	27	35	37
1M	256K X 36, 2 RE	5 V	NC	5 V	NC	NC	5 V	NC	5 V
1M	512K X 36, 4 RE	5 V	NC	5 V	NC	NC	5 V	NC	5 V
4M	1M X 36, 2 RE	5 V, NC	NC, 3.3 V	5 V, NC	NC, 3.3 V	NC, 3.3 V	5 V, NC	NC, 3.3 V	5 V, NC
4M	2M X 36, 4 RE	5 V, NC	NC, 3.3 V	5 V, NC	NC, 3.3 V	NC, 3.3 V	5 V, NC	NC, 3.3 V	5 V, NC
16M	4M X 36, 2 RE	5 V, NC	NC, 3.3 V	5 V, NC	NC, 3.3 V	NC, 3.3 V	5 V, NC	NC, 3.3 V	5 V, NC
16M	8M X 36, 4 RE	5 V, NC	NC, 3.3 V	5 V, NC	NC, 3.3 V	NC, 3.3 V	5 V, NC	NC, 3.3 V	5 V, NC
64M	16M X 36, 2 RE	NC	3.3 V	NC	3.3 V	3.3 V	NC	3.3 V	NC
64M	32M X 36, 4 RE	NC	3.3 V	NC	3.3 V	3.3 V	NC	3.3 V	NC
256M	64M X 36, 2 RE	NC	3.3 V	NC	3.3 V	3.3 V	NC	3.3 V	NC
256M	128M X 36, 4 RE	NC	3.3 V	NC	3.3 V	3.3 V	NC	3.3 V	NC

VDD POWER PIN ASSIGNMENT TABLE

FIGURE 4.4.3-1 B
88 PIN, BY 32 AND 36/39 DRAM CARD CONFIGURATION TABLES
Release 6-7

BLOCK DIAGRAM for 512K /2M/8M/32M X 36 or 1M/4M/16M/64M X 18
USING X8 or X9 DRAM



WORD ORGANIZATION	* BASE MEMORY DEVICE	
	D0 – D3	ADDRESS
512K X 36 or 1M X 18	4M (X9)	A0 – A9
2M X 36 or 4M X 18	16M (X9)	A0 – A10
8M X 36 or 16M X 18	64M (X9)	A0 – A12

* NOTE: The BASE MEMORY DEVICE columns give the total device capacity in bits and the data interface configuration

note 1: In an 18 bus system, RE0 and RE2 will be controlled independently and the data bus will be connected to for an 18 bit bus outside the card
In a 36 bit system, RE0 and RE2 will be actuated simultaneously
note 2: The card contains 4 bytes of data; 2 byte operation is allowed.

FIGURE 4.4.3-1 C
88 PIN, BY 36, DRAM CARD 1 BANK USING BY 9 DEVICES