

4.4.6 – 112 PIN MPDRAM DIMM FAMILY

CAPACITY—256K, and 512K WORDS OF 32 BITS ON THE SERIAL AND PARALLEL PORTS.

DATA CONFIGURATIONS—Two DEVICE configurations are defined: using X8 and X16 MPDRAM

CONFIGURATION—2 Different Configurations are defined using X4 & X8 memories with 2 banks.

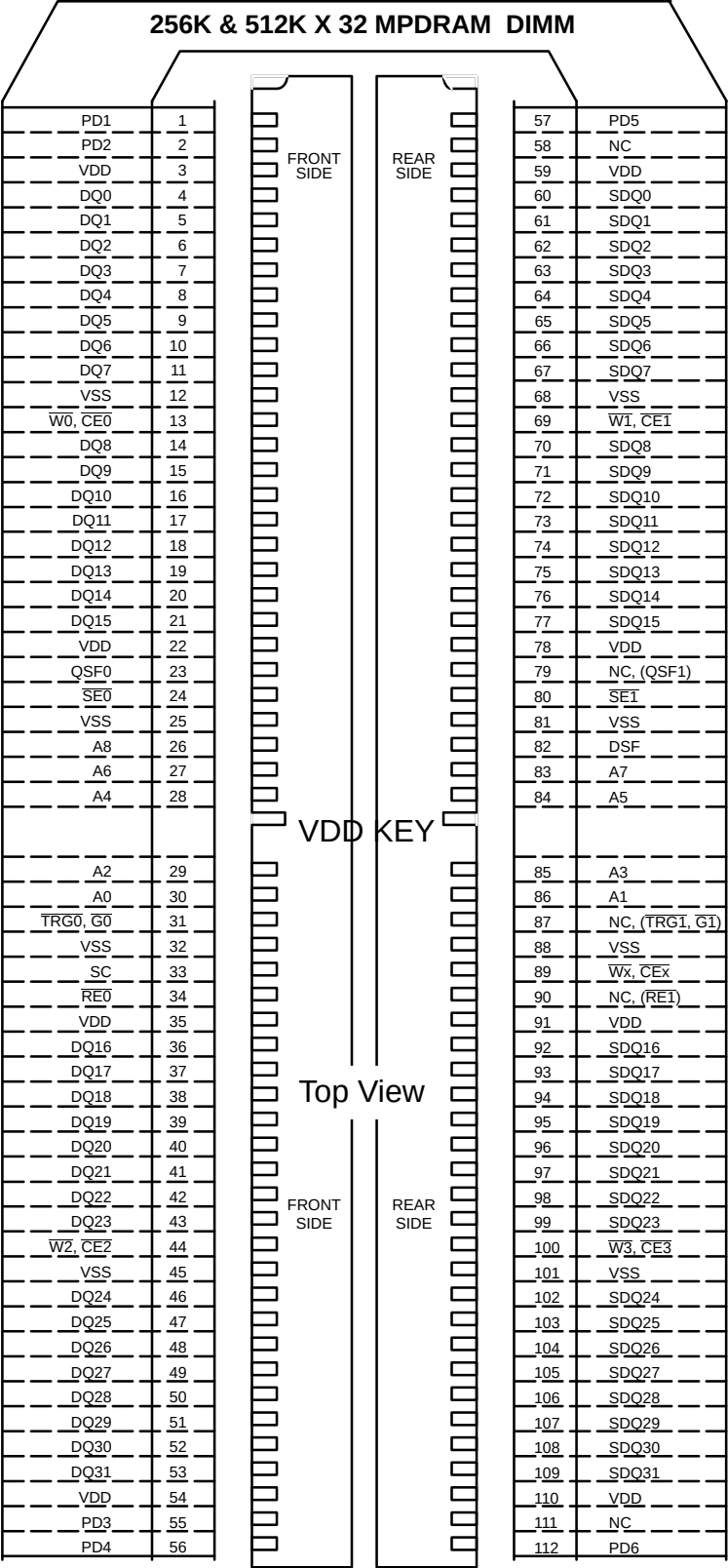
LOGIC FEATURES—The modules contain independent clock control of the 4 separate BYTE groups of data bits and “PRESENCE DETECT” features that consists of output pins in the PDn field which supplies encoded values that define the storage capacity, SAM length, read mode, refresh mode, $\overline{CE}/\overline{W}$ logic configuration, and speed of the module.

PACKAGE—112 PIN JEDEC DIMM MEMORY MODULE

PIN ASSIGNMENTS AND PD TABLES—Figs. 4.4.6-A

PRESENCE DETECT TABLES—Fig. 4.4.6-B

CONFIGURATION BLOCK DIAGRAM—Figs. 4.4.6-B & 4.4.6-C



NOTE: Pin functions in ()
may be re;quired on certain
2-bank 512K X 32 module
implementations

FIGURE 4.4.6-A
256K & 512K MPDRAM DIMM