

■ 4.5.12 – 184 PIN DIMM FAMILY SUPPLEMENTARY DESIGN STANDARDS

BACKGROUND INFORMATION: The 184 Pin DIMM Module family consists of numerous configurations using SDR and DDR SDRAM devices. These consist of Unbuffered, and Registered designs. Complete Standards for Unbuffered SDR and Unregistered DDR devices have been published in chapter 4.5 of this Standard. Additional Buffered and Registered DIMMs can be achieved using the same pinouts with the addition of a few supplementary signals to control the buffering and registering functions.

This section contains standards defining various aspects of additional 184P DIMM configurations.

The contents of this Section are as follows:

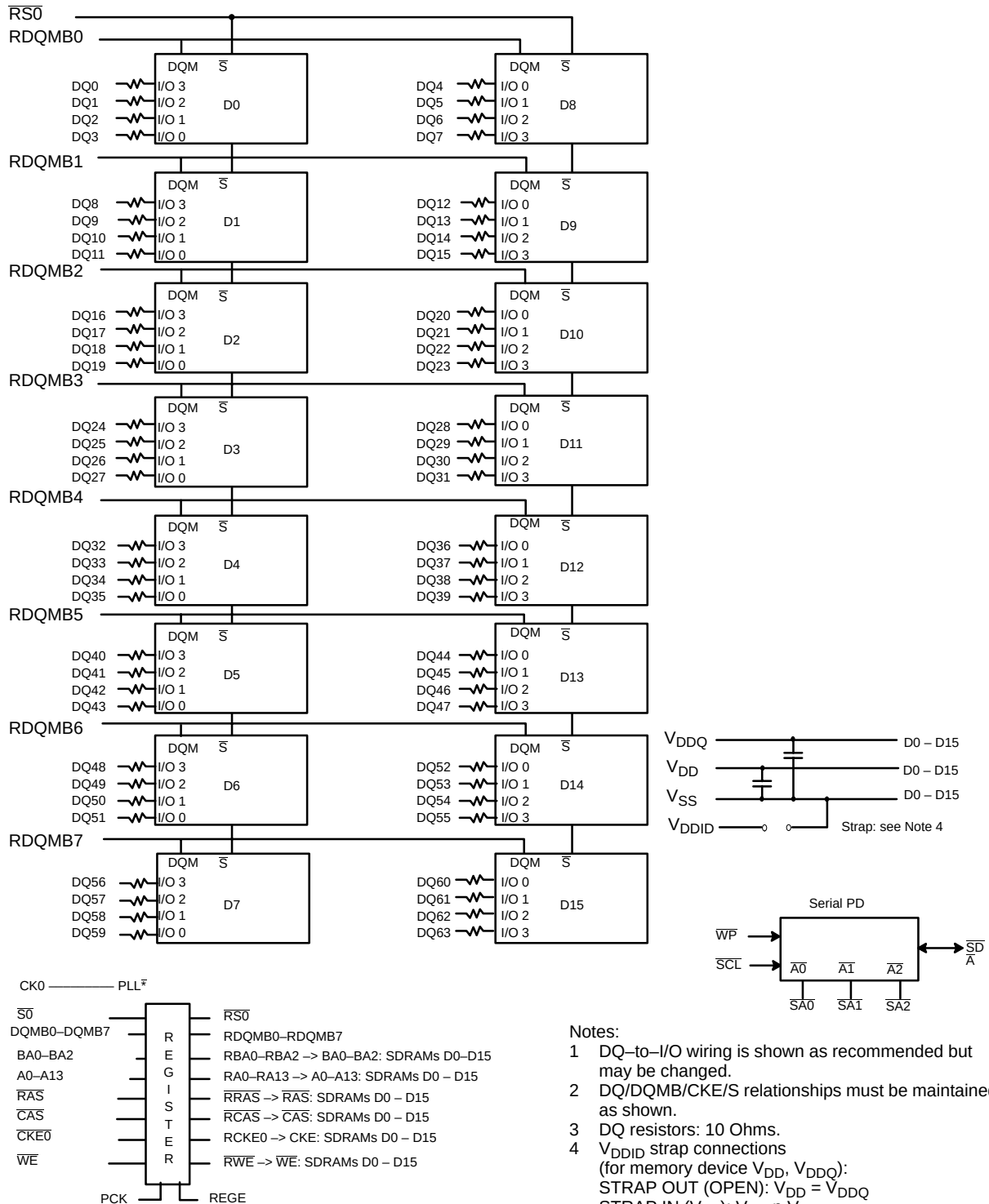
Section 1 gives a series of 18 **Block Diagrams** for an SDR Registered DIMM sub-family.

Section 2 contains **Clock Topology** layouts for DDR Registered DIMM and DDR Unbuffered DIMM.

Section 3 contains a **PINOUT** for the DDR Registered DIMM member of the family.

4.5.12.1 – 184 PIN SDR Registered DIMM Block Diagrams

CONFIGURATION BLOCK DIAGRAM—Figs. 4.5.12-A through 4.5.12-P



[†]Wire per Clock Loading Table/Wiring Diagrams

FIGURE 4.5.12-A
184 PIN X64 SDR REGISTERED SDRAM DIMM (1 BANK, X4 SDR SDRAMs)

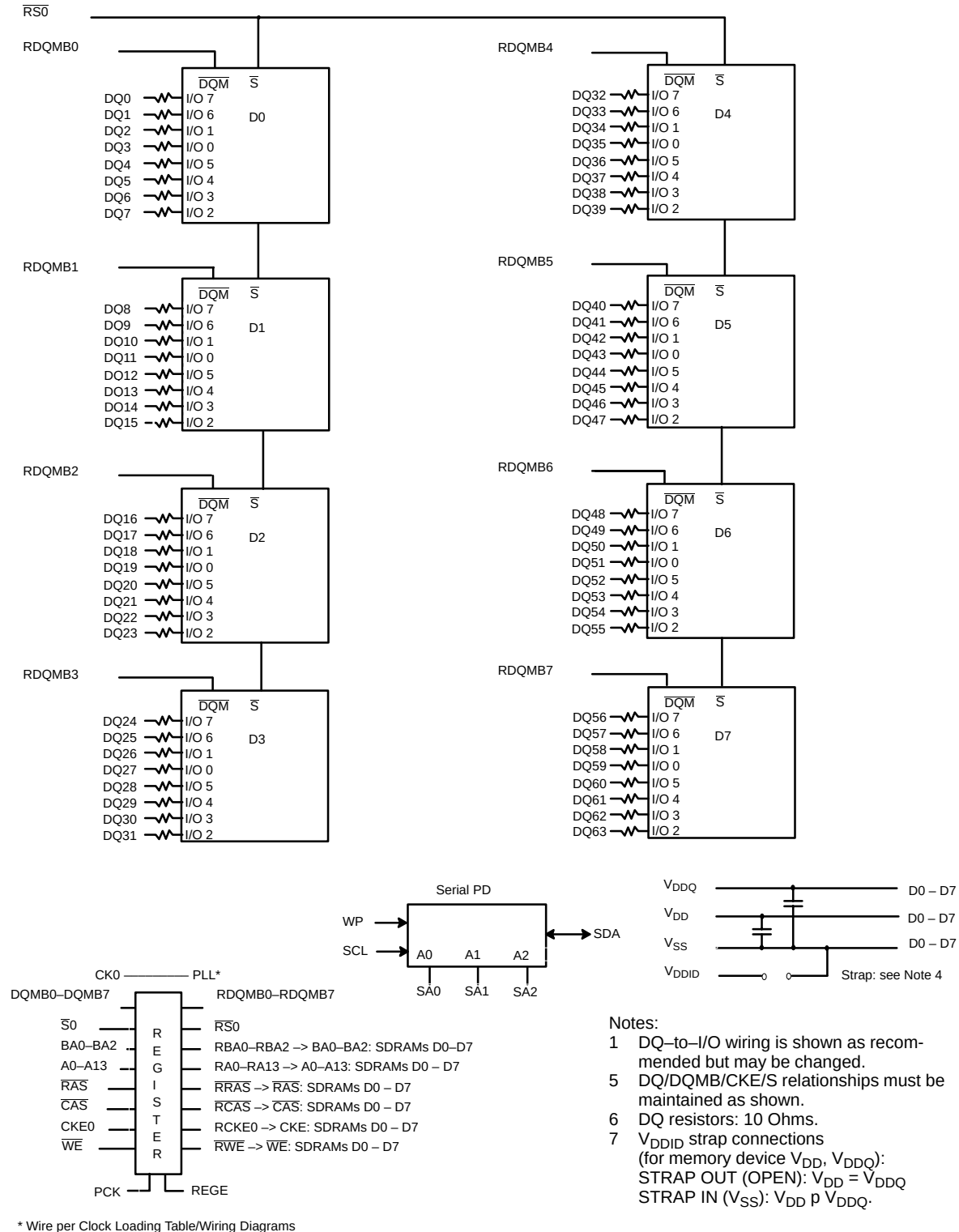
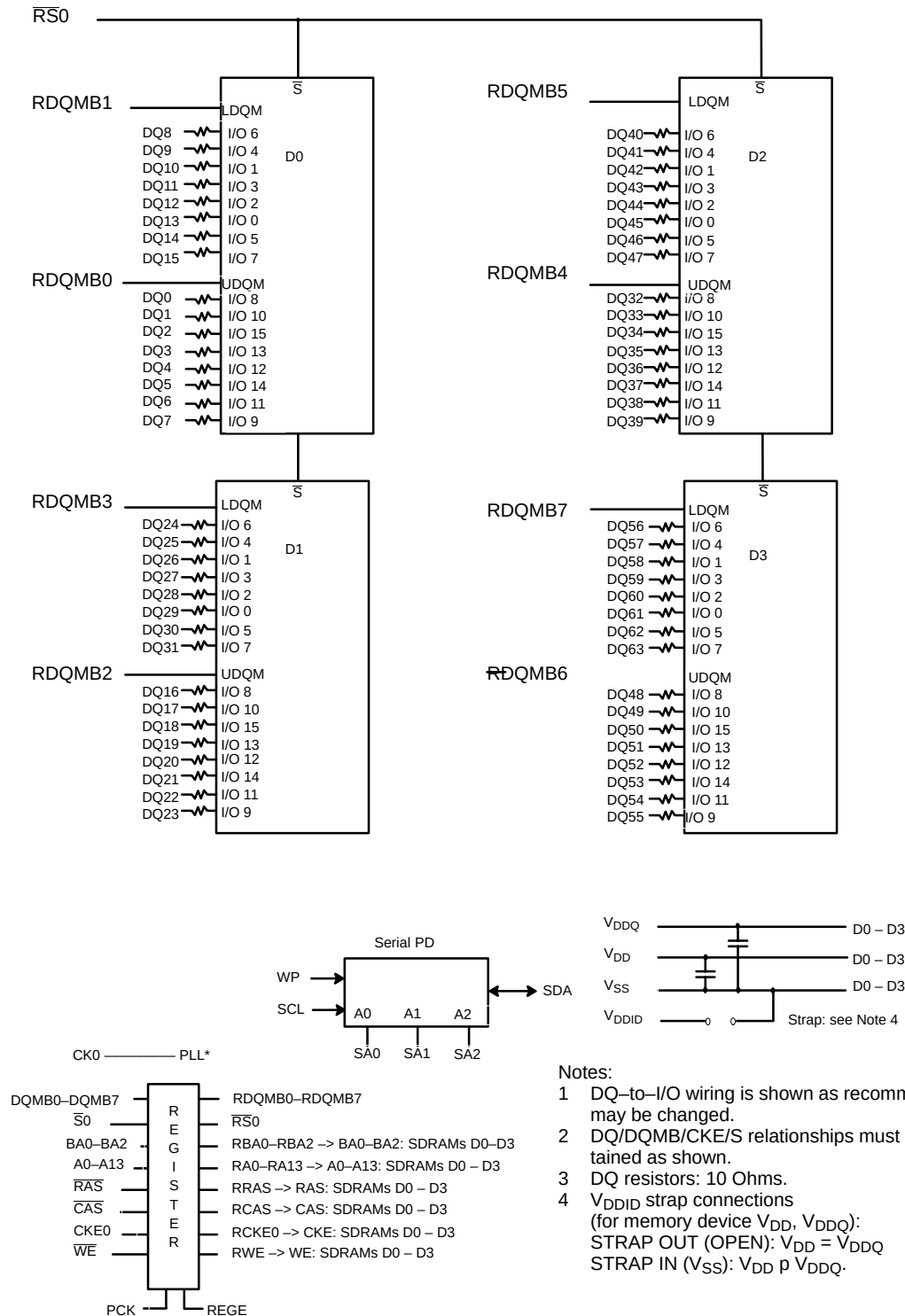


FIGURE 4.5.12-B
184 PIN X64 SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM (1 BANK, X8 SDR SDRAMs)



* Wire per Clock Loading Table/Wiring Diagrams

FIGURE 4.5.12-C
184 PIN X64 SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM (1 BANK, X16 SDR SDRAMs)

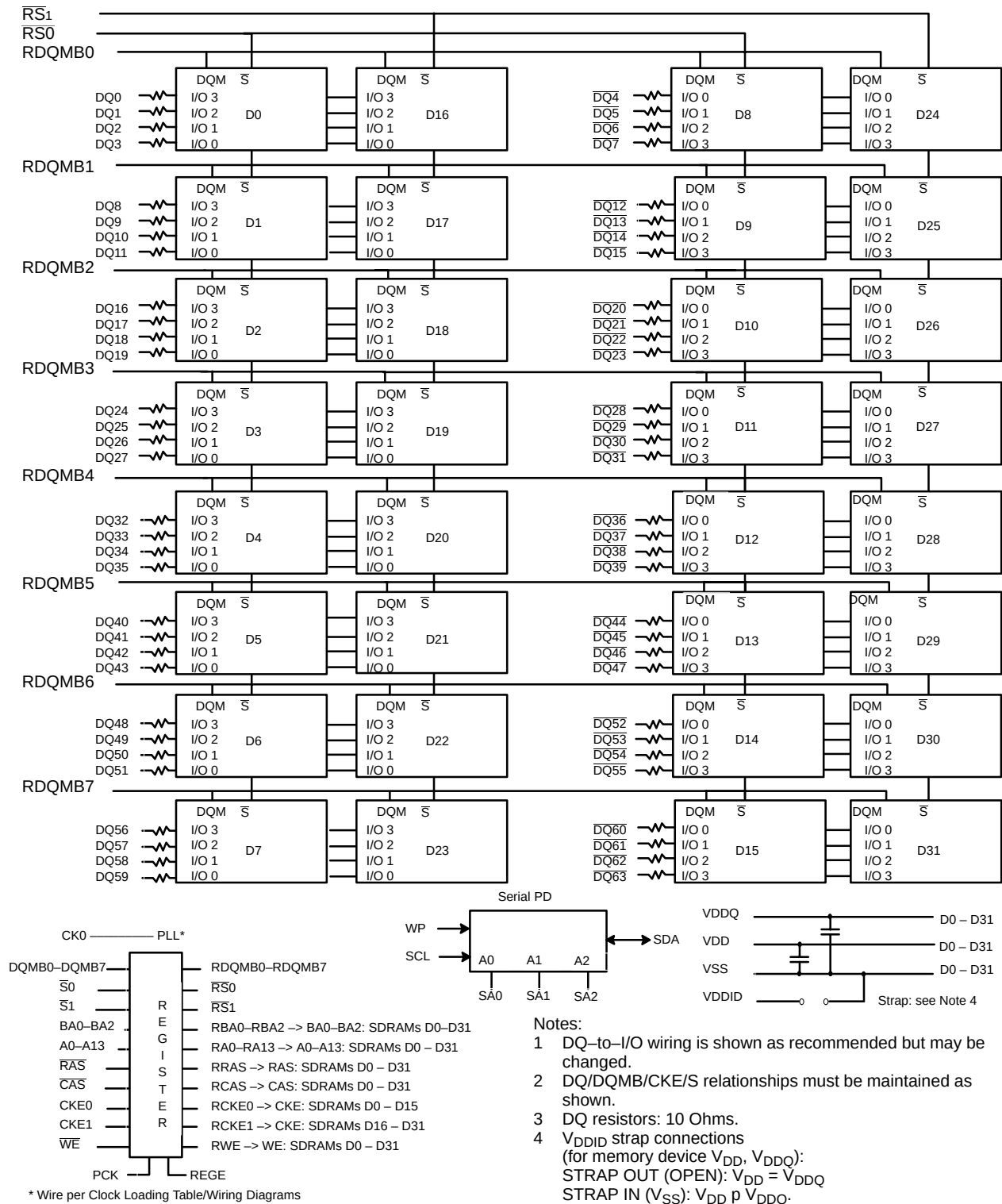


FIGURE 4.5.12-D
184 PIN X64 SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM
(2 BANKS, X4 SDR SDRAMs WITH DOUBLE CKE)

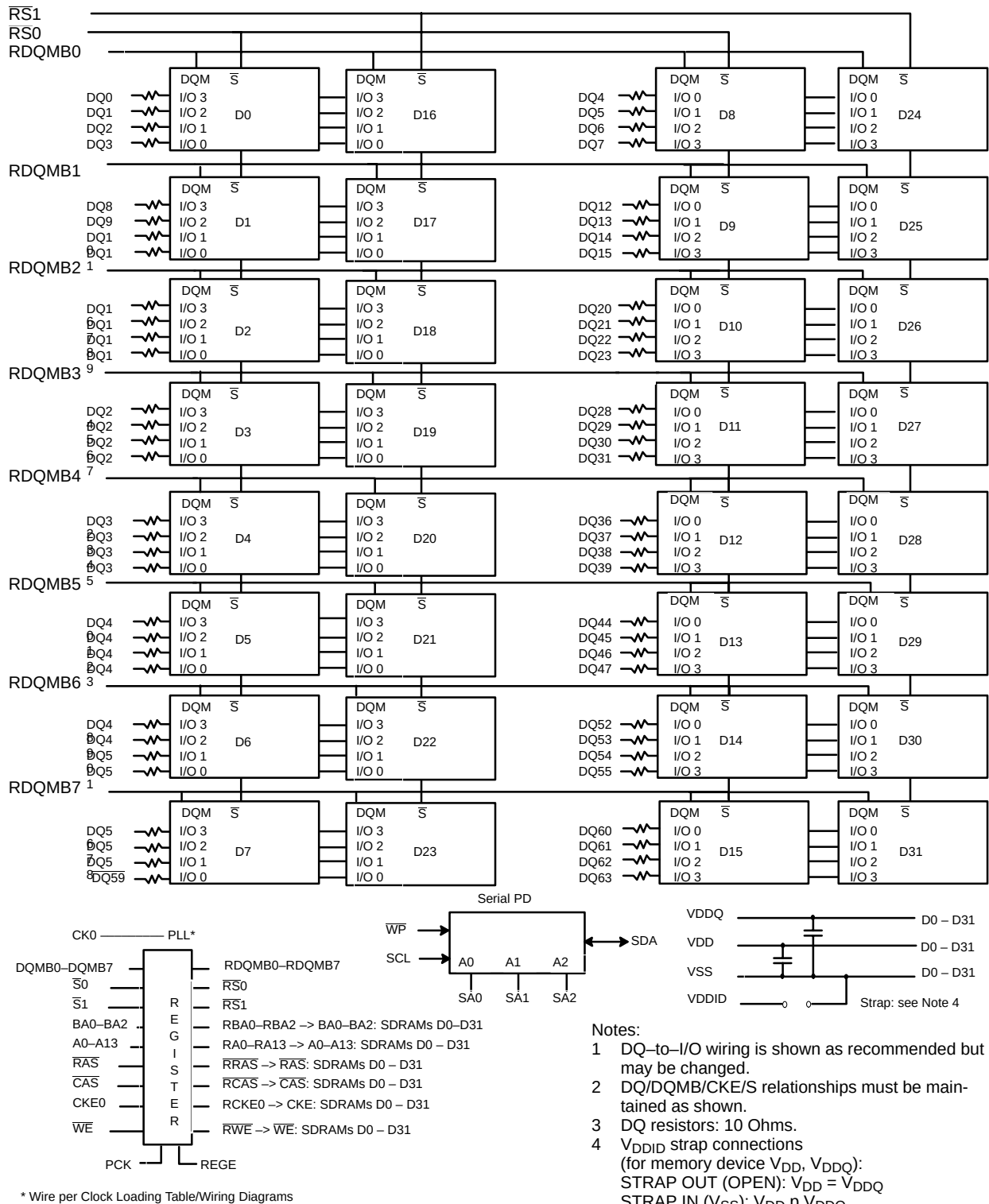
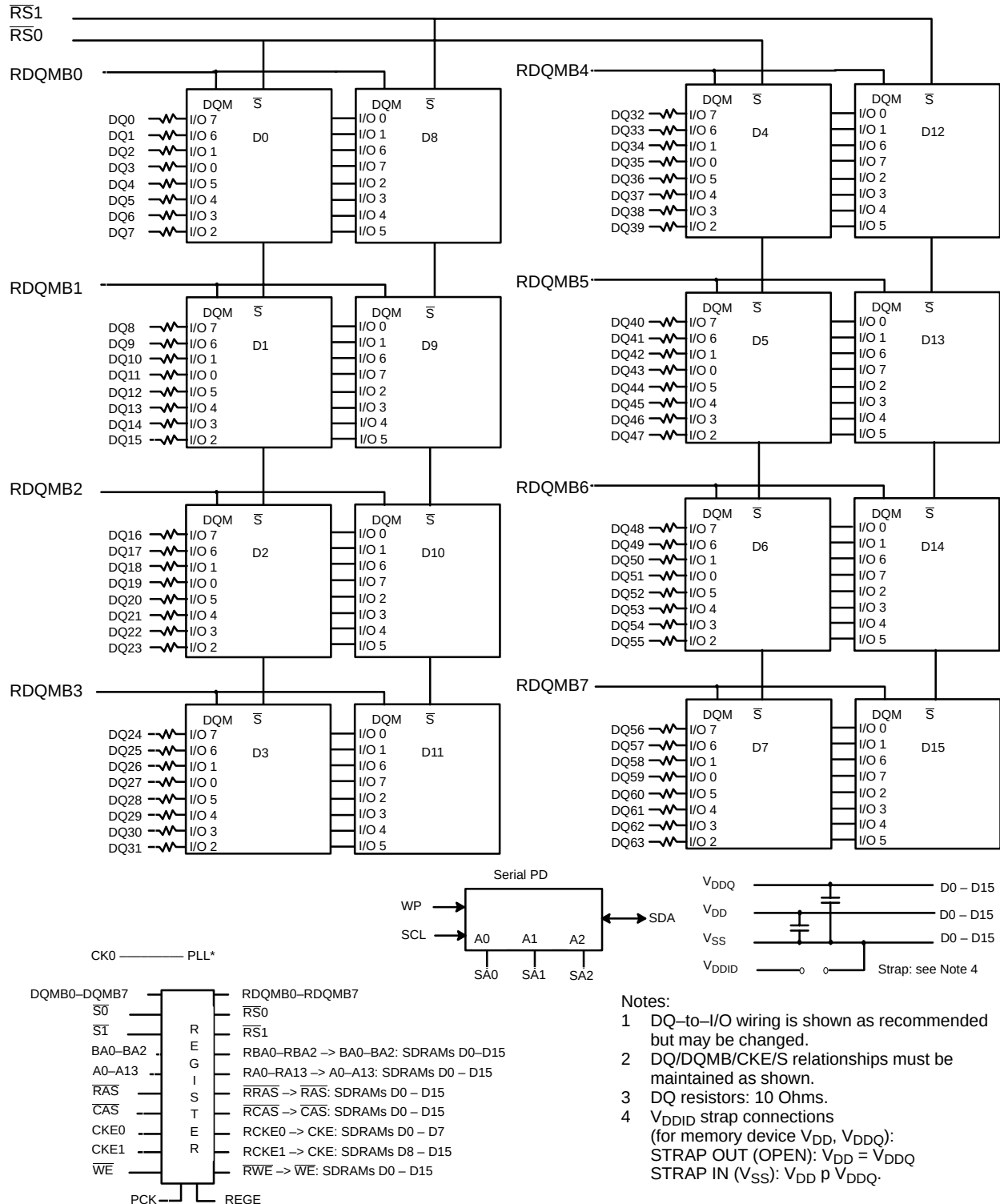


FIGURE 4.5.12-E
184 PIN X64 SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM
(2 BANKS, X4 SDR SDRAMs WITH SINGLE CKE)



* Wire per Clock Loading Table/Wiring Diagrams

FIGURE 4.5.12-F
184 PIN X64 SDR REGISTERED SDRAM DIMM BLOCK DIAGRAM (2 BANK, X8 SDR SDRAMs)