

4.5.13 – 144 & 168 PIN PROCESSOR ENHANCED MEMORY MODULE (PEMM) FAMILIES WITH EDO-DRAM OR SDRAM

BACKGROUND INFORMATION: The Processor Enhanced Memory Module (PEMM) architecture is a modification to existing JEDEC DIMM standards which enables processing to take place directly on memory modules. This architecture is sometimes referred to as "Basava Technology". The applicable modules were modified in an earlier release to add signals that are needed to enable this new functionality. This Standard shows three possible block diagrams for PEMMs including these new additions/ changes.

PEMMs are intended to be designed using X64 interfaces only, on 144-pin or 168-pin DIMMs, containing either EDO-DRAM or SDRAM devices. These block diagrams are being supplied to JEDEC for reference only as a guideline for possible PEMM designs.

CAPACITY—As defined on the applicable module standards.

DATA CONFIGURATIONS—One DATA Word configuration is defined:
—64 BIT without PARITY

CONFIGURATION—3 Different Configurations are defined using various combinations of X8 & X16 memory devices.

LOGIC FEATURES—The modules contain processor enhancement functionality.

PACKAGE—144 & 168 PIN JEDEC DIMM MEMORY MODULES

PIN ASSIGNMENTS AND PD TABLES—As defined in the applicable DIMM Standards.

PIN DEFINITIONS—As defined in the applicable DIMM Standards.

CONFIGURATION BLOCK DIAGRAM—Figs. 4.5.13-F through 4.5.13-M

The contents of this Standard are as follows:

Section 1 defines a series of terms and acronyms that are specific to the PEMM Architecture. The terms will not be added to the general terminology section in Chapter 2 of this Standard.

Section 2 contains descriptions of the PEMM Modes Of Operation.

Section 3 contains block diagrams that are being supplied for reference only as a guideline for possible PEMM designs.

Section 4.5.13.1–PEMM specific term and acronym definitions

C0: Reference designator for the PEMM controller.

CK0L, CK0H, CK1L, CK1H: Clock signals to shared memory (low and high, 2 copies each) on PEMM. Selected from MUX M2 and M3.

CKEL, CKEH: Clock Enable signals to shared memory (low and high) on PEMM. Sourced by PEMM Controller.

CKP: PEMM processor shared memory clock source signal.

M0L–M1L, M0H–M1H: Reference designators for 24–to–12 bit FET based MUXes. Used on the PEMM for selecting control lines to shared memory.

M2–M3: Reference designators for 4x 2–to–1 bit FET based MUXes. Used on the PEMM for selecting the clock source to shared memory.

$\overline{\text{MIRQ}}$: New card edge signal standardized for the PEMM to request an interrupt from the host.

$\overline{\text{MWAIT}}$: New card edge signal standardized for the PEMM to alert host to stall current memory access.

P0: Reference designator for the PEMM processor.

PA[n..0]: PEMM processor shared memory address bus.

PBA[m..0]: PEMM processor shared memory bank select bus.

$\overline{\text{PCAS}}$: PEMM processor shared memory CAS signal.

PDQ[31:0]: PEMM processor shared memory data bus.

PDQM[3..0]: PEMM processor shared memory data byte mask bus.

PEMM: Abbreviation for Processor Enhanced Memory Module.

PEMM controller: A device on the PEMM that controls the PEMM's general functions, such as: shared memory control, program download control, program execution control, etc.

PEMM processor: The processing device that is present on the PEMM.

$\overline{\text{PRAS}}$: PEMM processor shared memory RAS signal.

Processor Enhanced Memory Module: A 168–pin DIMM or 144–pin SO–DIMM with an embedded processor and shared system memory. PEMMs can be designed using SDRAM, or EDO DRAM, using X64 interfaces.

$\overline{\text{PS}}$: PEMM processor shared memory chip select signal.

$\overline{\text{PWE}}$: PEMM processor shared memory write enable signal.

S0A–S7A, S0B–S7B: Reference designators for X32 FET based data switches. These switches are controllable in 8–bit words. Used on the PEMM for selecting data lines to shared memory.

Section 4.5.13.2

1 PEMM Modes of Operation

The PEMM has three basic modes of operation. These modes are:

- 1) **Standard Mode:** Default power-up mode. (The PEMM appears to the system as a standard DIMM)
- 2) **Configuration Mode:** The PEMM is active, and its control registers are mapped into the main memory space
- 3) **Smart Mode:** Same as the configuration mode; however the embedded processor on the PEMM is actually executing

The **standard mode** is the default power-up mode of the module. In the standard mode, the module is functionally equivalent to a standard DIMM.

Before the benefits of the processor on the PEMM can be realized, the host system must first recognize the presence of the PEMM, and then activate the superset features of the PEMM by switching it from the standard mode to the configuration mode. Superset information is provided in the PEMM's SPD area to aid in the recognition and location of the PEMM at system power-up time.

The **configuration mode** is entered only after the following two requirements are met, in order, while in the standard mode:

- 1) The proper toggling pattern takes place (driven by the host system) on the PEMM's MIRQ signal line. This pattern needs only to occur once after power-up.
- 2) A specific serial signature is written to the "power-up address" location as specified in the Superset SPD area for the PEMM.

(See the "Transitioning from Standard Mode to Configuration Mode" Application Note (section 2) for more information regarding these two requirements.)

Once the configuration mode is active, the host system may configure the PEMM for operation by accessing any or all memory-mapped configuration registers, and downloading the program for the embedded processor. These memory-mapped registers control all of the PEMM's superset functions including:

- Control of the onboard shared memory
- Direct communication with the embedded processor on the PEMM
- PEMM program download and execution control
- General status monitoring and configuration

The memory-mapped registers are placed "on top" of the standard memory, starting at the SPD specified power-up address as shown in the following figure:

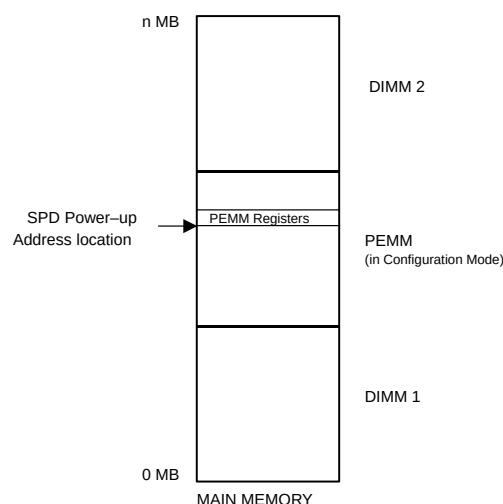


Figure 4.5.13-1: PEMM Registers shown on top of main memory

The **smart mode** can be entered from the configuration mode by simply accessing one of the memory–mapped configuration registers. Booting and execution of the embedded processor can be controlled directly via these registers.

Likewise, the standard mode can be re–entered from either the configuration mode or the smart mode at any time via control of the same memory–mapped configuration registers. It must be noted that whenever the smart mode is exited, that program execution on the PEMM will immediately halt.

The following figure shows the basic state diagram for the PEMM:

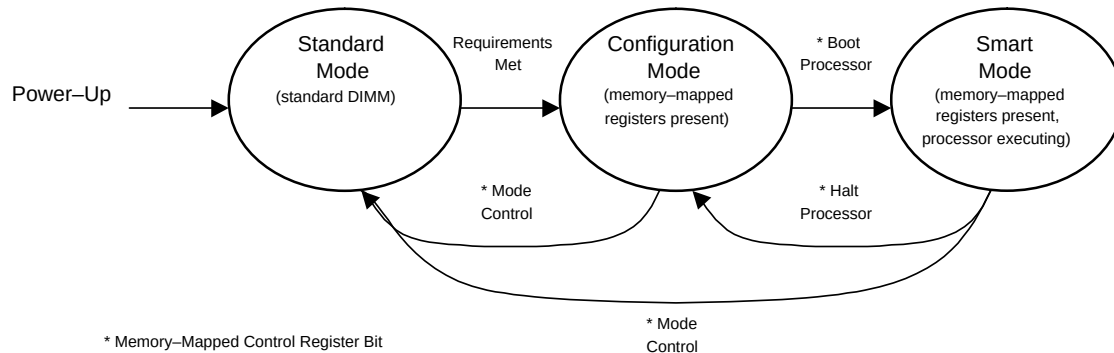


Figure 4.5.13–2: PEMM State Diagram

2 Transitioning from Standard Mode to Configuration Mode – Application Note (information only)

The PEMM device driver is responsible for the discovery (via SPD), management, and all communication with the PEMM's memory–mapped registers. This communication includes the switching between the PEMM's operational modes.

The PEMM's default mode after power–up is the standard mode. While in the standard mode, the PEMM appears as a normal DIMM to the host system. It is important that the PEMM remain in the standard mode until specific events occur that transition it to the configuration mode.

The first event that must occur following system power–up is that the PEMM's MIRQ signal line must be toggled in the proper sequence, driven by the host system. In the standard mode, the MIRQ line on the PEMM is configured as an input. (MIRQ becomes a PEMM open–drain output when the PEMM is in the configuration mode or smart mode; thus, the host system should **never** drive the MIRQ signal when any installed PEMM is in these modes.) After the MIRQ sequence has been transmitted after power–up, the host should configure MIRQ as an input, monitoring this signal for PEMM–driven falling edges (interrupt condition).

Directly after power–up, the PEMM will enter the IDLE state and wait for the proper MIRQ sequence to be received. Once the proper sequence is received, the PEMM will transition to the IDLE_2 state. It is only from this state that the PEMM will begin to monitor the memory bus for the serial signature sequence. The MIRQ sequence only needs to be entered once after power–up as the IDLE_2 state is re–entered directly upon transitioning to the standard mode from the configuration or smart modes.

The second event (receipt of the serial signature) must occur after the IDLE_2 state has been reached. From the IDLE_2 state, the PEMM can be placed into the configuration mode by writing a “serial signature” to the power–up address specified in the PEMM's SPD. This serial signature is sent to the PEMM by the host system by writing several words to this address, in a particular order with NO reads in between each write. Reads and writes to other addresses on the PEMM, or to other DIMMs will be ignored by the PEMM Controller, thus having no effect on the validation of the Serial Signature sequence. Any read or invalid write to the PEMM's power–up address will be rejected and necessitate the Serial Signature sequence attempt to begin again.

A proper serial signature entry from any other state other than IDLE_2 has no effect. The inclusion of the MIRQ sequence as a necessity to enter the IDLE_2 state acts as an added hardware safeguard against unwanted PEMM mode transitions.