

4.5.5 – 144 PIN DRAM SO-DIMM FAMILY

NOTE: It is recommended that this module be used primarily for main memory applications. At the time this standard was published, the Committee was working on a standard for a Graphics 144 Pin Module to be published in the near future.

CAPACITY—up to the addressing capacity of 16 bits, address multiplexed with words of 32, 36, & 40 bits.

DATA CONFIGURATIONS—Two DATA Word configurations are defined:

- 64 BIT DRAM without PARITY
- 72 BIT DRAM for ECC CODES

CONFIGURATION—10 Different Configurations are defined using various combinations of X4, X8, and X16 DRAM memories including 2 bank configurations, 5 for 64 bit and 5 for 72 bit.

LOGIC FEATURES—The modules contain the Serial Presence Detect (SPD) feature that consists of a built in serial access EEPROM that stores information on multiple parameters and attributes of the module such as technology, storage capacity, configuration, data word configuration, refresh mode, and speed of the module.

PACKAGE—144 PIN JEDEC SO-DIMM MEMORY MODULE

PIN ASSIGNMENTS —Figs. 4.5.5-A & 4.5.5-B

MODULE PIN NUMBERING AND KEYING METHODOLOGY — Fig. 4.5.5-C

TECHNOLOGY COMPARISON TABLE — Fig. 4.5.5-D

DRAM SPD INFORMATION — Fig. 4.5.5-E

X64 DRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.5.5-F through 4.5.5-J, 4.5.5-P, 4.5.5-Q ■

X72 DRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.5.5-K through 4.5.5-O

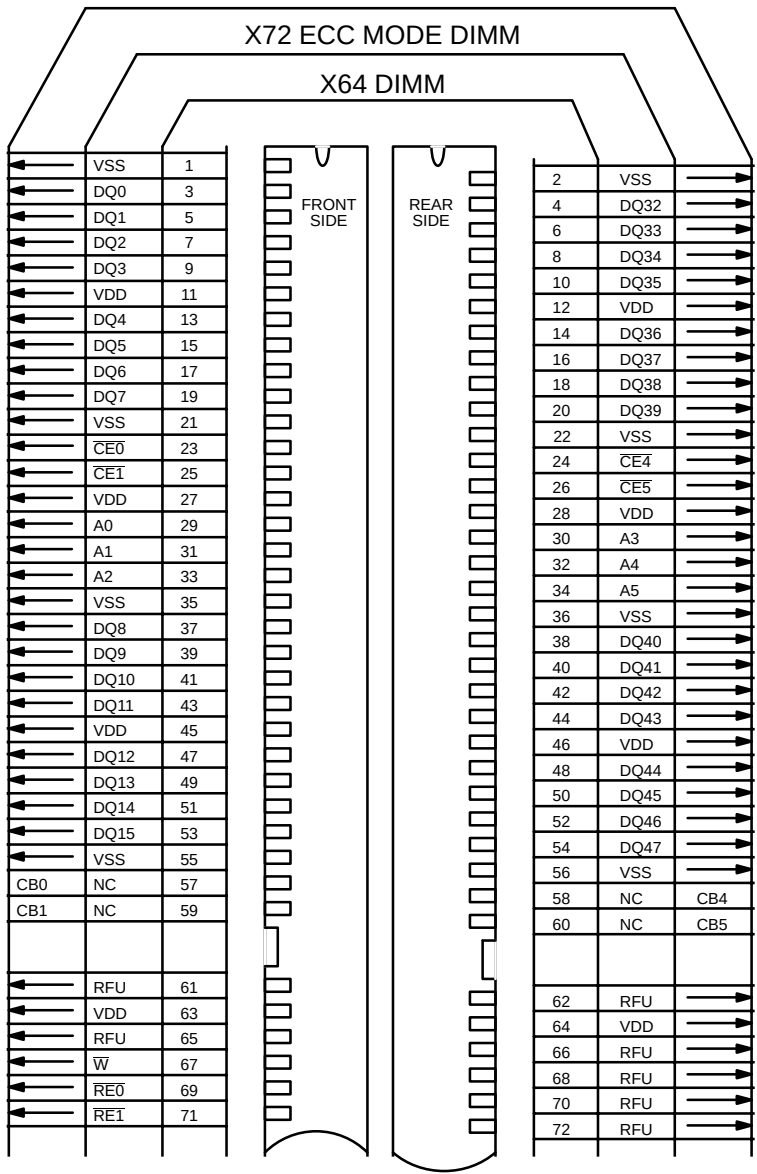


Figure 4.5.5-A
144 Pin X64 & X72 DRAM SO-DIMM, PIN ASSIGNMENTS
UPPER HALF

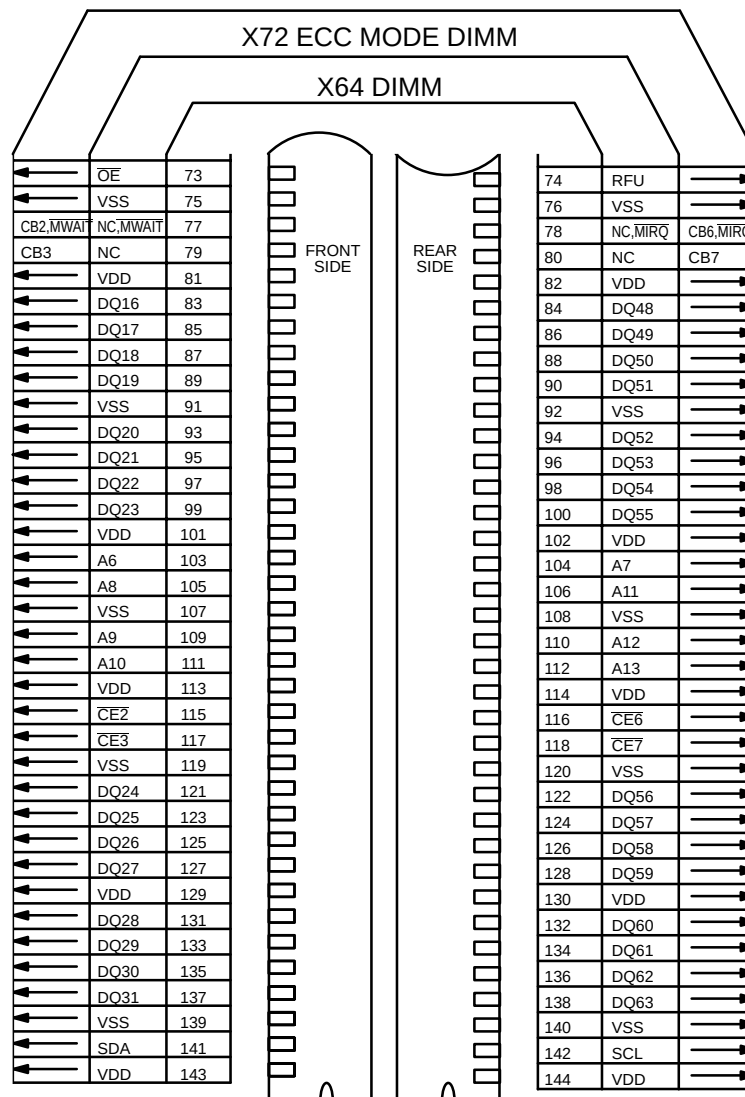


Figure 4.5.5-B
144 Pin X64 & X72 DRAM SO-DIMM, PIN ASSIGNMENTS
LOWER HALF

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The diagram below shows the keying methodology employed on 8-byte SO DIMMs. The voltage key provides a positive interlock so that SO DIMMs can only be plugged into a system with the proper supply voltage, reducing potential damage to the module DRAM chips. Unless the designer chooses the appropriate connector, the system will not work.

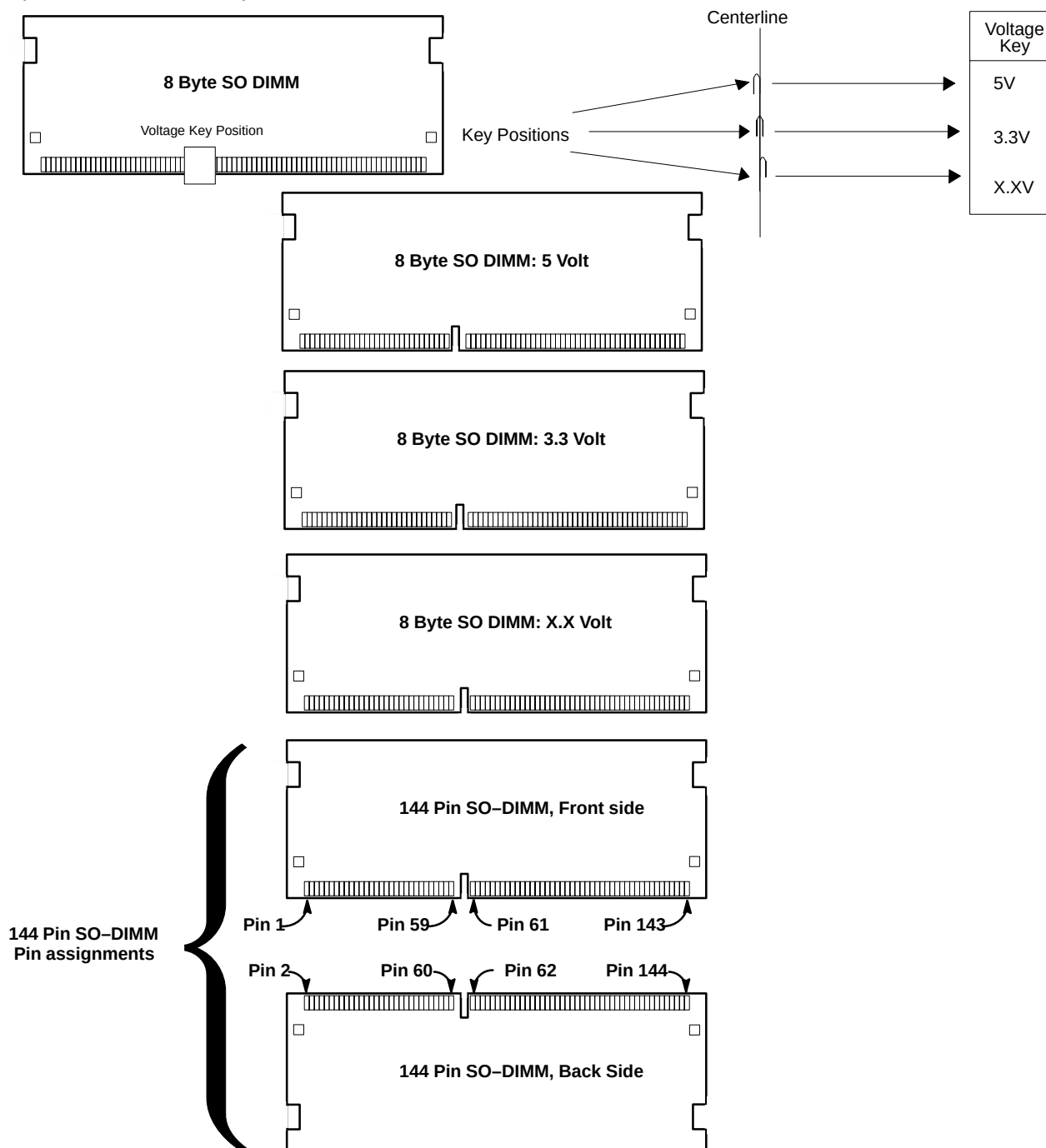


Figure 4.5.5-C
144 Pin SO-DRAM DIMM Keying Methodology

Pin #	DRAM SODIMM	SDRAM SODIMM
23	CAS0	DQMB0
25	CAS1	DQMB1
61	DU	CK0
65	DU	RAS
69	RAS0	S0
71	RAS1	S1
73	OE	DU
111	A10	A10/AP
115	CAS2	DQMB2
117	CAS3	DQMB3
24	CAS4	DQMB4
26	CAS5	DQMB5
62	DU	CKE0
66	DU	CAS
68	NC	CKE1
70	NC	A12
72	NC	A13, DSF
74	NC	CK1
106	A11	BA0
110	A12	BA1
112	A13	A11
116	CAS6	DQMB6
118	CAS7	DQMB7

Figure 4.5.5-D
Pinout Comparison, 144 Pin DRAM & SDRAM SO-DIMM

8 Byte DRAM SO–DIMM PD Information

- Serial PD Interface Protocol: I²C (Synchronous 2-Wire Bus)
- The following information is to be written into EEPROM device during module production:
 - Module Configurations, Addressing: (Bytes 3-7)

Module Configuration	DRAM Organization	Option 1		Option 2		Option 3	
		RAS Addr.	CAS Addr.	RAS Addr.	CAS Addr.	RAS Addr.	CAS Addr.
512K x 64/72	512K x 8	10	9				
512K x 64	512K x 32	10	9	12	7		
1M x 64/72	512K x 8	10	9				
1M x 64/72	1M x 4/16	10	10	12	8		
1M x 64	512K x 32	10	9	12	7		
2M x 64/72	1M x 16	10	10	12	8		
2M x 64/72	2M x 8	11	10	12	9		
2M x 64	2M x 32	12	9	13	8		
4M x 64/72	2M x 8	11	10	12	9		
4M x 64/72	4M x 4/16	11	11	12	10	*13	9
4M x 64	2M x 32	12	9	13	8		
8M x 64/72	4M x 16	11	11	12	10	*13	9
8M x 64/72	8M x 8	12	11	13	10		
8M x 64	8M x 32	TBD	TBD				
16M x 64/72	8M x 8	12	11	13	10		
16M x 64/72	16M x 4/16	12	12	13	11	*14	10
16M x 64	8M x 32	TBD	TBD				
32M x 64/72	16M x 16	12	12	13	11	*14	10
32M x 64/72	32M x 8	13	12	14	11		
32M x 64	32M x 32	TBD	TBD				
64M x 64/72	32M x 8	13	12	14	11		
64M x 64/72	64M x 4	13	13	14	12		
64M x 64	32M x 32	TBD	TBD				

(Note: All options possible with DRAM standards are shown)
 * This addressing option applies to x16 DRAM configuration

b. Allowable configurations: (Byte 11)

- x64 (Non-parity, Byte controls)
- x72 (ECC-optimized, Byte controls)

c. Functional Attributes:

- Power Supply Voltage/Interface levels (Byte 8)
- RAS access (Byte 9)
- CAS access (Byte 10)
- Refresh rate/type (Byte 12)

For Detailed Serial PD Byte data see section 4.1.2.3, Appendix C DRAM Serial Presence Detect Definitions.

- Serial PD interface is standard I²C architecture
- Pull-up resistors (4.7K typical value) are required on all open drain/open collector bus devices (SCL and SDA).
- Current sink capability on SCL and SDA source (I_{OL} max) must be at least 3ma to maintain a valid “low level”.
- I²C Bus specification:

Figure 4.5.5–E**144 Pin X64 DRAM SO–DIMM, SPD TABLE AND INFORMATION**