

4.5.6 – 144 PIN SDRAM SO-DIMM FAMILY

CAPACITY—up to the addressing capacity of 16 bits, address multiplexed with words of 32, 36, & 40 bits.

DATA CONFIGURATIONS—Two DATA Word configurations are defined:

- 64 BIT SDRAM without PARITY
- 72 BIT SDRAM for ECC CODES

CONFIGURATION—10 Different Configurations are defined using various combinations of X4, X8, and X16 SDRAM memories including 2 bank configurations, 5 for 64 bit and 5 for 72 bit.

LOGIC FEATURES—The modules contain the Serial Presence Detect (SPD) feature that consist of a built in serial access EEPROM that stores information on multiple parameters and attributes of the module such as technology, storage capacity, configuration, data word configuration, refresh mode, and speed of the module.

PACKAGE—144 PIN JEDEC SO-DIMM MEMORY MODULE

PIN ASSIGNMENTS —Figs. 4.5.6-A & 4.5.6-B

SDRAM SPD INFORMATION — Fig. 4.5.6-C

MODULE PIN NUMBERING AND KEYING METHODOLOGY — Fig. 4.5.6-D

TECHNOLOGY COMPARISON TABLE — Fig. 4.5.6-E

SDRAM CLOCK LOADING & WIRING—Figs. 4.5.6-F

X64 SDRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.5.6-G through 4.5.6-L

X72 SDRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.5.6-M through 4.5.6-P

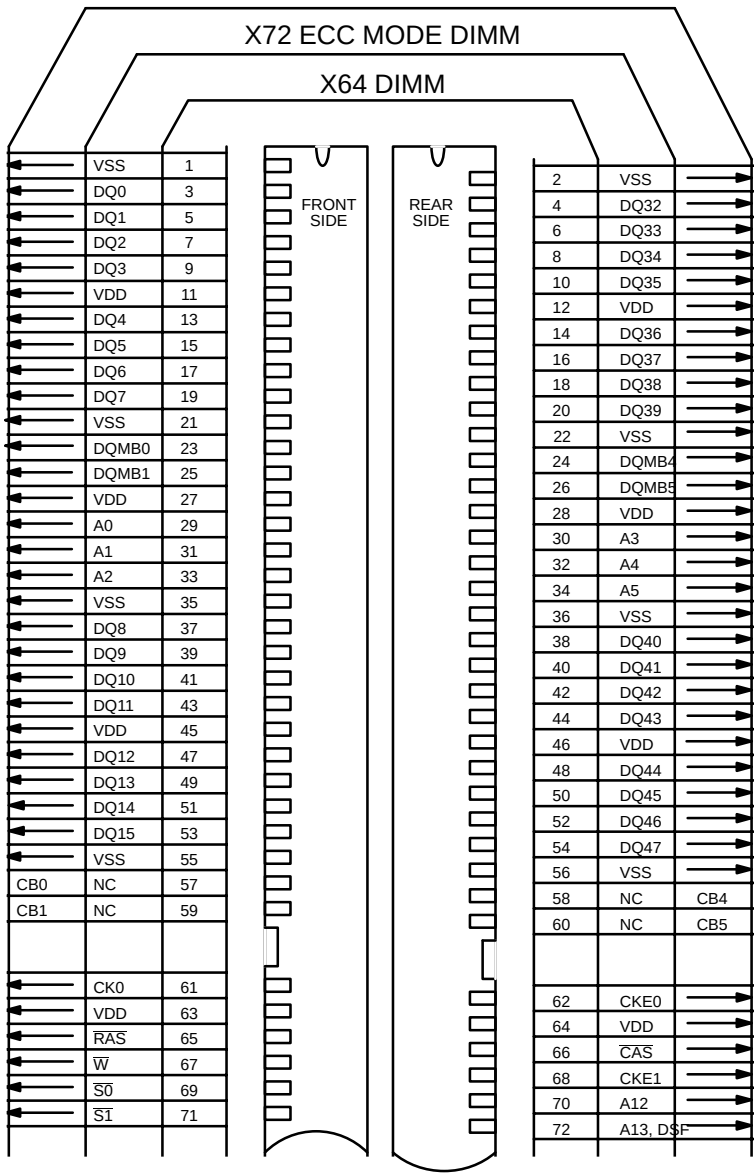


Figure 4.5.6-A
144 Pin X64 & X72 SDRAM SO-DIMM, PIN ASSIGNMENTS
UPPER HALF

50 DQ34

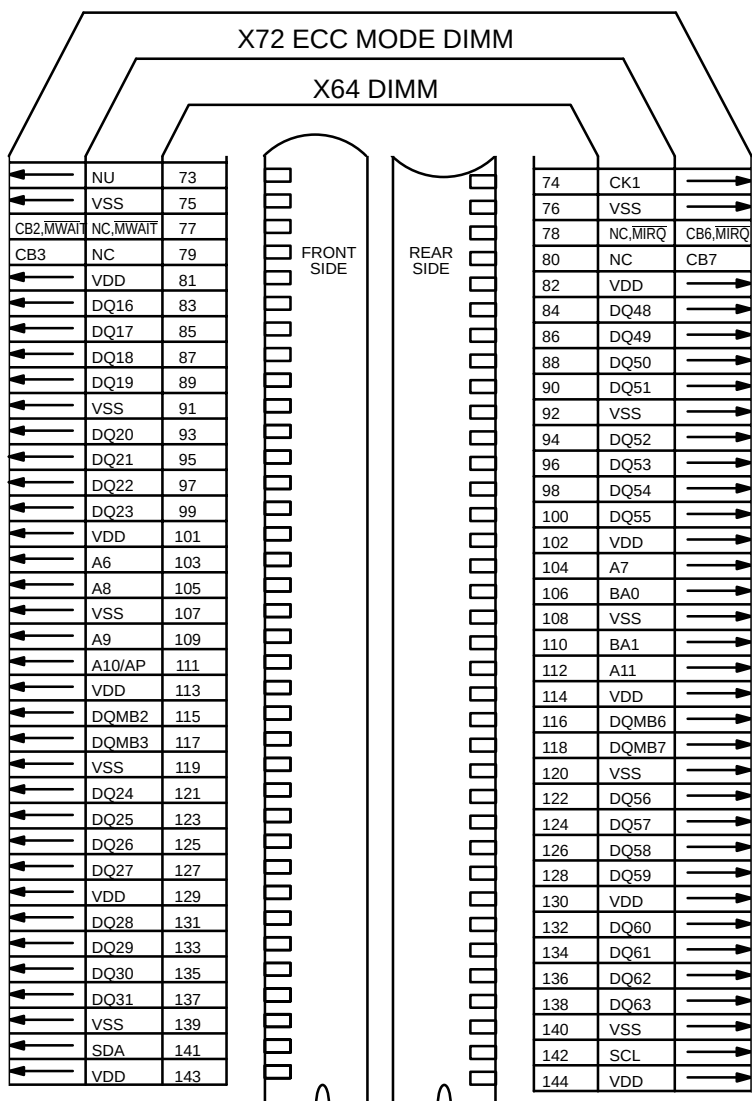


Figure 4.5.6-B
144 Pin X64 & X72 SDRAM SO-DIMM, PIN ASSIGNMENTS
LOWER HALF

Module Configuration	SDRAM Organization	Option 1			Option 2			Option 3		
		# Bank accr.	RAS accr.	CAS accr.	# Bank accr.	RAS accr.	CAS accr.	# Bank accr.	RAS accr.	CAS accr.
1M x 64/72	1M x 16	1	11	8						
2M x 64/72	1M x 16	1	11	8						
2M x 64	2M x 32	2	11	8						
2M x 64/72	2M x 8	1	11	9						
4M x 64/72	2M x 8	1	11	9						
4M x 64	2M x 32	2	11	8						
4M x 64/72	4M x 16	2	12	8	1	13	8			
8M x 64/72	4M x 16	2	12	8	1	13	8			
8M x 64	8M x 32	2	13	8	2	12	9			
8M x 64/72	8M x 8	2	12	9	1	13	9			
16M x 64/72	8M x 8	2	12	9	1	13	9			
16M x 64	8M x 32	2	13	8	2	12	9			
16M x 64/72	16M x 16	2	13	9						
32M x 64/72	16M x 16	2	13	9						
32M x 64/72	32M x 8	2	13	10						
64M x 64/72	32M x 8	2	13	10						
(Note: All options possible with SDRAM standards are shown)										

b. Allowable configurations: (Byte 11)

- x64 (Non-parity, Byte controls)
- x72 (ECC-optimized, Byte controls)

c. Functional Attributes:

- Power Supply Voltage/Interface levels (Byte 8)
- SDRAM cycle time (Byte 9)
- SDRAM access from Clock (Byte 10)
- Refresh rate/type (Byte 12)
- SDRAM module attributes (Byte 13)
- SDRAM device attributes (Bytes 14 - 20)
- Primary/Secondary SDRAM (Bytes 21 - 22)

Figure 4.5.6-C
144 Pin SDRAM SO-DIMM, PD INFORMATION

The diagram below shows the keying methodology employed on 8-byte SO DIMMs. The voltage key provides a positive interlock so that SO DIMMs can only be plugged into a system with the proper supply voltage, reducing potential damage to the module DRAM chips. Unless the designer chooses the appropriate connector, the system will not work.

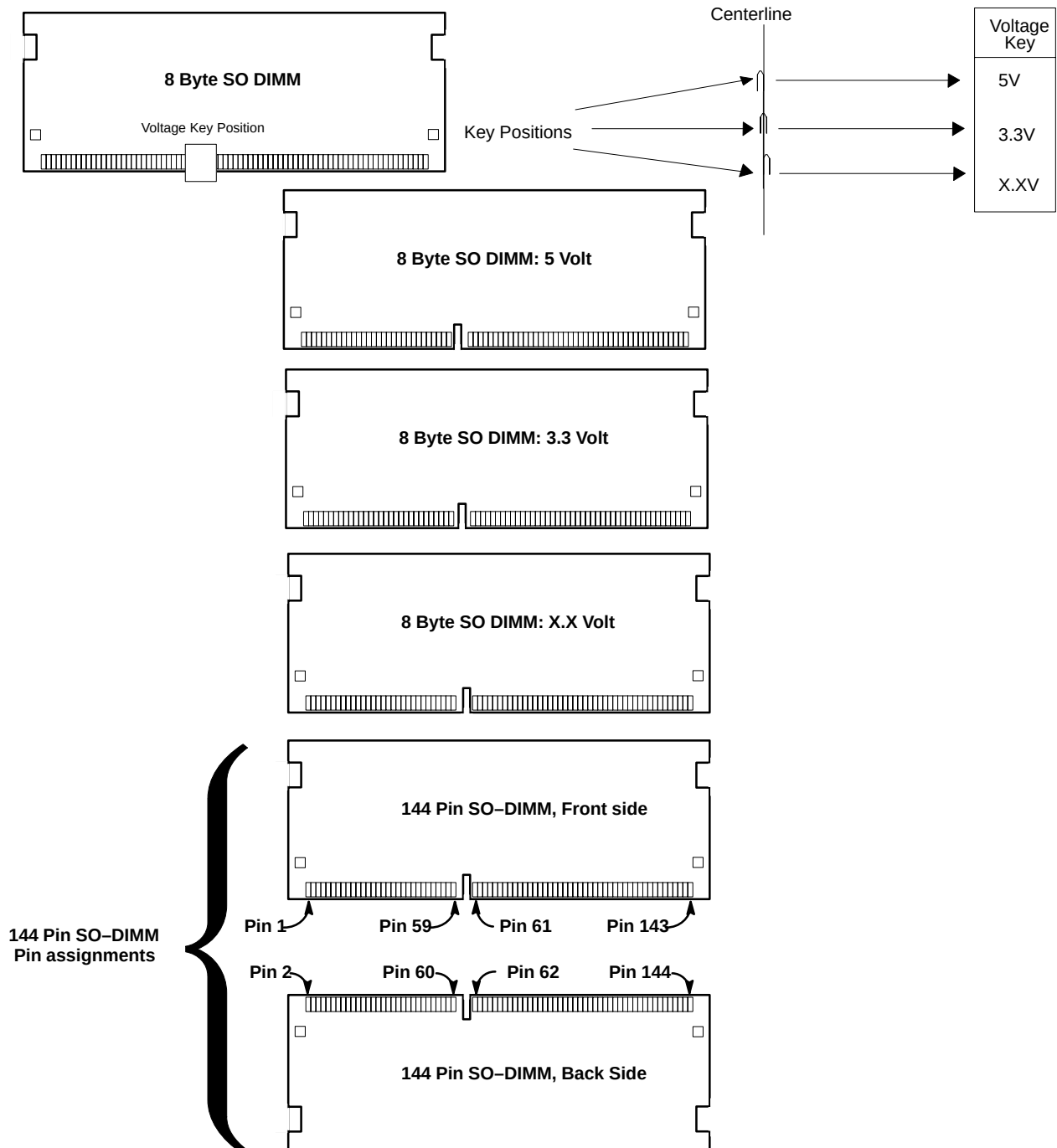


Figure 4.5.6-D
144 Pin SDRAM DIMM Keying Methodology

Release 7

Pin #	DRAM SODIMM	SDRAM SODIMM
23	$\overline{\text{CAS}}0$	DQMB0
25	$\overline{\text{CAS}}1$	DQMB1
61	DU	CK0
65	DU	$\overline{\text{RAS}}$
69	$\overline{\text{RAS}}0$	$\overline{\text{S}}0$
71	$\overline{\text{RAS}}1$	$\overline{\text{S}}1$
73	$\overline{\text{OE}}$	DU
111	A10	A10/AP
115	$\overline{\text{CAS}}2$	DQMB2
117	$\overline{\text{CAS}}3$	DQMB3
24	$\overline{\text{CAS}}4$	DQMB4
26	$\overline{\text{CAS}}5$	DQMB5
62	DU	CKE0
66	DU	$\overline{\text{CAS}}$
68	NC	CKE1
70	NC	A12
72	NC	A13, DSF
74	NC	CK1
106	A11	BA0
110	A12	BA1
112	A13	A11
116	$\overline{\text{CAS}}6$	DQMB6
118	$\overline{\text{CAS}}7$	DQMB7

FIGURE 4.5.6-E
Pinout Comparison, 144 Pin DRAM & SDRAM SO-DIMM