

4.5.8 – 144 PIN SDR SGRAM/SDRAM SO-DIMM FAMILY

NOTE: It is recommended that this module be used primarily for Graphics Memory applications. 144 P DRAM & SDRAM standards for Main Memory use have been adopted and are published elsewhere in JESD 21-C.

CAPACITY—up to the addressing capacity of 12 bits, address multiplexed with words of 32, & 64 bits.

DATA CONFIGURATIONS—Two DATA Word configurations are defined:

—32 BIT SGRAM or SDRAM without PARITY

—64 BIT SGRAM or SDRAM without PARITY

CONFIGURATION—4 Different Configurations are defined using X32 SGRAM or SDRAM memories in 1 and 2 bank configurations.

LOGIC FEATURES—The modules contain the Serial Presence Detect (SPD) feature (optional) that consist of a built in serial access EEPROM that stores information on multiple parameters and attributes of the module such as technology, storage capacity, configuration, data word configuration, refresh mode, and speed of the module.

HARDWARE FEATURES—Physical layout parameters and terminating resistors are given to optimize the speed characteristics of the module. The key has been located at pin 50 and is different from the other 144 P SO-DIMM packages.

LOGIC INTERFACE LEVEL—LVTTTL

POWER SUPPLY— $3.3 \text{ V} \pm 10\%$

PACKAGE—144 PIN JEDEC SO-DIMM MEMORY MODULE with the Key at pin 50.

PIN ASSIGNMENTS —Figs. 4.5.8-A & 4.5.8-B

Configuration, Electrical Characteristics, SPD, & Output Measurement Ckt — P 4.5.8-4 & Fig. 4.5.8-C

Resistor Strapping Options & PCB Layout Considerations — P 4.5.8-5

QFP Clock Routing —Fig. 4.5.8-D

QFP Address and Control Routing — Fig. 4.5.8-E

QFP Data Routing — Fig. 4.5.8-F

TSOP Layout Considerations — P 4.5.8-9

256K, 512K, 1M X 32 Block Diagram (1 bank of 1 X 32 device) — Fig. 4.5.8-G

512K, 1M, 2M X 32 Block Diagram (2 bank of 1 X 32 devices) — Fig. 4.5.8-H

256K, 512K, 1M X 64 Block Diagram (1 bank of 2 X 32 devices) — Fig. 4.5.8-I

512K, 1M, 2M X 64 Block Diagram (2 bank of 2 X 32 devices) — Fig. 4.5.8-J

The Pinout below is based on routing for QFP

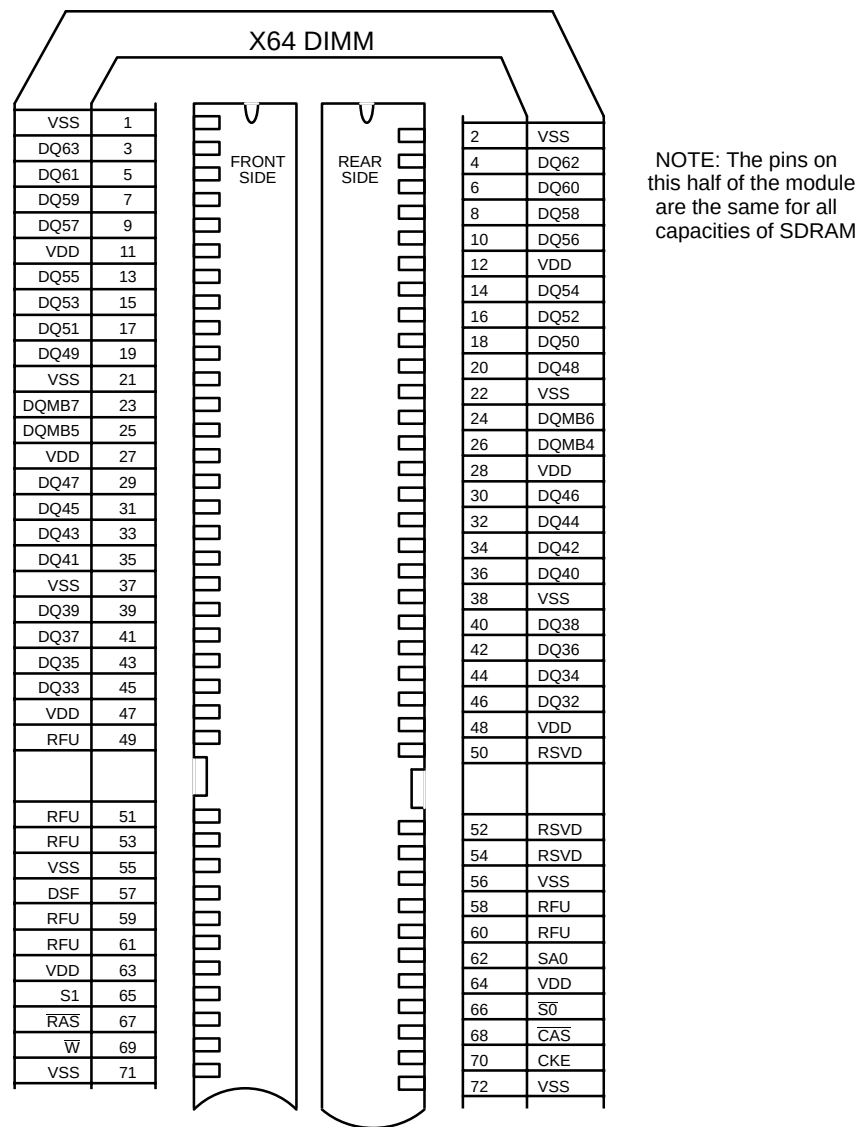


FIGURE 4.5.8-A
144 Pin X32 & X64 SGRAM SO-DIMM, PIN ASSIGNMENTS
UPPER HALF

The Pinout below is based on routing for QFP

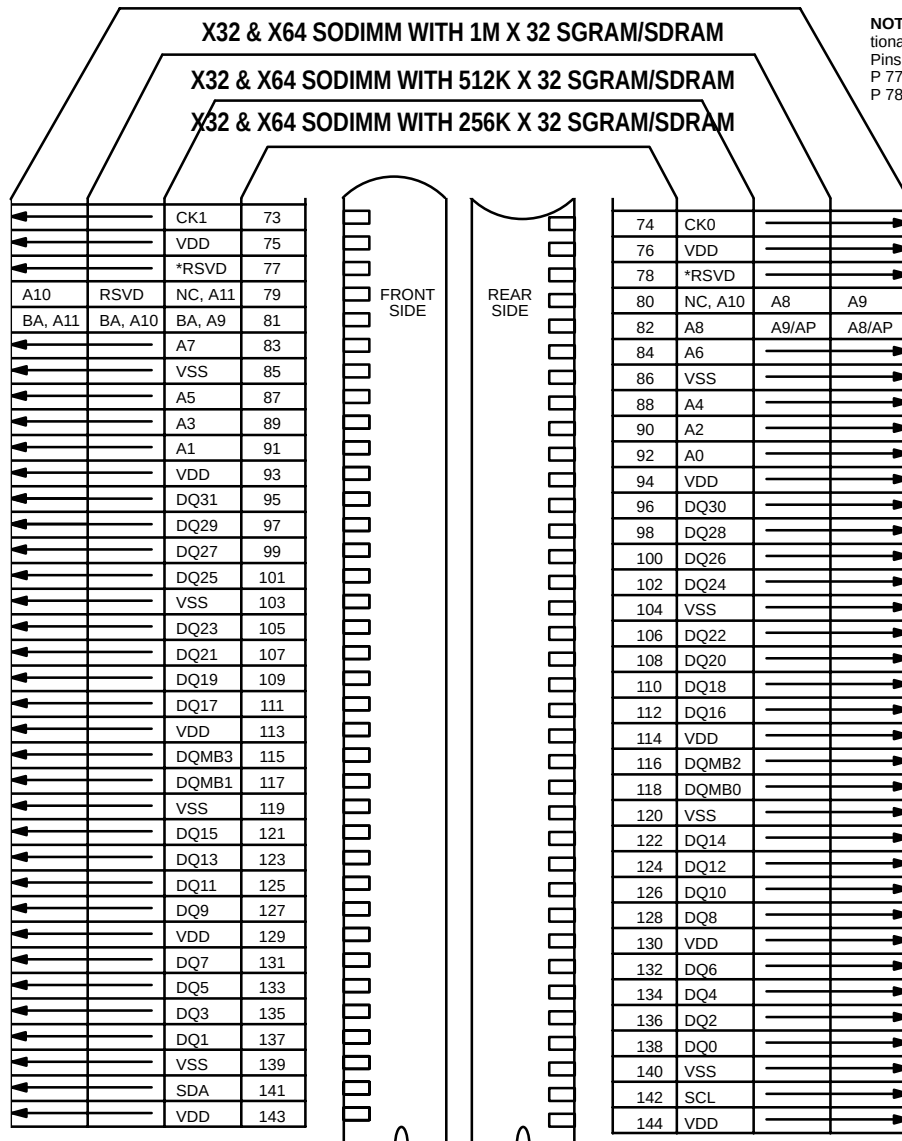


FIGURE 4.5.8-B
144 PIN X32 & X64 SGRAM SO-DIMM, PIN ASSIGNMENTS
LOWER HALF

Release 8r9r10

Configuration

Graphic controllers can determine the module capabilities one of three ways; they are:

- Using the default parameters with power-up testing
- Using resistor strapping options on the data lines
- Using an optional Serial Presence Detect EEPROM

Modules are required to include resistor support (3 resistors); the Serial Presence Detect EEPROM is optional.

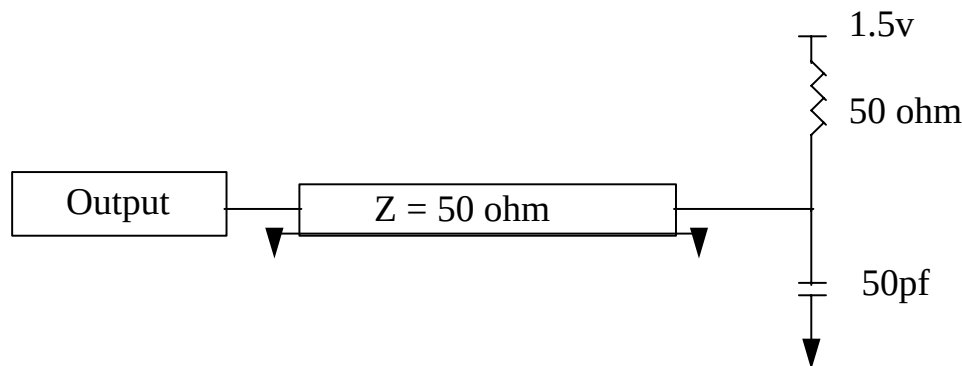
Electrical Characteristics

The module electrical characteristics are carefully controlled to allow system configurations with two separate memory arrays. This may include either two modules or one module plus memory soldered directly to the motherboard or add-in card PCB. Routing on the main board will generally be done as a T-topology. The module's electrical characteristics (as well as the main board's characteristics) must be carefully implemented to insure a balanced T-topology.

The board must have a characteristic impedance between 55 and 85 ohms.

Serial Presence Detect EEPROM

This EEPROM is optional on the module



Reference level for measurement is set at 1.4V.

FIGURE 4.5.8-C
OUTPUT MEASUREMENT LOAD CIRCUIT