

4.5.9 – 144 PIN DDR SGRAM SO–DIMM FAMILY**GENERAL FEATURES**

- 144-pin small outline dual in line memory module (SO-DIMM)
- 64-bit data bus with no ECC and no parity
- Module capacity ranges from 1 MB to 8 MB
- Supports 8 Mb and 16 Mb double data rate (DDR) SGRAMs
- Dual supply 3.3 V and 2.5 V
- 2.5 V DDR I/O Class B on single data rate (SDR) signals
- 2.5 V DDR I/O Class A on double data rate signals
- Similar to existing SDR SO-DIMM

CAPACITY—Module capacity ranges from 1 MB to 8 MB

DATA CONFIGURATIONS—Two DATA Word configurations are defined:

—32 BIT without PARITY

—64 BIT without PARITY

CONFIGURATION—4 Different Configurations are defined using X32 SGRAM memories in 1 and 2 bank configurations.

LOGIC FEATURES—The modules contain the Serial Presence Detect (SPD) feature (optional) that consist of a built in serial access EEPROM that stores information on multiple parameters and attributes of the module such as technology, storage capacity, configuration, data word configuration, refresh mode, and speed of the module.

HARDWARE FEATURES—Physical layout parameters and terminating resistors are given to optimize the speed characteristics of the module. The key has been located at pin 50 and is different from the other 144 P SO–DIMM packages.

LOGIC INTERFACE LEVELS—The interface signals fall into three classes as defined in Tables 1 & 2

Single Data Rate Signals (SDR)

Double Data Rate Signals (DDR)

Serial EEPROM signals (EEPROM)

POWER SUPPLIES—There are 3 power supplies as defined in Tables 1 & 2

VDD,

VCCQ

VDDSPD

PIN ASSIGNMENTS —Figs. 4.5.9–A & 4.5.9–B

PACKAGE—144 PIN JEDEC SO–DIMM MEMORY MODULE with the Key at pin 50.

Clock Net Routing —Fig. 4.5.9–C

512K X 1 Bank X 32 Block Diagram (1 bank of 512K X 32) — Fig. 4.5.9–D

512K X 1 Bank X 64 Block Diagram (1 bank of 512K X 64) — Fig. 4.5.9–E

512K X 2 Banks X 32 Block Diagram (2 banks of 512K X 32) — Fig. 4.5.9–F

1024K X 2 Banks X 32 Block Diagram (2 banks of 1024K X 32) — Fig. 4.5.9–G

Changes From Single Data Rate SO-DIMM

Single Data Rate	Double Data Rate
Single 3.3 V supply VDD (18 pins)	3.3 V VDD (4 pins), 2.5 V VDDQ (15 pins), VDDSPD (1 pin)
All signals 3.3 V LVTTTL	DDR signals are 2.5 V DDR I/O Class A, SDR signals are 2.5 V DDR I/O Class B
Single ended clock, no return data strobe	Differential clock with return data strobe
Clock and data loading not matched	Clock and data loading matched
Clock 0 supplied to both SGRAMs on top side. Clock 1 to both SGRAMs on bottom	Clock 0 applied to SGRAMs on DQ(31:0), Clock 1 to SGRAMs on DQ(63:32)
Few termination resistors required	Series termination on all DDR signals
PQFP or TQFP SGRAM packages	LQFP SGRAM packages
3.3 V Serial Presence Detect (SPD) EEPROM optional	SPD required, with separate supply voltage pin
Pulldown resistors indicate module speed	Module speed parameters stored in SPD
Some references to TSOP options	No TSOP references

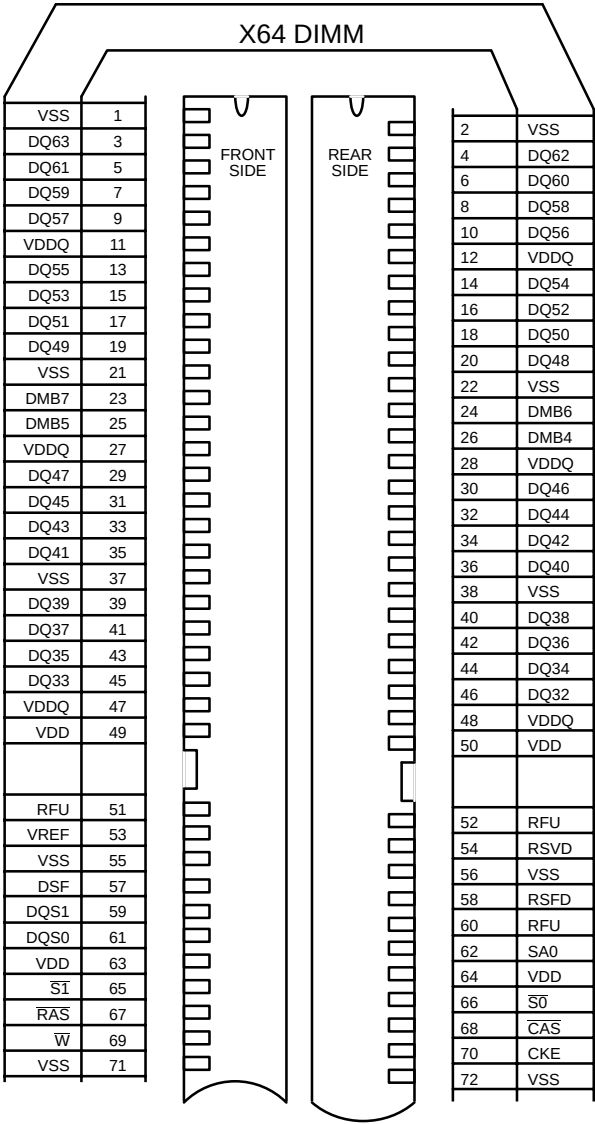


FIGURE 4.5.9-A
144 Pin X32 & X64 DDR SGRAM SO-DIMM, PIN ASSIGNMENTS
UPPER HALF

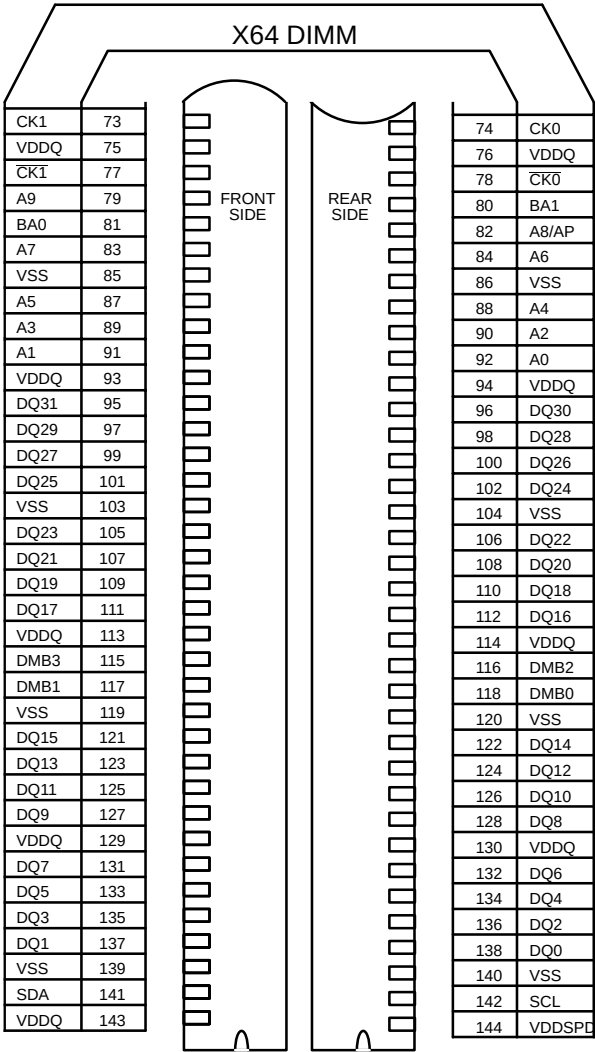


FIGURE 4.5.9-B
144 PIN X32 & X64 DDR SGRAM SO-DIMM, PIN ASSIGNMENTS
LOWER HALF

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