

4.6.1 – 278 PIN BUFFERED SDRAM DIMM FAMILY

CAPACITY—up to the addressing capacity of 16 bits, address multiplexed with words of 16 bytes (144 bits).

DATA CONFIGURATIONS—Only one DATA Word configurations is defined in the initial release:

—144 BIT SDRAM with the location of CHECKBITS undefined

CONFIGURATION—2 Different Configurations are defined using X16 SDRAM memories with 1 and 2 banks

LOGIC FEATURES—The modules contain the Serial Presence Detect (SPD) feature that consist of a built in serial access EEPROM that stores information on mutiple parameters and attributes of the module such as technology, storage capacity, configuration, data word configuration, refresh mode, and speed of the module.

PACKAGE—278 PIN JEDEC DIMM MEMORY MODULE

PIN ASSIGNMENTS —Figs. 4.6.1-A, 4.6.1-B, & 4.6.1-C

DRAM SPD INFORMATOION — Fig. 4.6.1-D

MODULE KEYING DEFINITION — Fig. 4.6.1-E

MODULE PIN DEFINITIONS — Fig. 4.6.1-F

X144 SDRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.6.1-G and 4.6.1-H

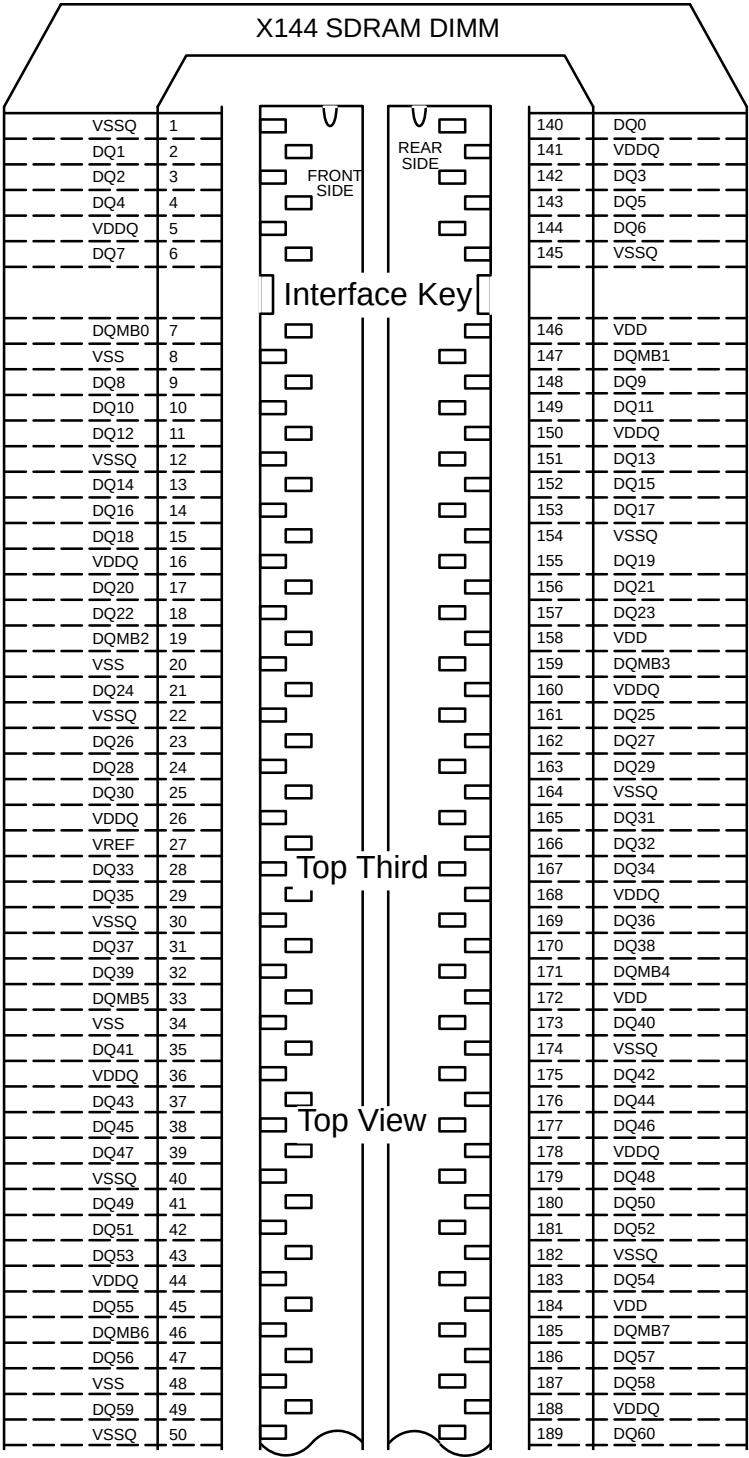


Figure 4.6.1-A
278 PIN X144 SDRAM DIMM PINOUT (TOP THIRD)

Release 7

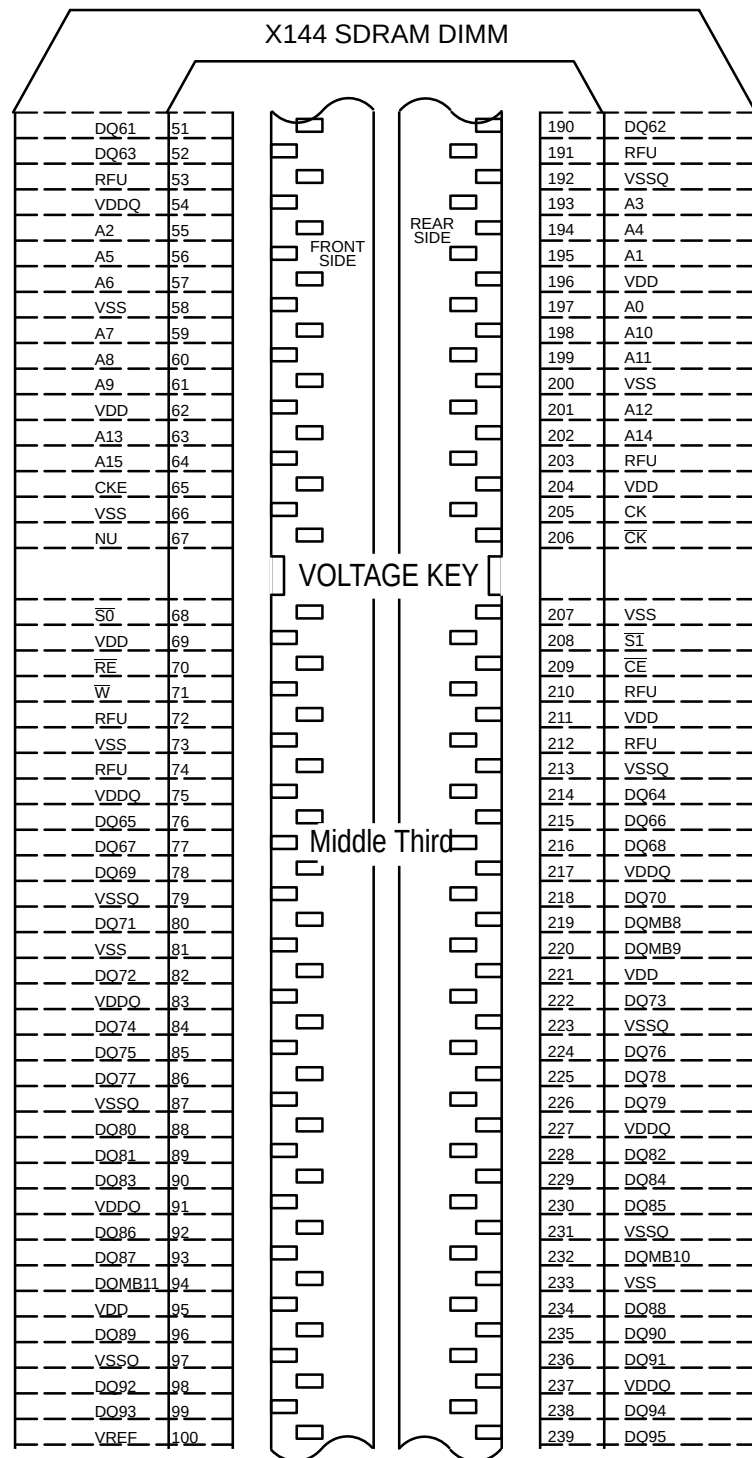


Figure 4.6.1-B
278 PIN X144 SDRAM DIMM PINOUT (MIDDLE THIRD)

Release 7C8