

3.10.3 Word Wide MPDRAM & GRAM

3.10.3.1 - 128K & 256K BY 16 MPDRAM IN SOG WITH MULTIPLE CLOCKS

CAPACITY--256K WORDS OF 16 BITS

LOGIC FEATURES--Multiplexed Address

--SERIAL and RAM data ports

There are two versions of these parts: One with $2\overline{W}$ and the other with $2\overline{CE}$, controlling the lower and upper bytes of data.: 128K & 256K with $2\overline{W}$, 256K with $2\overline{CE}$.

PACKAGE--64 PIN SOG, 12 mm wide, 0.8 mm pin pitch

PIN ASSIGNMENTS--FIG. 3.10.3-1

3.10.3.2 - 128K & 256K BY 16 MPDRAM IN TSOP-2 WITH MULTIPLE CLOCKS

CAPACITY--128K AND 256K WORDS OF 16 BITS

LOGIC FEATURES--Multiplexed Address

--SERIAL and RAM data ports

There are two versions of these parts: One with $2\overline{W}$ and the other with $2\overline{CE}$, controlling the lower and upper bytes of data.: 128K & 256K with $2\overline{W}$, 128K & 256K with $2\overline{CE}$.

PACKAGE--70 PIN TSOP-2 10.16 mm wide (0.400"), 23.49 mm long. 0.65 mm pin pitch

NOTE: These parts have essentially the same pin rotation as the parts defined in Par. 3.10.3.1 with the exception of the addition of NC pins in the middle.

PIN ASSIGNMENTS--FIG. 3.10.3-2

3.10.3.3 - 256K BY 16 SGRAM IN TSOP-2

CAPACITY--256K WORDS OF 16 BITS

LOGIC FEATURES--Multiplexed Address

--A single data port with Graphics oriented features.

--Synchronous address & control interface.

PACKAGE--50 PIN TSOP-2, 10.16 mm wide (0.400"), 0.8 mm PP

PIN ASSIGNMENTS--FIG. 3.10.3-3

NOTE: This part has the same pinout as the SDRAM part shown in Fig. 3.11.4-1 with the exception of the DSF function on P 33.

3.10.3.4 - 128K, 256K, & 512K BY 32, 2 & 4 BANK SGRAM IN QFP or TQFP

CAPACITY--128, 256K, OR 512K WORDS OF 32 BITS WITH 2 OR 4 BANKS

LOGIC FEATURES--Multiplexed Address

--A single data port with Graphics oriented features.

--Synchronous address & control interface.

PACKAGE--100 PIN QFP or TQFP, 20 mm X 14 mm, 0.65 mm PP

PIN ASSIGNMENTS--FIG. 3.10.3-4

NOTE: This part has the same pinout as the SDRAM part shown in Fig. 3.11.4-4 with the exception of the DSF function on P 33.

3.10.3.5 - 256K BY 32 SGRAM IN TSOP2

CAPACITY--256K WORDS OF 32 BITS

LOGIC FEATURES--Multiplexed Address

--A single data port with Graphics oriented features.

--Synchronous address & control interface.

PACKAGE--80 PIN TSOP2, 10.16 mm wide (0.400"), 0.65 mm PP

PIN ASSIGNMENTS--FIG. 3.10.3-5

Release 6c7r9r10

3.10.3.6 - 256K BY 32 SYNCHRONOUS MPDRAM IN TSOP2

CAPACITY--256K WORDS OF 32 BITS

LOGIC FEATURES--Multiplexed Address

- A multiple data port with Graphics oriented features.
- Synchronous address & control interface.

PACKAGE--120 PIN QFP or TQFP, 20 mm X 14 mm, 0.5 mm PP

PIN ASSIGNMENTS--FIG. 3.10.3-5

3.10.3.7 - 256K BY 32 SYNCHRONOUS MPDRAM IN QFP

CAPACITY--256K WORDS OF 32 BITS

LOGIC FEATURES--Multiplexed Address

- A multiple data port with Graphics oriented features.
- Synchronous address & control interface.

PACKAGE--100 PIN QFP or TQFP, 20 mm X 14 mm, 0.65 mm PP

PIN ASSIGNMENTS--FIG. 3.10.3-6

3.10.3.8 - 256K BY 32 MPDRAM IN QFP

CAPACITY--256K WORDS OF 32 BITS

LOGIC FEATURES--Multiplexed Address

- A multiple data port with Graphics oriented features.
- Asynchronous address & control interface.

PACKAGE--100 PIN QFP or TQFP, 20 mm X 14 mm, 0.65 mm PP

PIN ASSIGNMENTS--FIG. 3.10.3-7

3.10.3.9 - 128K, 256K, & 512K BY 32 X 4 BANK SYNCHRONOUS DDR SGRAM IN LQFP

CAPACITY--128K, 256K, & 512K WORDS OF 32 BITS X 4 BANKS

LOGIC FEATURES--Multiplexed Address

- A multiple data port with Graphics oriented features.
- Synchronous address & control interface.

This device will contain all of the logic features described in Sec. 3.11.5 for DDR devices.

PACKAGE--100 PIN LQFP, 20 mm X 14 mm, 0.65 mm PP

PIN ASSIGNMENTS--FIG. 3.10.3-8

3.10.3.10 - 4M BY 32 DDR SGRAM (4 BANK) IN FBGA

CAPACITY--4M WORDS OF 32 BITS Organized as 4 Banks

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM. It can be optionally used as an SDRAM.

PACKAGE--12 X 12 Ball LFBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.10.3-9

BALL LOCATIONS--The package has all balls populated except as noted for the central 16 thermal balls..

3.10.3.11 - 8M BY 32 GDDR3 GRAPHICS RAM IN 144-BALL FBGA

CAPACITY--8M WORDS OF 32 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--12 X 12 Ball LFBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.10.3-10

BALL LOCATIONS--The package has all balls populated except as the noted option for the central 16 thermal balls.

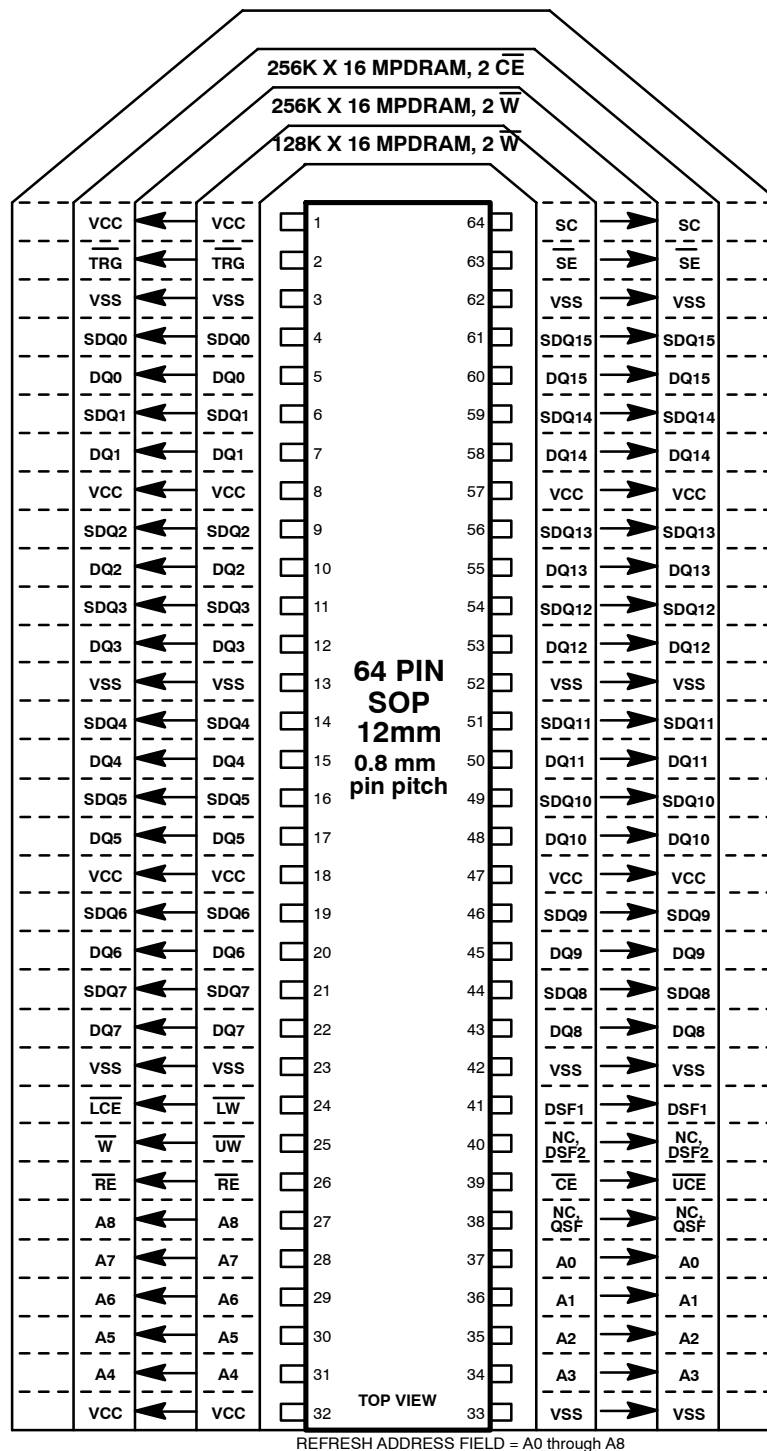
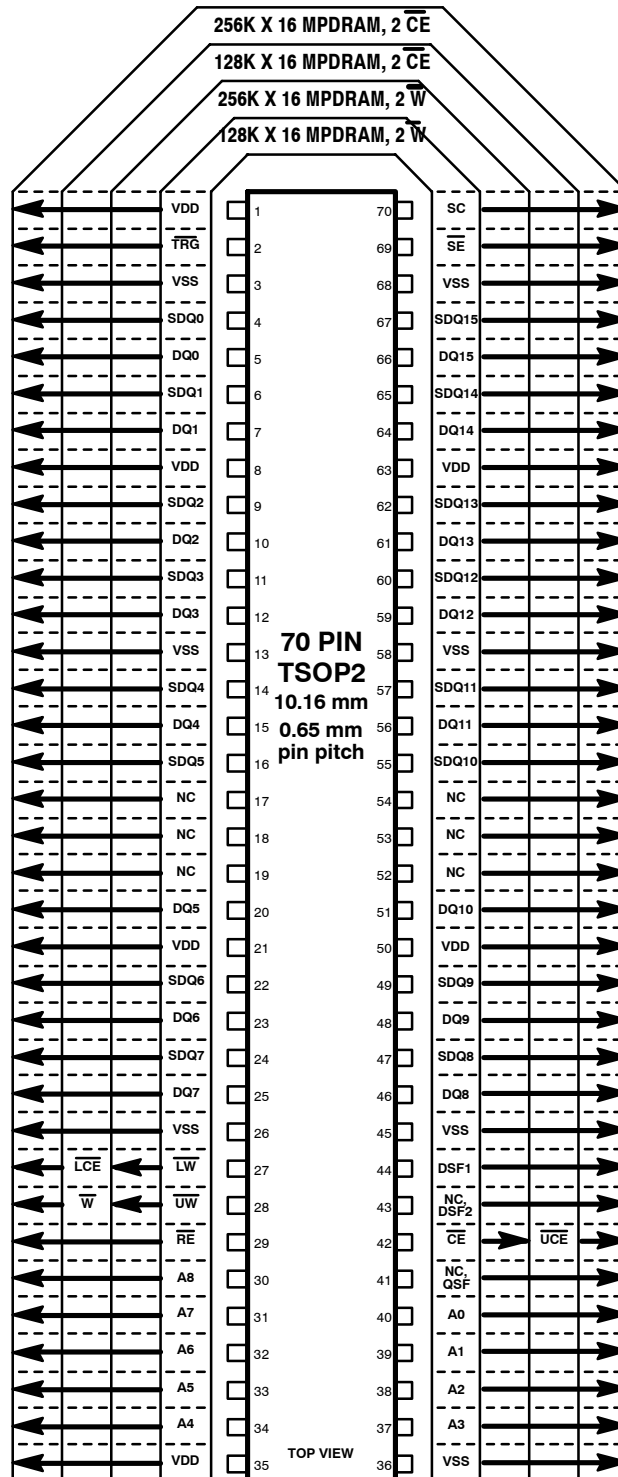


FIGURE 3.10.3-1
128K & 256K BY 16 MPDRAM WITH 2 W
256K BY 16 WITH 2 CE IN SOP

Release 3



REFRESH ADDRESS FIELD = A0 through A8

* NOTE: The JEDEC Std. 30 term for the TSOP-2 package is PDSO-G.

FIGURE 3.10.3-2
128K & 256K BY 16 MPDRAM IN TSOP-2 with 2 $\overline{W}$ & 2 $\overline{CE}$