

3.10.4 MPDRAM Optional Features

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3.10.4.1 – 256K X 4 MPDRAM MINIMUM FEATURE SET TRUTH TABLE

The 256K X 4 MPDRAM described in this Standard must contain, as a minimum, the feature set described in Table 3.10.4–1, 256K X 4 MPDRAM FEATURE SET TRUTH TABLE.

3.10.4.2 – 256K X 4 MPDRAM EXTENDED FEATURE SET TRUTH TABLE

The 256K X 4 MPDRAM described in this Standard, in addition to the minimum feature set defined in Table 3.10.4–1, may contain any of the features described in the Table, 256K X 4 MPDRAM FEATURE SET TRUTH TABLE, and still meet the Standard. These logic features must operate exactly as defined in the table to conform to the Standard.

3.10.4.3 – MPDRAM BIT WRITE OPTIONAL FEATURE

This feature allows individual data bits of a memory array with a multi bit data interface to be selectively modified during a write cycle while other bits remain unchanged. The timing sequence used to control the feature is shown in figure 3.10.4–1 and operates as follows:

- 1–If $\overline{W}$ is low at the time that $\overline{RE}$ goes low, the state of the individual DQ pins determines if that data bit is to be written.
- 2–If DQ is HIGH write is ENABLED for that bit and the data present on DQ at the time that $\overline{CE}$ goes low is written.
- 3–If DQ is LOW, write is DISABLED for that bit and no subsequent writing can occur during that $\overline{RE}$ cycle.
- 4–If $\overline{W}$ is high at the time that $\overline{RE}$ goes low but goes low later in the cycle, a normal write cycle will be performed and all data bits will be written.

3.10.4.4 – 128K X 8 MPDRAM MINIMUM FEATURE SET TRUTH TABLE

The 128K BY 8 MPDRAM described in this standard must contain, as a minimum, the feature set described in Table 3.10.4–2, 128K X 8 MPDRAM FEATURE SET TRUTH TABLE.

3.10.4.5 – 128K X 8 MPDRAM EXTENDED FEATURE SET TRUTH TABLE

The 128K X 8 MPDRAM described in this Standard may, in addition to the minimum feature set defined, contain any of the other features described in Table 3.10.4–2, 128K X 8 MPDRAM FEATURE SET TRUTH TABLE, and still meet the Standard. These logic features must operate exactly as defined in the table to conform to the Standard.

3.10.4.6 – 128K X 16, 256K X 8, & 256K X 16 MPDRAM MINIMUM FEATURE SET TRUTH TABLE

The 2Mb & 4Mb density MPDRAMs described in this Standard must contain, as a minimum, the feature set described in Table 3.10.4–3, 2Mb & 4Mb MPDRAM FEATURE SET TRUTH TABLE. Note: Release 5 contains a new TRUTH TABLE.

3.10.4.7 – 128K X 16, 256K X 8, & 256K X 16 MPDRAM EXTENDED FEATURE SET TRUTH TABLE INCLUDING REQUIRED MINIMUM OPTIONAL FEATURE SET

The 2Mb & 4Mb density MPDRAMs described in this Standard must, in addition to the minimum basic feature set defined in Par. 3.10.4.6, contain all of the minimum defined set of optional features if any of them are included. In addition, any of the other features described may be included. The basic and optional features are shown in Table 3.10.4–3, 2Mb & 4Mb MPDRAM FEATURE SET TRUTH TABLE. These logic features must operate exactly as defined in the table to conform to the Standard. Note: Release 5 contains a new TRUTH TABLE.

3.10.4.8 – SPLIT REGISTER WITH PROGRAMMABLE STOPS FOR MPDRAM

This standard describes an option internal architectural feature which is applicable to the SERIAL PORT in MPSRAMs. The details are shown in Figure 3.10.4–2.

3.10.4.9 – PIPELINED FAST PAGE MODE FOR MPDRAM

This standard describes the operational characteristics of an optional serial access data mode for the RAM PORT of MPDRAMs. The details and timing diagrams are given in Figures 3.10.4–3A and 3.10.4–3B.

3.10.4.10 – EXTENDED DATA OUT FAST PAGE MODE FOR MPDRAM

The EXTENDED DATA OUT FAST PAGE MODE defined in Sec. 3.9.5, DRAM OPTIONAL Features, on Page 3.9.5–11, Par. 1.4 is also applicable to MPDRAM as is needed. The mode is further defined with timing diagrams in Fig. 3.10.4–4.

3.10.4.11 – SAM OPTIONS FOR 4Mb MPDRAM

For 4 Mb MPDRAMs organized as 256K x 16, there are two options for the length of the SAM (Serial Access Memory). It may be either (1), 256 (Half SAM) or (2), 512 bits (Full SAM) for a 512 Column Page Depth. The details of these two options are described in Figs. 3.10.4–5A and 3.10.4–5B.

3.10.4.12 – Synchronous GRAM Special Mode Set Procedure

This standard defines a procedure for setting SPECIAL OPERATIONAL MODES into a Synchronous Graphics DRAM. A timing diagram and logic truth table are given in Fig. 3.10.4–6 on Page 3.10.4–15.

3.10.4.13 – Synchronous MPDRAM Special Mode Set Procedure

This standard defines a procedure for setting SPECIAL OPERATIONAL MODES into a Synchronous Multiport DRAM. A timing diagram and logic truth table are given in Fig. 3.10.4–7 on Page 3.10.4–16.

3.10.4.14 – Synchronous GRAM OPERATIONAL FUNCTION TABLES

This standard gives a set of functional truth tables for Synchronous Graphics DRAM. Three truth tables are given that define all standard operational functions. They are given in Tables 3.10.4–4A⇒C on Pages 3.10.4–17⇒19.

3.10.4.15 – 8Mb MPDRAM FEATURE SET FUNCTION TABLE

The 8Mb MPDRAM described in this Standard must contain, as a minimum, the feature set described in Table 3.10.4–15 on Page 3.10.4–8. This standard applies to devices with any interface data word length.

3.10.4.16 – Extended Functions for SGRAM and MPDRAM.

These standards define two special write function operations for SGRAM and MPDRAM. The functions defined are:

Write–Per–Bit
Block Write

These logic features must operate exactly as defined in the table to conform to the Standard. Details of the standards are given on Page 3.10.4–6.

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256K BY 4 MPDRAM FEATURE SET TRUTH TABLE
TABLE 3.10.4-1

CYCLE	RE					CE	A(n)		DQ(n)			WRITE	RASTER	REGISTER			FUNCTION
CODE	CE	TRG	W	DSF	SE	DSF	RE	CE	RE	CE	CE, W	MASK	OP'N	WM1	WM2	COLOR	
Mandatory Features																	
RT	1	0	1	0	X	X	ROW	TAP +MSB	X	X	X	X	X	X	X	X	READ TRANSFER CYCLE
RW	1	1	1	0	X	0	ROW	COL	X	–	DATA INPUT	NO	YES	X	USE	X	READ WRITE CYCLE (NO MASK)
RWNM	1	1	0	0	X	0	ROW	COL	WM1	–	DATA INPUT	NEW WM1	X	LOAD USE	X	X	READ WRITE CYCLE (NEW MASK DATA)
CBR	0	X	1	X	X	—	X	—	X	–	X	X	X	X	X	X	CE BEFORE RE REFRESH
Optional Features																	
SWT	0	0	0	1	X	–	ROW	–	X	–	X	OLD	X	USE	X	X	SELECTIVE SPLIT WRITE TRANSFER CYCLE (OLD MASK)
LS	0	1	0	X	X	–	CODE	–	WM2	–	X	X	SET-UP	X	X	X	LOGIC SET-UP CYCLE (RASTER OPERATION CODE)
MWT	1	0	0	0	0	X	ROW	TAP +MSB	WM1	X	X	NEW WM1	X	LOAD USE	X	X	MASK WRITE TRANSFER (NEW MASK)
PWT	1	0	0	0	1	X	ROW	TAP +MSB	WM1	X	X	NEW WM1	X	LOAD	X	X	PSEUDO WRITE TRANSFER CYCLE
FWT	1	0	0	1	X	X	ROW	X	WM1	X	X	NEW WM1	X	LOAD USE	X	USE	FLASH WRITE WITH MASK (NEW MASK DATA)
SRT	1	0	1	1	X	X	ROW	TAP +MSB	X	X	X	X	X	X	X	X	SPLIT READ TRANSFER CYCLE
RWCM	1	1	0	1	X	0	ROW	COL	X	–	DATA INPUT	OLD WM1	X	USE	X	X	READ WRITE CYCLE (OLD MASK DATA)
LWR	1	1	1	1	X	0	ROW	COL	X	–	WM1	X	X	LOAD	X	X	LOAD WRITE MASK 1 REGISTER
BWNM	1	1	0	0	X	1	ROW	COL CA2–8	WM1	COL SEL	–	NEW WM1	X	LOAD USE	X	USE	BLOCK WRITE CYCLE (NEW MASK DATA)
BWCM	1	1	0	1	X	1	ROW	COL CA2–8	X	COL SEL	–	OLD WM1	X	USE	X	USE	BLOCK WRITE CYCLE (OLD MASK DATA)
BW	1	1	1	0	X	1	ROW	COL CA2–8	X	COL SEL	–	NO	X	X	X	USE	BLOCK WRITE (NO MASK)
LCR	1	1	1	1	X	1	ROW	COL	X	–	COLOR	X	X	X	X	LOAD	LOAD COLOR REGISTER

256K BY 4 MPDRAM FEATURE SET TRUTH TABLE

128K BY 8 MPDRAM FEATURE SET TRUTH TABLE

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TABLE 3.10.4-2

CYCLE	RE					CE	A(n)		DQ(n)			WRITE	RASTER	REGISTER			FUNCTION
CODE	CE	TRG	W	DSF	SE	DSF	RE	CE	RE	CE	CE, W	MASK	OP'N	WM1	WM2	COLOR	
Mandatory Features																	
RT	1	0	1	0	0	0	ROW	TAP +MSB	0	0	0	0	0	0	0	0	READ TRANSFER CYCLE
RW	1	1	1	0	0	0	ROW	COL	0	–	DATA INPUT	NO	YES	0	USE	0	READ WRITE CYCLE (NO MASK)
RWNM	1	1	0	0	0	0	ROW	COL	WM1	–	DATA INPUT	NEW WM1	0	LOAD USE	0	0	READ WRITE CYCLE (NEW MASK DATA)
CBR	0	0	1	0	0	—	0	—	0	–	0	0	0	0	0	0	CE BEFORE RE REFRESH
Optional Features																	
SWT	0	0	0	1	0	–	ROW	–	0	–	0	OLD	0	USE	0	0	SELECTIVE SPLIT WRITE TRANSFER CYCLE (OLD MASK)
LS	0	1	0	0	0	–	CODE	–	WM2	–	0	0	SET-UP	0	0	0	LOGIC SET-UP CYCLE (RASTER OPERATION CODE)
MWT	1	0	0	0	0	0	ROW	TAP +MSB	WM1	0	0	NEW WM1	0	LOAD USE	0	0	MASK WRITE TRANSFER (NEW MASK)
PWT	1	0	0	0	1	0	ROW	TAP +MSB	WM1	0	0	NEW WM1	0	LOAD	0	0	PSEUDO WRITE TRANSFER CYCLE
FWT	1	0	0	1	0	0	ROW	0	WM1	0	0	NEW WM1	0	LOAD USE	0	USE	FLASH WRITE WITH MASK (NEW MASK DATA)
SRT	1	0	1	1	0	0	ROW	TAP +MSB	0	0	0	0	0	0	0	0	SPLIT READ TRANSFER CYCLE
RWCM	1	1	0	1	0	0	ROW	COL	0	–	DATA INPUT	OLD WM1	0	USE	0	0	READ WRITE CYCLE (OLD MASK DATA)
LWR	1	1	1	1	0	0	ROW	COL	0	–	WM1	0	0	LOAD	0	0	LOAD WRITE MASK 1 REGISTER
BWNM	1	1	0	0	0	1	ROW	COL CA2–8	WM1	COL SEL	–	NEW WM1	0	LOAD USE	0	USE	BLOCK WRITE CYCLE (NEW MASK DATA)
BWCM	1	1	0	1	0	1	ROW	COL CA2–8	0	COL SEL	–	OLD WM1	0	USE	0	USE	BLOCK WRITE CYCLE (OLD MASK DATA)
BW	1	1	1	0	0	1	ROW	COL CA2–8	0	COL SEL	–	NO	0	0	0	USE	BLOCK WRITE (NO MASK)
LCR	1	1	1	1	0	1	ROW	COL	0	–	COLOR	0	0	0	0	LOAD	LOAD COLOR REGISTER

128K BY 8 MPDRAM FEATURE SET TRUTH TABLE

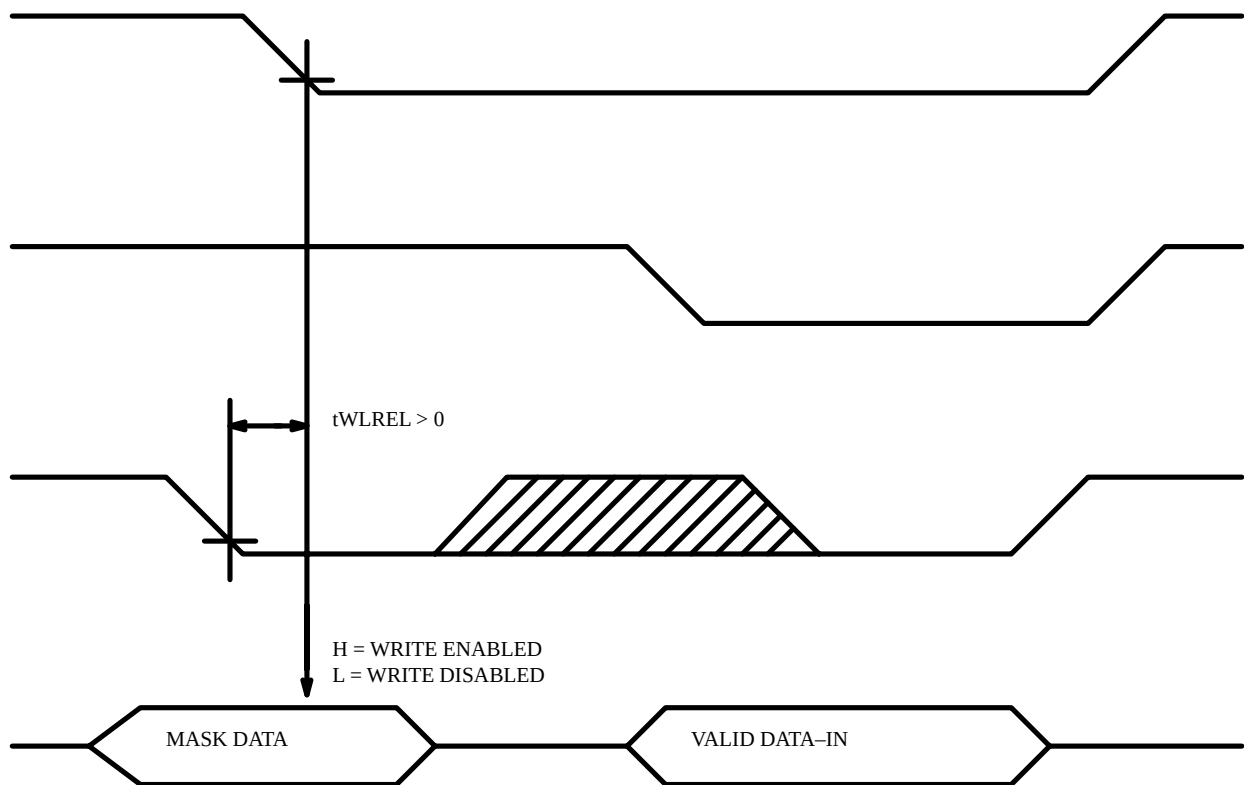


FIGURE 3.10.4-1
BIT WRITE TIMING