

### **3.6.3 - Low Power Double Data Rate (LPDDR) Non-Volatile Memory (NVM)**

**- 256 Mb (16Mx16) through 256 Gb (16Gx16)**

## Contents

|                                                              |    |
|--------------------------------------------------------------|----|
| 1 SCOPE .....                                                | 4  |
| 2 FEATURES.....                                              | 5  |
| 3 GENERAL DESCRIPTION .....                                  | 5  |
| 4 TERMINOLOGY DEFINITIONS.....                               | 9  |
| 5 FUNCTIONAL DESCRIPTION .....                               | 9  |
| 5.1 INITIALIZATION.....                                      | 10 |
| 5.2 WARM-RESET .....                                         | 11 |
| 5.3 REGISTER DEFINITION.....                                 | 13 |
| 5.3.1 MODE REGISTER .....                                    | 13 |
| 5.3.1.1 BURST LENGTH.....                                    | 14 |
| 5.3.1.2 BURST TYPE.....                                      | 16 |
| 5.3.1.3 READ LATENCY .....                                   | 16 |
| 5.3.2 EXTENDED MODE REGISTER.....                            | 17 |
| 5.3.2.1 OUTPUT DRIVE STRENGTH.....                           | 17 |
| 5.3.3 MODE REGISTER 11 .....                                 | 18 |
| 5.3.3.1 OVERLAY WINDOW BASE ADDRESS.....                     | 18 |
| 5.3.3.2 OVERLAY WINDOW ENABLE .....                          | 18 |
| 5.3.3.3 FLUSH.....                                           | 18 |
| 5.3.3.4 DEVICE AUTO-INITIALIZATION.....                      | 18 |
| 5.3.4 SRR READ-ONLY REGISTERS.....                           | 20 |
| 5.3.4.1 SRR REGISTER 0 (Address 0000h) .....                 | 21 |
| 5.3.4.2 SRR REGISTER 17 (Address 0011h) .....                | 22 |
| 5.3.4.3 SRR REGISTERS 18 and 19 (Addresses 0012h-0013h)..... | 23 |
| 6 COMMANDS .....                                             | 24 |
| 7 ADDRESSING .....                                           | 30 |
| 7.1 Three-Phase Address .....                                | 30 |
| 7.2 Logical To Physical Map.....                             | 30 |
| 8 OPERATION .....                                            | 32 |
| 8.1 DESELECT .....                                           | 32 |
| 8.2 NO OPERATION.....                                        | 32 |
| 8.3 MODE REGISTER SET .....                                  | 33 |
| 8.4 SRR Command Sequence.....                                | 34 |
| 8.5 PREACTIVE .....                                          | 35 |
| 8.6 AUTO PRECHARGE.....                                      | 36 |
| 8.7 ACTIVE.....                                              | 36 |
| 8.8 READ.....                                                | 38 |
| 8.8.1 READ to READ .....                                     | 40 |
| 8.8.2 READ BURST TERMINATE .....                             | 40 |
| 8.8.3 READ to WRITE .....                                    | 40 |
| 8.8.4 READ to PREACTIVE or ACTIVE .....                      | 40 |
| 8.9 BURST TERMINATE .....                                    | 45 |
| 8.10 WRITE.....                                              | 46 |
| 8.10.1 WRITE to WRITE.....                                   | 48 |
| 8.10.2 WRITE to READ .....                                   | 48 |
| 8.10.3 WRITE to PREACTIVE or ACTIVE: .....                   | 48 |
| 8.11 POWER-DOWN.....                                         | 55 |
| 8.11.1 POWER-DOWN WITH CLOCK STOP .....                      | 56 |
| 8.12 CLOCK STOP (during Active and Idle States).....         | 57 |
| 8.13 DEEP POWER-DOWN.....                                    | 58 |
| 8.14 LATENCY SUMMARY: .....                                  | 58 |

Contents

9 ABSOLUTE MAXIMUM RATINGS ..... 59

10 AC & DC OPERATING CONDITIONS ..... 60

    10.1 DRIVER CHARACTERISTICS ..... 70

ANNEX A - SOFTWARE EXAMPLES ..... 72

## 1 SCOPE

This document defines the Low Power Double Data Rate (LPDDR) NVM specification, including features, functionality, AC and DC characteristics, packages, and pin assignments.

The purpose of this Specification is to define the minimum set of requirements for JEDEC compliant Low Power Double Data Rate NVM devices. System designs based on the required aspects of this specification will be supported by all LPDDR NVM vendors providing compliant devices.

This specification was created based on preliminary drafts of the LPDDR-333 SDRAM specification (JEDEC committee ballots JC-42.3-05-373 and -357 and -355 and -261, and JC-42.3-04-391). Each aspect of the changes for NVM operation were considered and balloted by JC-42.4. DDR370 and DDR400 speed bins were balloted by JC-42.6. The accumulation of these ballots were then incorporated to prepare this LPDDR NVM specification.

## 2 FEATURES

- Double-data rate architecture; two data transfers per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver
- Differential clock inputs (CK and  $\overline{\text{CK}}$ )
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Four internal Row-Data-Buffers (RDBs) for pipelining tRCD during data bursts
- Data mask (DM) for write data
- Burst Length: 4 or 8 or 16
- Burst Type: Sequential
- CAS latency: 3 (2 and 4 are optional)
- Clock Stop capability during idle periods
- Configurable Drive Strength
- LV-CMOS compatible inputs
- VDD and VDDQ: 1.8 +/- 0.1V

## 3 GENERAL DESCRIPTION

The LPDDR NVM uses a double data rate architecture to achieve high speed operation. The double data rate architecture is essentially a 2n prefetch architecture internally with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the LPDDR NVM effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal NVM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the LPDDR NVM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center aligned with data for WRITEs.

The LPDDR NVM operates from a differential clock (CK and  $\overline{\text{CK}}$ : the crossing of the CK going high and  $\overline{\text{CK}}$  going low will be referred to as the positive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered at both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the LPDDR NVM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a sequential sequence. Accesses begin with the registration of an optional PREACTIVE command and a required ACTIVE command, which is then followed by a READ or WRITE command. The address and BA bits registered coincident with the PREACTIVE and ACTIVE commands are used to select the row to be accessed and the Row-Data-Buffer which will store sensed data. The address and BA bits registered coincident with the READ or WRITE command are used to select the Row-Data-Buffer and the starting column location for the burst access.

The LPDDR NVM provides for programmable read or write bursts of 4 or 8 or 16 locations.

The pipelined bus protocol may utilize the four Row-Data-Buffers of LPDDR NVMs, thereby providing high effective bandwidth by hiding row activation times. The protocol allows interleaving commands between LPDDR NVMs and LPDDR SDRAMs on a shared bus, contingent on proper signal-integrity design.

A CKE pin controls the power saving Power-down mode.

All inputs are LV-CMOS compatible. Devices will have a VDD and VDDQ supply of 1.8V (nominal).

This datasheet includes all features and functionality required for JEDEC LPDDR NVM devices. Certain vendors may elect to offer a superset of this specification by offering improved timings and/or including optional features. Users benefit from knowing that any system design based on the required aspects of the specification are supported by all LPDDR NVM vendors; conversely users seeking to use any superset specifications bear the responsibility to verify support with individual vendors.

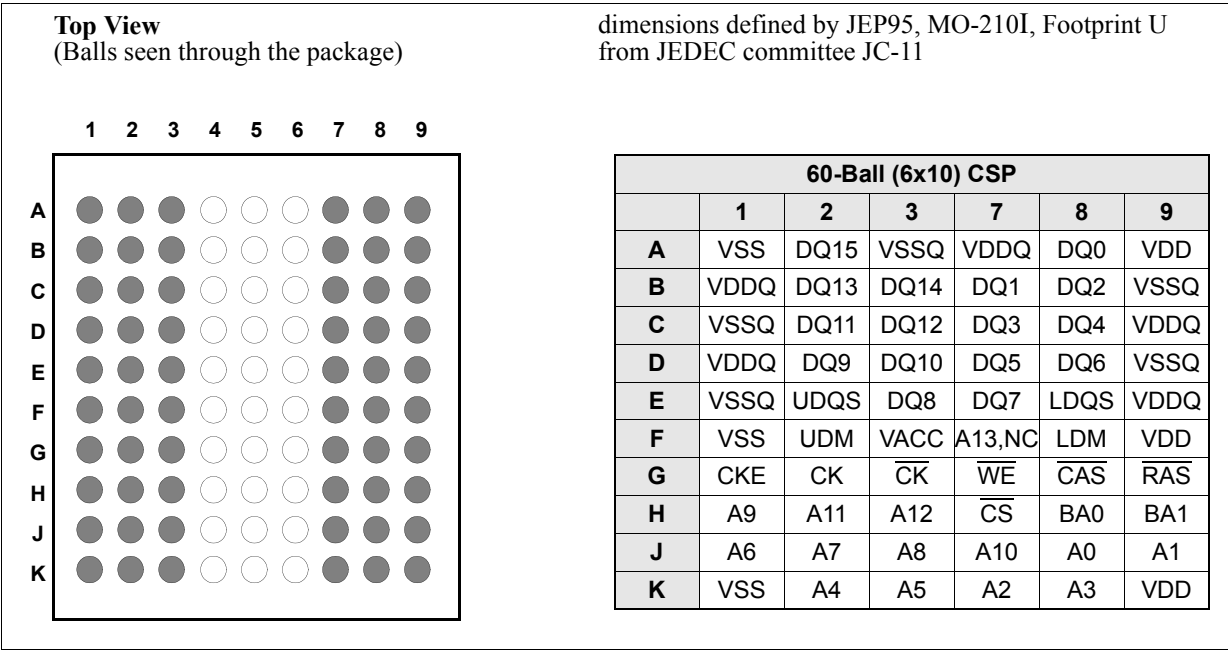
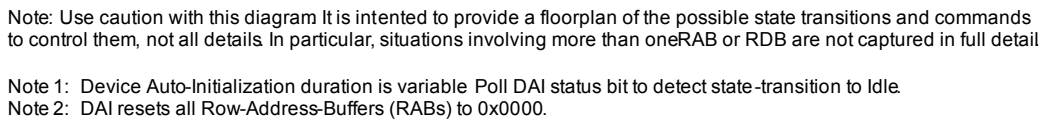


Table 1 Pin Descriptions

| Symbol                                                                     | Type   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|----------------------------------------------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CK, $\overline{\text{CK}}$                                                 | Input  | Clock: CK and $\overline{\text{CK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{\text{CK}}$ . Input and output data is referenced to the crossing of CK and $\overline{\text{CK}}$ (both directions of crossing). Internal clock signals are derived from CK/ $\overline{\text{CK}}$ .                                     |
| CKE                                                                        | Input  | Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides IDLE POWER-DOWN (all RDBs idle), or ACTIVE POWER-DOWN (row ACTIVE in one or more RDBs). CKE is synchronous for all functions. Input buffers, excluding CK, $\overline{\text{CK}}$ and CKE, are disabled during power-down mode which is contrived for low standby power consumption. |
| $\overline{\text{CS}}$                                                     | Input  | Chip Select: $\overline{\text{CS}}$ enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external bank selection on systems with multiple banks. $\overline{\text{CS}}$ is considered part of the command code.                                                                                         |
| $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ | Input  | Command Inputs: $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$ ) define the command being entered.                                                                                                                                                                                                                                                                         |
| LDM, UDM                                                                   | Input  | Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading matches the DQ and DQS loading.<br>For x16 devices, LDM corresponds to the data on DQ0-DQ7, UDM corresponds to the data on DQ8-DQ15.                                                         |
| BA0, BA1                                                                   | Input  | Bank Address Inputs: BA0 and BA1 define to which RAB and/or RDB a PREAMP, ACTIVE, READ, or WRITE command is being applied. Also used to select between SRR command sequence, and regular Mode Register Set command. Also used to select between Mode Register, Extended Mode Register, of Mode Register 11 during MRS command.                                                                                                              |
| A[n : 0]                                                                   | Input  | Address Inputs: provide the row address during PREAMP and ACTIVE commands, and the column address during READ / WRITE commands, to select one location out of the memory array or overlay window. The address inputs also provide the opcode during a MODE REGISTER SET command, and also select a register to read during the SRR command sequence. Thirteen pins (A0 - A12) are used for densities 16 Gbit and smaller.                   |
| DQ0-DQ15                                                                   | I/O    | Data Bus: Input / Output                                                                                                                                                                                                                                                                                                                                                                                                                    |
| LDQS, UDQS                                                                 | I/O    | Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered with write data. Used to capture write data.<br>For x16 device, LDQS corresponds to the data on DQ0-DQ7, UDQS corresponds to the data on DQ8-DQ15.                                                                                                                                                                                         |
| NC                                                                         | —      | No Connect: No internal electrical connection is present                                                                                                                                                                                                                                                                                                                                                                                    |
| VDDQ                                                                       | Supply | I/O Power Supply                                                                                                                                                                                                                                                                                                                                                                                                                            |
| VSSQ                                                                       | Supply | I/O Ground                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| VDD                                                                        | Supply | Power Supply                                                                                                                                                                                                                                                                                                                                                                                                                                |
| VSS                                                                        | Supply | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| VACC                                                                       | Supply | Power Supply for Factory Acceleration of some Array Operations                                                                                                                                                                                                                                                                                                                                                                              |



### Figure 3: Simplified Bus Interface State Diagram

## 4 TERMINOLOGY DEFINITIONS

The following are the definitions of the terms LPDDR200, LPDDR266, and LPDDR333 as used in this specification

**LPDDR200:** A speed grade for LPDDR-NVM devices. The nominal operating (clock) frequency of such devices is 100 MHz. This means that although the device operates over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 100 MHz clock frequency. The corresponding nominal data transfer rate is 200 Million Transfers per Second per pin (MTS).

**LPDDR266:** A speed grade for LPDDR-NVM devices. The nominal operating (clock) frequency of such devices is 133 MHz. This means that although the device operates over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 133 MHz clock frequency. The corresponding nominal data transfer rate is 266 MTS.

**LPDDR333:** A speed grade for LPDDR-NVM devices. The nominal operating (clock) frequency of such devices is 166 MHz. This means that although the device operates over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 166 MHz clock frequency. The corresponding nominal data transfer rate is 333 MTS.

**LPDDR370:** A speed grade for LPDDR-NVM devices. The nominal operating (clock) frequency of such devices is 185 MHz. This means that although the device operates over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 185 MHz clock frequency. The corresponding nominal data transfer rate is 370 MTS.

**LPDDR400:** A speed grade for LPDDR-NVM devices. The nominal operating (clock) frequency of such devices is 200 MHz. This means that although the device operates over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 200 MHz clock frequency. The corresponding nominal data transfer rate is 400 MTS.

## 5 FUNCTIONAL DESCRIPTION

The Low Power Double Data Rate (LPDDR) Non-Volatile Memory (NVM) is intended to operate in harmony with LPDDR SDRAM memories on either the same bus interface or on a separate instantiation (i.e. copy) of the same bus interface. By combining NVM and Volatile Memory devices on the same interface, the number of memory interfaces can be reduced. By placing NVM on a separate instantiation of the same LPDDR interface, the system design complexity and validation effort can be reduced.

LPDDR NVMs may be produced by different vendors using different memory technologies, and therefore the product families may offer a variety of densities, row sizes, and tRCD latencies. However, this specification defines common methods for power-up initialization, bootmode, and address assignments. Some LPDDR NVMs may support software eXecution In Place (XIP) directly from the NVM on the LPDDR SDRAM interface which is already present in many systems.

The LPDDR NVM uses a double data rate architecture to achieve high speed bus operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. The LPDDR protocol allows pipelining of initial access latency within individual memories as well as among different memories using a shared bus.

Read and write accesses to the LPDDR NVM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses may begin with a PREACTIVE command to deliver part of the Row Address to one of four Row-Address-Buffers (RABs) in the NVM. Accesses also utilize an ACTIVE command, which delivers the remainder of the Row Address and starts internal sensing of the selected row to fill one of four Row-Data-Buffers (RDBs) in the NVM. After tRCD latency (which may vary among vendors and products), a READ (or WRITE) command invokes a read-burst from (or a write-burst to) one of the four RDBs, starting at the column location addressed by the READ (or WRITE) command.

LPDDR NVM uses only Address pins to select a memory location within the core memory array. BA1 and BA0 do not select 25% of the array. Rather, BA1 and BA0 are used to select 1 of 4 Row-Address-Buffers (RABs), and 1 of 4 Row-Data-Buffers (RDBs), independent of core memory array address to increase the opportunity to pipeline tRCD, and to allow 4 rows anywhere in the array to be kept open for fast access by pipelined burst READ or WRITE commands.

Prior to normal operation, the LPDDR NVMs must be initialized. The following sections provide detailed information covering device initialization, register definition, command description, addressing, and device operation.

## 5.1 INITIALIZATION

LPDDR NVMs must be powered up and initialized in a predefined manner. Initialization procedures other than those specified may result in undefined operation. If there is any interruption to the device power, the initialization routine should be followed. Parts of the initialization sequence shall also be used to perform a warm-reset of the NVM when the memory controller is reset.

LPDDR NVMs shall include a Device Auto-Initialization mechanism. Device Auto-Initialization loads the mode registers with default values, and may invoke additional reset procedures within the memory. The memory controller shall invoke Device Auto-Initialization as specified below in Steps 11 through 14.

Every LPDDR NVM shall support, but shall not require, the initialization steps as specified in JEDEC LPDDR SDRAM standard N05-DR36. However, LPDDR NVMs require additional initialization steps beyond the SDRAM. The steps to be followed for device initialization are listed below. The Initialization Flow Diagram is shown in Figure 4, and the Initialization Flow Waveform Sequence in Figure 5.

The clock stop feature is not available until the device has been properly initialized from Step 1 through Step 13.

- Step 1 Provide power, the device core power (VDD) and the device I/O power (VDDQ) must be brought up simultaneously to prevent device latch-up. Although not required, it is recommended that VDD and VDDQ are from the same power source. While VDD and VDDQ are raised, CKE shall be driven at any voltage between VIL MIN and VIH MAX. After VDD and VDDQ are valid, CKE shall be driven at the VIH logic high level.
- Step 2 Once the system has established consistent device power and CKE is driven high, it is safe to apply stable clock with a frequency in compliance with  $t_{CKBOOT}$ . Clock shall not stop until after step 13. (After step 2, the NVM shall be ready to receive LPDDR-NVM bus commands. However, the NVM need not be ready for Active operations until step 15.)
- Step 3 Optionally, issue NOP or DESELECT commands for at least 200 us.  
(The memory shall allow but shall not require this optional step, which provides backward compatibility with the LPDDR SDRAM initialization procedure.)
- Steps 4 and 5  
Optionally, issue a PRACTIVE command with A10 driven high and provide NOP or DESELECT commands for at least  $t_{RP}$  time.  
(The memory shall allow but shall not require these optional steps, which provides backward compatibility with the LPDDR SDRAM initialization procedure.)
- Step 6 Optionally, issue an (SDRAM) AUTO REFRESH command followed by NOP or DESELECT commands for at least (SDRAM)  $t_{RFC}$  time. Optionally, issue a second (SDRAM) AUTO REFRESH command followed by NOP or DESELECT commands for at least (SDRAM)  $t_{RFC}$  time. (The memory shall allow but shall not require this optional step, which provides backward compatibility with the LPDDR SDRAM initialization procedure.)  
(Note: step 6 may also occur between steps 10 and 11.)
- Steps 7 and 8  
Optionally, use the MRS command to load the Mode Register and provide NOP or DESELECT commands for at least  $t_{MRD}$  time.  
(The memory shall allow but shall not require these optional steps, which provides backward compatibility with the LPDDR SDRAM initialization procedure. However, the Mode Register value will be overwritten by step 11, so steps 7 and 8 may also occur after step 15.)
- Steps 9 and 10  
Optionally, use the MRS command to load the Extended Mode Register and provide NOP or DESELECT commands for at least  $t_{MRD}$  time.  
(The memory shall allow but shall not require these optional steps, which provides backward compatibility with the LPDDR SDRAM initialization procedure. However, the Extended Mode Register value will be overwritten by step 11, so steps 9 and 10 may also occur after step 15.)  
(Note: steps 9 and 10 may also occur between steps 6 and 7.)
- Step 11 Use the MRS command to set DAI = 1 in Mode Register 11. Then provide NOP or DESELECT commands for at least  $t_{MRD}$  time.  
(When the controller sets DAI = 1, the NVM shall start an internal Device Auto-Initialization process, which keeps DAI = 1 during its variable latency. Immediately after the controller sets DAI = 1, the NVM immediately shall set the Mode Register to the default value, and shall set the Extended Mode Register to the

default value, and shall set the Mode Register 11 to the default value. This overwrites any mode register values which may have been loaded in steps 7 and 9. The NVM shall reset DAI to 0 after it finishes its internal Device Auto-Initialization process.) A controller may repeat steps 7 and 8, and/or steps 9 and 10, after step 15.

- Step 12 Issue MRS command with BA=01 and A=0x12. Then provide NOP or DESELECT commands for at least  $t_{SRR}$  time.
- Step 13 Issue READ command with BA=01 and A=0x12. Then provide NOP or DESELECT commands at least CL times to satisfy  $t_{SRC}$ . Read and test the DAI bit (bit 7) for “1” (still busy) or “0” (ready, Device Auto-Initialization finished).
- Step 14 While DAI = “1” (still busy), continue polling by repeating steps 12 through 14. After DAI = “0”, proceed to step 15. Optionally, the clock may be stopped after step 13 of each polling iteration, but the clock shall be restarted (in compliance with  $t_{CKBOOT}$ ) before returning to step 12.
- Step 15 The NVM has been properly initialized. Continue driving the clock slowly (in compliance with  $t_{CKBOOT}$ ) until Drive Strength is adjusted in the Extended Mode Register to optimize system signal integrity. Device Auto-Initialization (Steps 11 through 14) resets all mode registers to default values, so Steps 7 through 10 may need to be repeated after Step 15.

## 5.2 WARM-RESET

When NVM delivers boot-code after a warm-reset, it is important to reset the NVM when the Memory Controller is also reset. Steps 2 and 3 are recommended (to finish any bursts already in progress), and step 11 through step 15 shall be used to achieve a warm-reset.

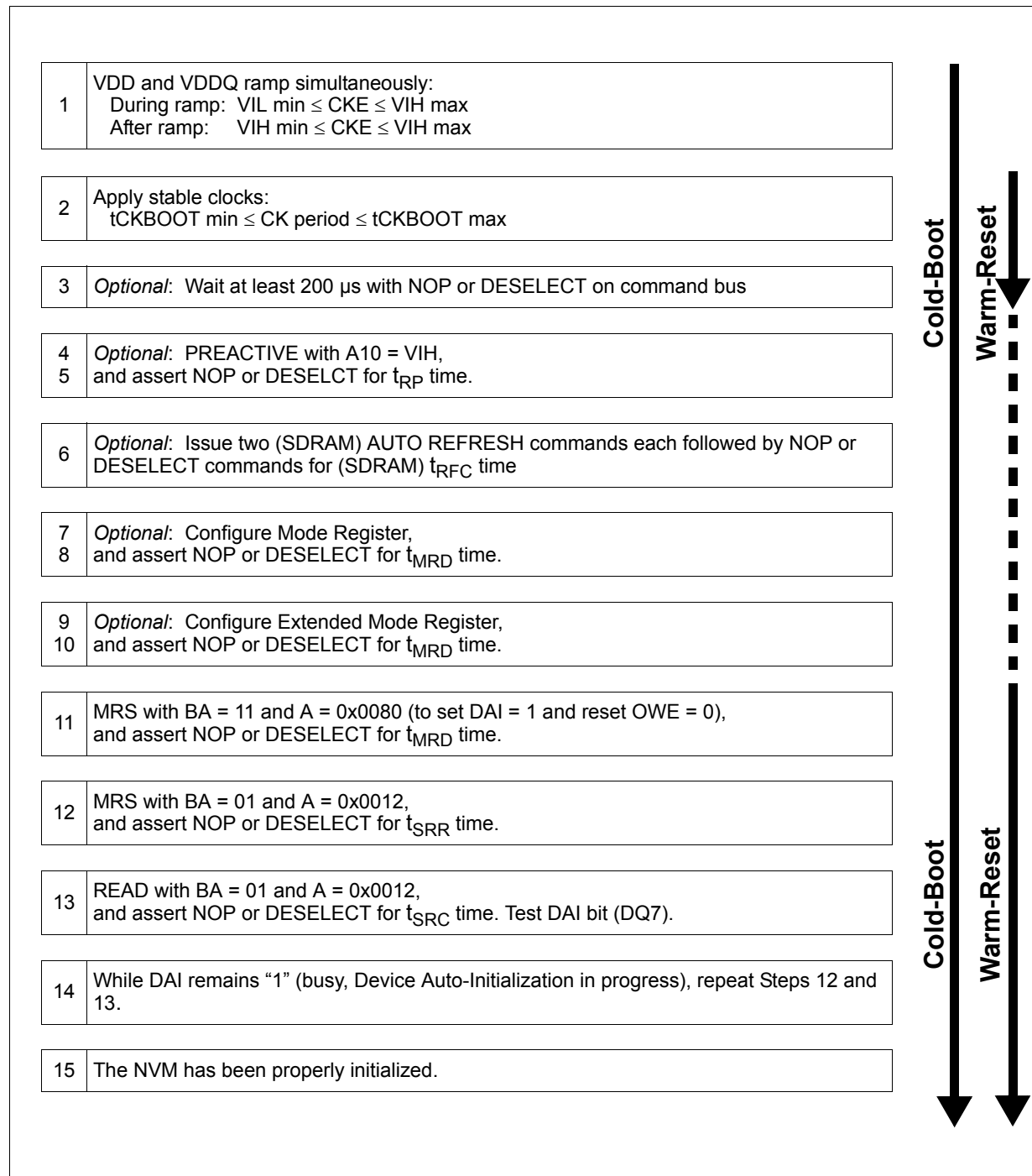


Figure 4: Initialization Flow Diagram

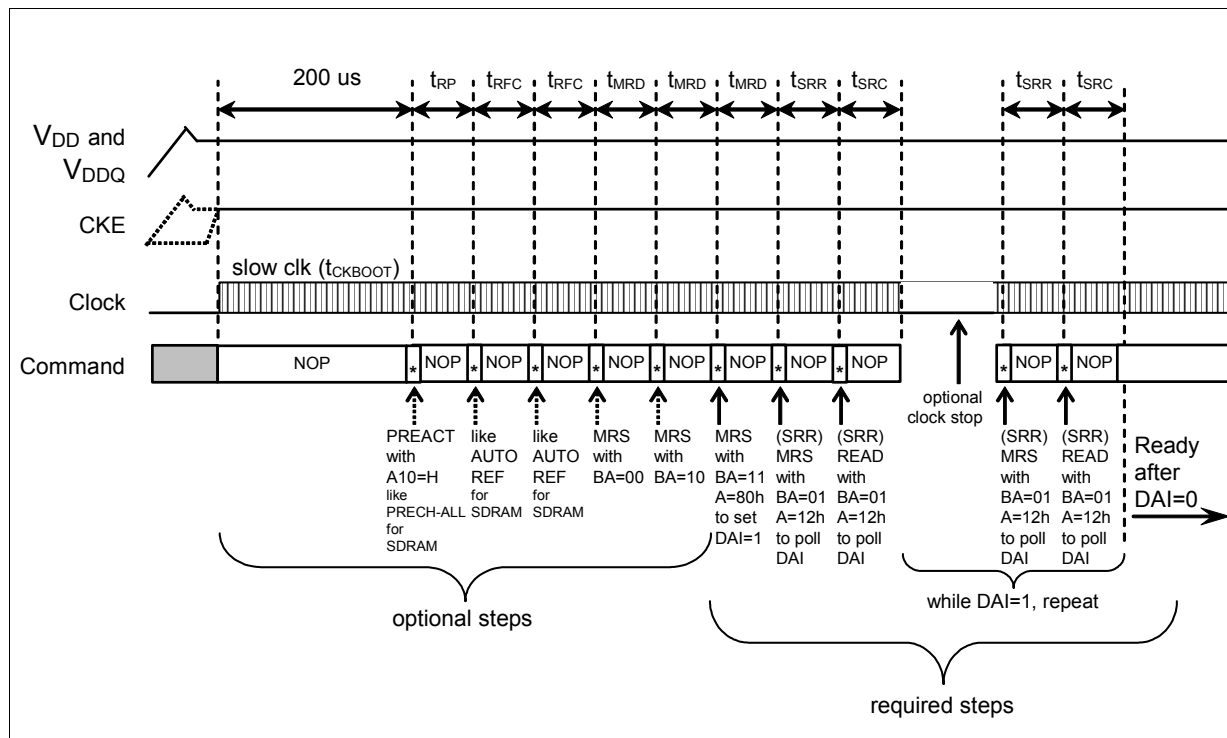


Figure 5: Initialization Flow Waveform Sequence

## 5.3 REGISTER DEFINITION

### 5.3.1 MODE REGISTER

The Mode Register is used to define the specific mode of operation of the LPDDR NVM. This definition includes the definition of a burst length, a burst type, a CAS latency as shown in Figure 6.

The Mode Register is programmed via the MODE REGISTER SET command (with BA0=0 and BA1=0) and will retain the stored information until it is reprogrammed, the device loses power, or DAI is written to "1".

Mode Register bits A0-A2 specify the burst length, A3 the type of burst (sequential only), A4-A6 the CAS latency. A logic 0 should be programmed to all the undefined address bits to ensure future compatibility.

The Mode Register must be loaded when no bursts are in progress, and the controller must wait the specified time  $t_{MRD}$  before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

At the beginning of Device Auto-Initialization, the memory shall set the Mode Register to the default value 0x0032 (CAS Latency = 3, Sequential burst type, BL = 4).

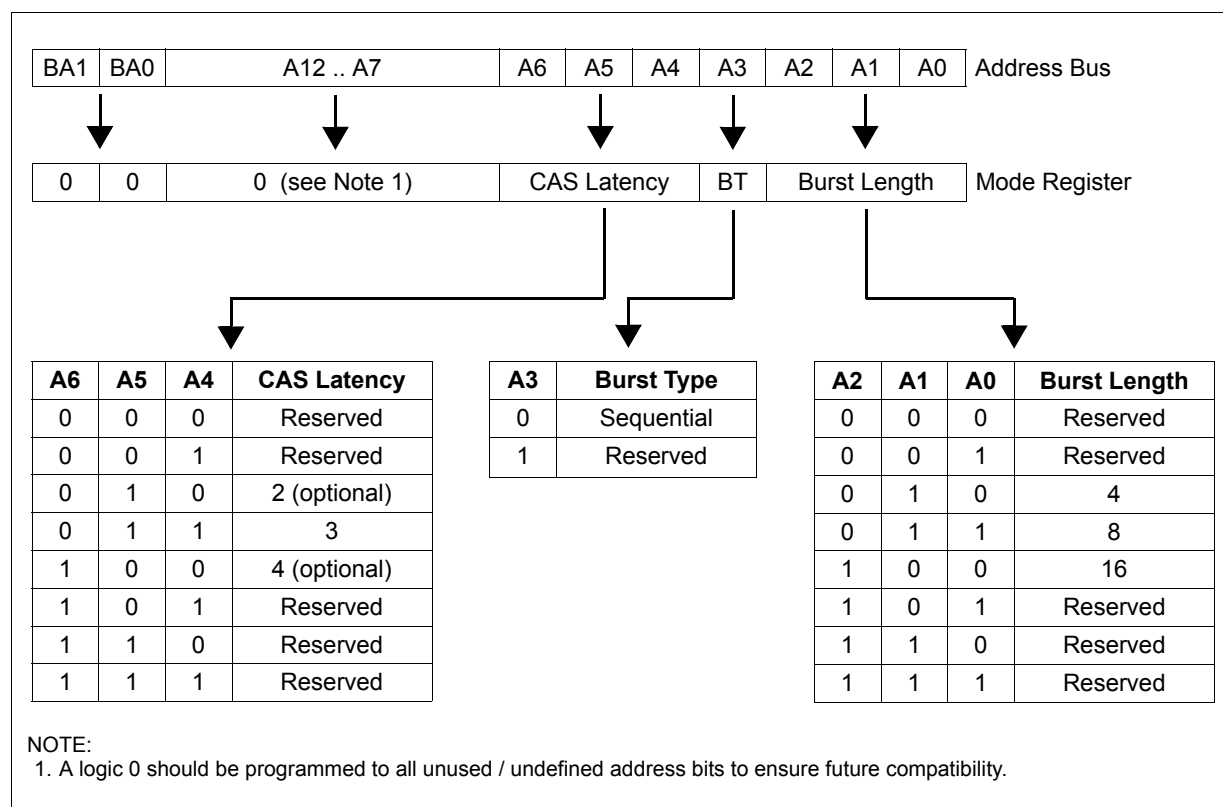


**Figure 6: Mode Register Definition**

### 5.3.1.1 BURST LENGTH

Read and write accesses to the LPDDR NVM are burst oriented, with the burst length being set as in Figure 6, and the burst order as in Table 2.

The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 4, 8 or 16 locations are available for the sequential burst type. “Interleave” burst type is not supported by LPDDR Non-Volatile Memories.

**Table 2 Burst Definition**

| BURST LENGTH | STARTING COLUMN ADDRESS |    |    |    | ORDER OF ACCESSES WITHIN A BURST (HEXADECIMAL NOTATION) |  |
|--------------|-------------------------|----|----|----|---------------------------------------------------------|--|
|              | A3                      | A2 | A1 | A0 | SEQUENTIAL                                              |  |
| 4            |                         |    | 0  | 0  | 0 - 1 - 2 - 3                                           |  |
|              |                         |    | 0  | 1  | 1 - 2 - 3 - 0                                           |  |
|              |                         |    | 1  | 0  | 2 - 3 - 0 - 1                                           |  |
|              |                         |    | 1  | 1  | 3 - 0 - 1 - 2                                           |  |

**Table 2 Burst Definition**

| BURST LENGTH | STARTING COLUMN ADDRESS |    |    |    | ORDER OF ACCESSES WITHIN A BURST (HEXADECIMAL NOTATION) |  |
|--------------|-------------------------|----|----|----|---------------------------------------------------------|--|
|              | A3                      | A2 | A1 | A0 | SEQUENTIAL                                              |  |
| 8            |                         | 0  | 0  | 0  | 0 - 1 - 2 - 3 - 4 - 5 - 6 - 7                           |  |
|              |                         | 0  | 0  | 1  | 1 - 2 - 3 - 4 - 5 - 6 - 7 - 0                           |  |
|              |                         | 0  | 1  | 0  | 2 - 3 - 4 - 5 - 6 - 7 - 0 - 1                           |  |
|              |                         | 0  | 1  | 1  | 3 - 4 - 5 - 6 - 7 - 0 - 1 - 2                           |  |
|              |                         | 1  | 0  | 0  | 4 - 5 - 6 - 7 - 0 - 1 - 2 - 3                           |  |
|              |                         | 1  | 0  | 1  | 5 - 6 - 7 - 0 - 1 - 2 - 3 - 4                           |  |
|              |                         | 1  | 1  | 0  | 6 - 7 - 0 - 1 - 2 - 3 - 4 - 5                           |  |
|              |                         | 1  | 1  | 1  | 7 - 0 - 1 - 2 - 3 - 4 - 5 - 6                           |  |
| 16           | 0                       | 0  | 0  | 0  | 0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F                         |  |
|              | 0                       | 0  | 0  | 1  | 1-2-3-4-5-6-7-8-9-A-B-C-D-E-F-0                         |  |
|              | 0                       | 0  | 1  | 0  | 2-3-4-5-6-7-8-9-A-B-C-D-E-F-0-1                         |  |
|              | 0                       | 0  | 1  | 1  | 3-4-5-6-7-8-9-A-B-C-D-E-F-0-1-2                         |  |
|              | 0                       | 1  | 0  | 0  | 4-5-6-7-8-9-A-B-C-D-E-F-0-1-2-3                         |  |
|              | 0                       | 1  | 0  | 1  | 5-6-7-8-9-A-B-C-D-E-F-0-1-2-3-4                         |  |
|              | 0                       | 1  | 1  | 0  | 6-7-8-9-A-B-C-D-E-F-0-1-2-3-4-5                         |  |
|              | 0                       | 1  | 1  | 1  | 7-8-9-A-B-C-D-E-F-0-1-2-3-4-5-6                         |  |
|              | 1                       | 0  | 0  | 0  | 8-9-A-B-C-D-E-F-0-1-2-3-4-5-6-7                         |  |
|              | 1                       | 0  | 0  | 1  | 9-A-B-C-D-E-F-0-1-2-3-4-5-6-7-8                         |  |
|              | 1                       | 0  | 1  | 0  | A-B-C-D-E-F-0-1-2-3-4-5-6-7-8-9                         |  |
|              | 1                       | 0  | 1  | 1  | B-C-D-E-F-0-1-2-3-4-5-6-7-8-9-A                         |  |
|              | 1                       | 1  | 0  | 0  | C-D-E-F-0-1-2-3-4-5-6-7-8-9-A-B                         |  |
|              | 1                       | 1  | 0  | 1  | D-E-F-0-1-2-3-4-5-6-7-8-9-A-B-C                         |  |
|              | 1                       | 1  | 1  | 0  | E-F-0-1-2-3-4-5-6-7-8-9-A-B-C-D                         |  |
|              | 1                       | 1  | 1  | 1  | F-0-1-2-3-4-5-6-7-8-9-A-B-C-D-E                         |  |

## NOTES:

1. For a burst length of four, A2-An selects the four data element block; A0-A1 selects the first access within the block
2. For a burst length of eight, A3-An selects the eight data element block; A0-A2 selects the first access within the block.
3. For a burst length of sixteen, A4-An selects the sixteen data element block; A0-A3 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence, the following access wraps within the block.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within the block, meaning that the burst will wrap within the block if a boundary is reached.

The block is uniquely selected by A2-An when the burst length is set to 4, by A3-An when the burst length is set to 8, and A4-An when the burst length is set to 16 (where An is the most significant column address bit for a given configuration). The remaining (least significant) address bits are used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

### 5.3.1.2 BURST TYPE

Accesses within a given burst shall be programmed to be sequential; this is referred to as the burst type and is selected via bit A3.

The ordering of accesses within a burst is determined by the burst length and the starting column address, as shown in Table 2.

(“Interleave” burst type is not supported by LPDDR Non-Volatile Memories.)

### 5.3.1.3 READ LATENCY

The READ latency, or CAS latency (CL), is the delay between the registration of a READ command and the availability of the first piece of output data. The latency should be set to 3 clocks. Some vendors may offer an additional option of 2 or 4 clocks.

If a READ command is registered at a clock edge  $n$  and the latency (CL) is 4 clocks, the first data element will be valid at  $n + 3t_{CK} + t_{AC}$ .

If a READ command is registered at a clock edge  $n$  and the latency (CL) is 3 clocks, the first data element will be valid at  $n + 2t_{CK} + t_{AC}$ .

If a READ command is registered at a clock edge  $n$  and the latency (CL) is 2 clocks, the first data element will be valid at  $n + t_{CK} + t_{AC}$ .

### 5.3.2 EXTENDED MODE REGISTER

The Extended Mode Register controls output drive strength selection as shown in Figure 7.

The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA1=1 and BA0=0) and will retain the stored information until it is reprogrammed, the device loses power, or DAI is written to “1”.

The Extended Mode Register must be loaded when no bursts are in progress, and the controller must wait the specified time  $t_{MRD}$  before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

A logic 0 should be programmed to all the undefined or reserved address bits to ensure future compatibility.

At the beginning of Device Auto-Initialization, the memory shall set the Extended Mode Register to the default value 0x0080 (Half Drive Strength).

#### 5.3.2.1 OUTPUT DRIVE STRENGTH

The drive strength may be adjusted via address bits A5 and A6 and A7. Weak drive strengths are intended for lighter loads or point-to-point environments. Strong drive strengths are available, intended for the higher loads of a bus shared by both SDRAM and NVM. The I-V curves for Full Drive Strength and Half Drive Strength are included in this document (cf. Table 19, Figure 51 and Figure 52).

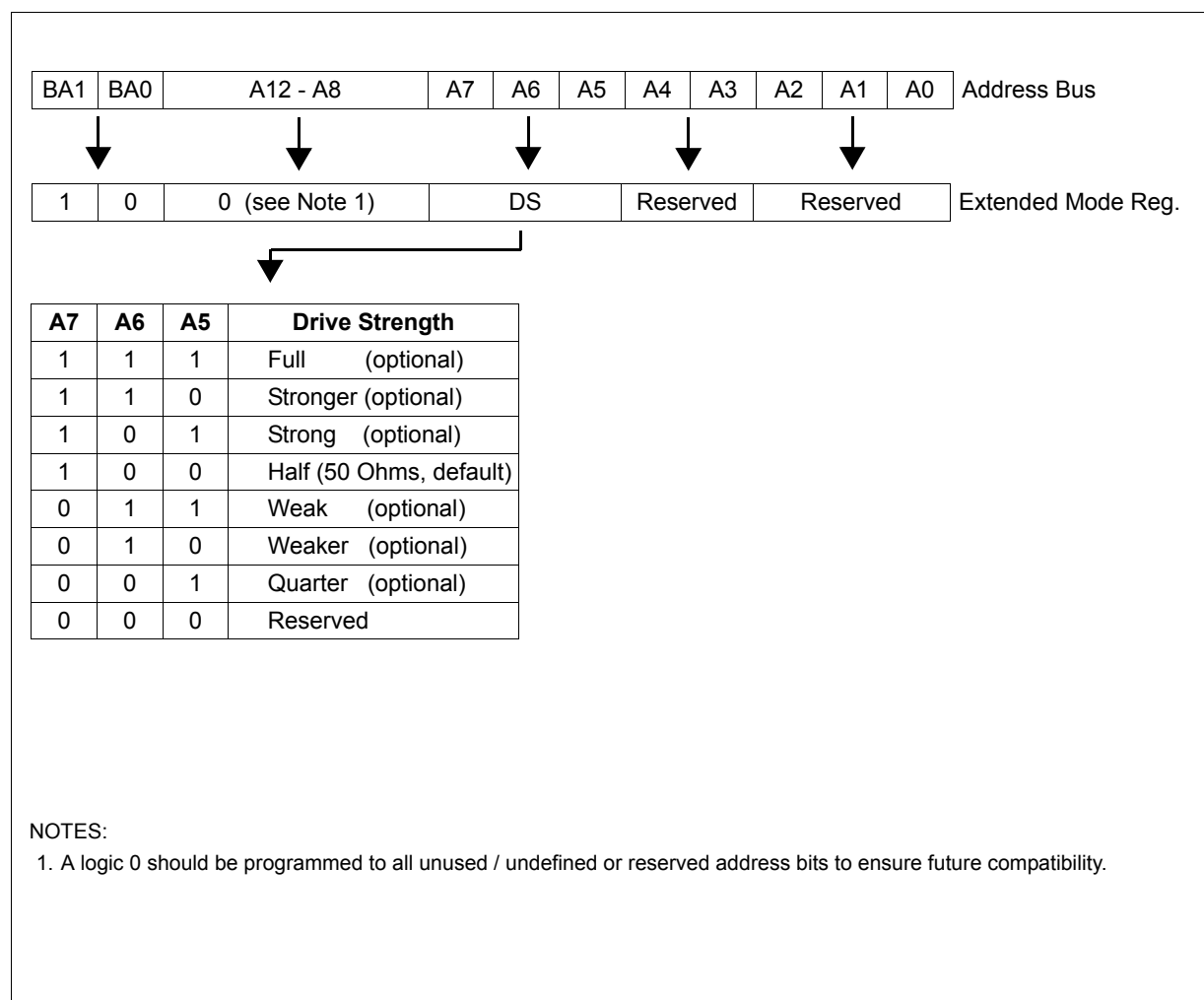


Figure 7: Extended Mode Register Definition

### 5.3.3 MODE REGISTER 11

The Mode Register 11 includes three controls for LPDDR Non-Volatile Memories: Overlay Window Base Address (OWBA), Overlay Window Enable (OWE) field, and Device Auto-Initialization (DAI) field, as shown in Figure 8.

The Mode Register 11 is programmed via the MODE REGISTER SET command (with BA1=1 and BA0=1) and will retain stored information (except the DAI field) until this mode register is reprogrammed, the device loses power, or DAI is written to “1”.

(When DAI is written to “1”, the memory shall set the Mode Register 11 to the default value with zeros in all fields except the DAI field.

After DAI has been written to “1”, the memory shall reset the DAI field to “0” when the internal Device Auto-Initialization process is finished.)

In general, the Mode Register 11 shall be loaded only when each Row-Data-Buffer is in either Idle or Row-Active state (so that no bursts are in progress), however, an exception is allowed to start Device Auto-Initialization (during system warm-reset). The controller must wait the specified time  $t_{MRD}$  before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

A logic 0 should be programmed to all the undefined and reserved address bits to ensure future compatibility. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

Address bits A8-A9 select 1 of 4 sub-registers, which include fields described below.

#### 5.3.3.1 OVERLAY WINDOW BASE ADDRESS

Sub-registers 11, 10, and 01 hold some logical address bits of the Overlay Window Base Address (OWBA). System software may adjust OWBA[35:13], but OWBA[12:0] are assumed all zeros, because the Overlay Window may be positioned only at 8-KByte alignment granularity in the address map. Notice that this logical address defines OWBA[0] to be a byte-select address bit. Software might need to convert a word-address to a byte-address before masking and shifting individual bytes of OWBA to write into Mode Register 11.

#### 5.3.3.2 OVERLAY WINDOW ENABLE

Sub-register 00 bit 6 holds the Overlay Window Enable (OWE) field. Set OWE = 1 to enable the Overlay Window. Reset OWE = 0 to disable the Overlay Window.

#### 5.3.3.3 FLUSH

Sub-Register 00, Bit 5 optionally may contain the Flush Bit (FL) to flush the Row Data Buffers (RDBs). Valid data in the RDBs will be written to the offset location within the overlay window when the Flush Bit is written with “1”. The FL Bit is a write-only bit.

When implemented, the Flush Bit is used to help maintain coherency within the Flash Device. The Flush Bit may be used to ensure that data written to the RDBs is committed to the internal registers or to the program buffer.

#### 5.3.3.4 DEVICE AUTO-INITIALIZATION

Sub-register 00 bit 7 holds the Device Auto-Initialization (DAI) field.

During system cold-boot, the memory controller shall set DAI = 1 as shown in the Power-up Initialization Sequence to reset the memory. Similarly, during system warm-reset, the memory controller shall set DAI=1.

When the controller sets DAI = 1, the NVM shall start an internal Device Auto-Initialization process, which keeps DAI = 1 during its variable latency. Immediately after the controller sets DAI = 1, the NVM immediately shall set the Mode Register to the default value, and shall set the Extended Mode Register to the default value, and shall set the Mode Register 11 to the default value with zeros in all fields except the DAI field. This overwrites any mode register values which may have been loaded previously.

Therefore, the memory controller shall use the SRR (register read) method to poll the status of the DAI field (in SRR read-only register 18) until Device Auto-Initialization is finished (until DAI = 0).

The memory shall keep DAI = 1 (“busy”) for the duration of the Device Auto-Initialization process, and shall reset DAI to 0 (“finished”) when the Device Auto-Initialization process is finished.

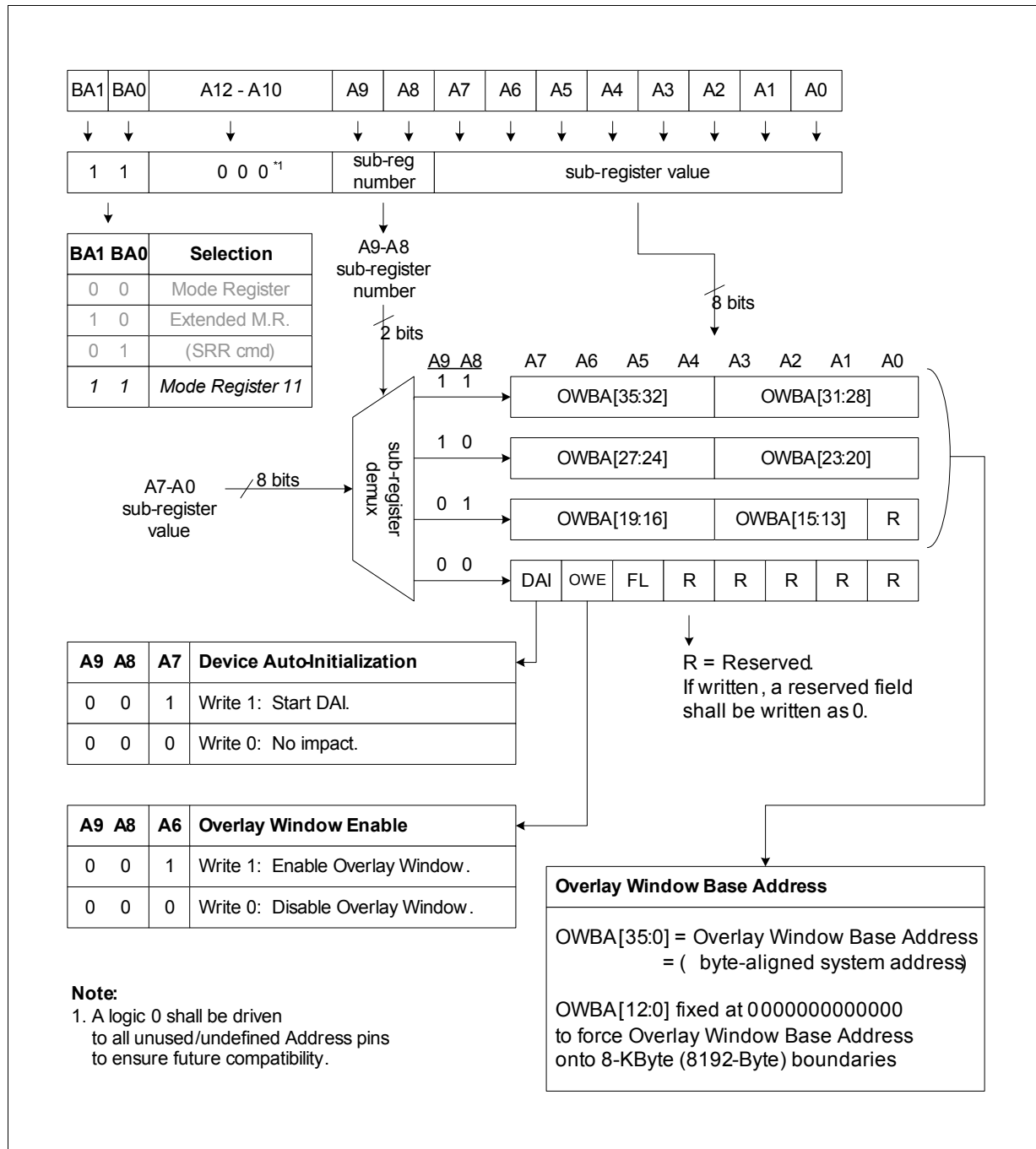


Figure 8: Mode Register 11 Definition

### 5.3.4 SRR READ-ONLY REGISTERS

A memory-controller may read several read-only registers using the SRR Command Sequence, which comprises a special MRS command followed by a special READ command. Software authors should consult their memory-controller documentation in order to invoke a read-only SRR command sequence.

LPDDR Non-Volatile Memories shall support the SRR read-only registers defined in this section, and shall support the SRR command sequence defined in the Operations section on page 34.

An address map of the SRR read-only registers is shown in Table 3, and each SRR read-only register is defined in detail on the following pages.

(Meanwhile, different memory-mapped read/write registers are available in the Overlay Window while the Overlay Window is enabled. Software may access those other memory-mapped registers using regular software instructions to read and write uncached unbuffered external memory. See Mode Register 11 definition in Figure 8 on page 19. Also see \*\*\* TBD future documentation on Overlay Window and memory-mapped register map \*\*\*)

**Table 3 SRR Read-Only Registers Address Map**

| with MRS cmd |                       | with READ cmd |                       | SRR Read-Only Register |                                          | Notes |
|--------------|-----------------------|---------------|-----------------------|------------------------|------------------------------------------|-------|
| BA1 BA0      | An-A0                 | BA1 BA0       | An-A0                 | #                      | Description                              |       |
| 0 1          | 0x0000                | 0 1           | 0x0000                | 0                      | LPDDR-NVM Signature                      |       |
| 0 1          | 0x0001 through 0x000F | 0 1           | 0x0001 through 0x000F | 1 .. 15                | reserved                                 |       |
| 0 1          | 0x0010                | 0 1           | 0x0010                | 16                     | reserved                                 |       |
| 0 1          | 0x0011                | 0 1           | 0x0011                | 17                     | Basic Characteristics                    |       |
| 0 1          | 0x0012                | 0 1           | 0x0012                | 18                     | Mode Register 11 sub-registers 01 and 00 |       |
| 0 1          | 0x0013                | 0 1           | 0x0013                | 19                     | Mode Register 11 sub-registers 11 and 10 |       |
| 0 1          | 0x0014 through 0x001F | 0 1           | 0x0014 through 0x001F | 20 .. 31               | reserved                                 |       |

5.3.4.1 SRR REGISTER 0 (Address 0000h)

A memory controller may read this register to determine the LPDDR memory is a Non-Volatile Memory (and is not an SDRAM memory).

When reading the SRR Register 0, the LPDDR Non-Volatile Memory shall drive DQ3-DQ0 with the binary value 1010 (which is a signature value for LPDDR-NVM).

Figure 9 defines SRR Register 0.

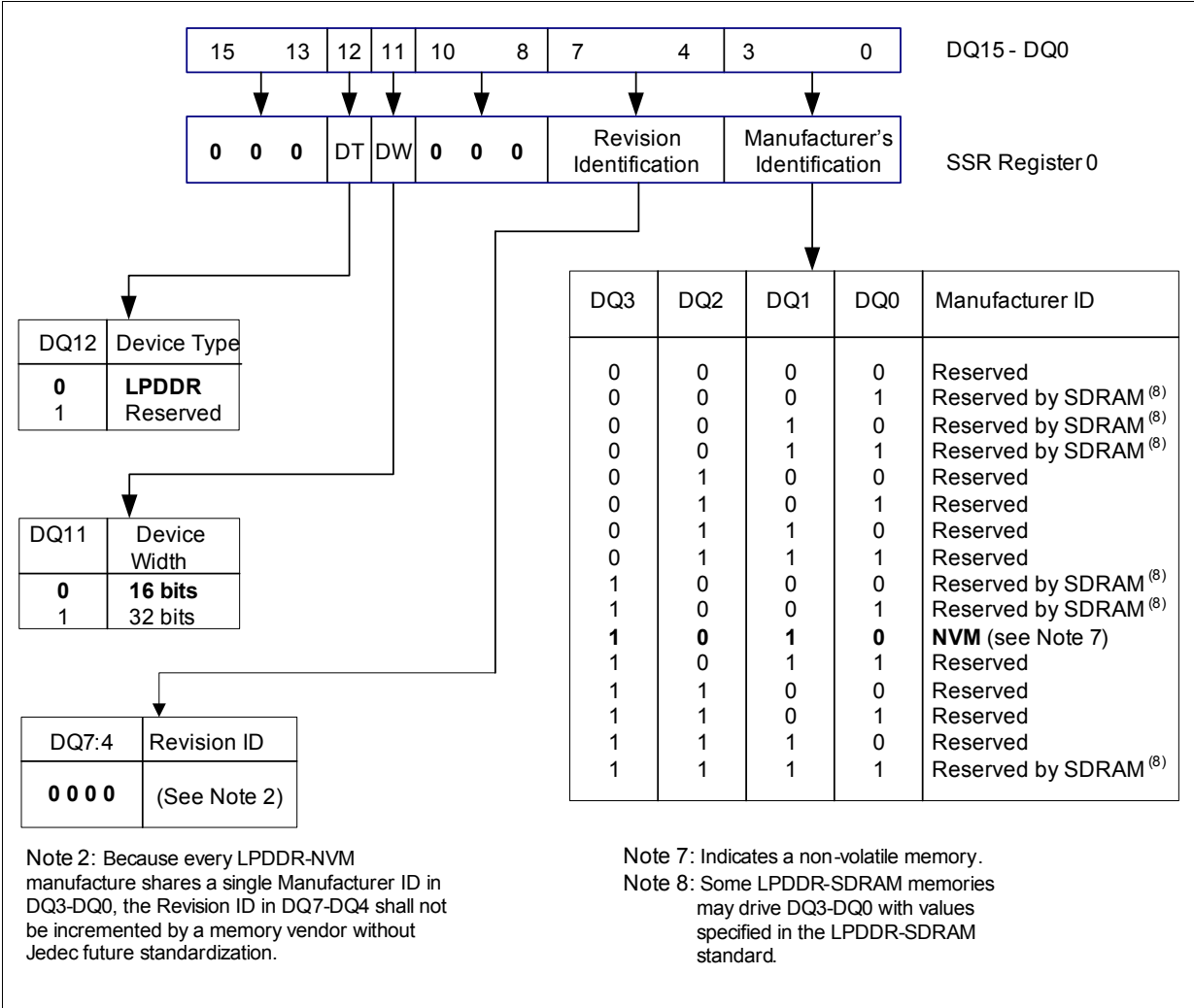


Figure 9: SRR Register 0

5.3.4.2 SRR REGISTER 17 (Address 0011h)

A memory controller may read this register to determine some basic characteristics of the LPDDR-NVM, which might be useful to optimize boot-mode execution time.

Figure 10 defines SRR Register 17.

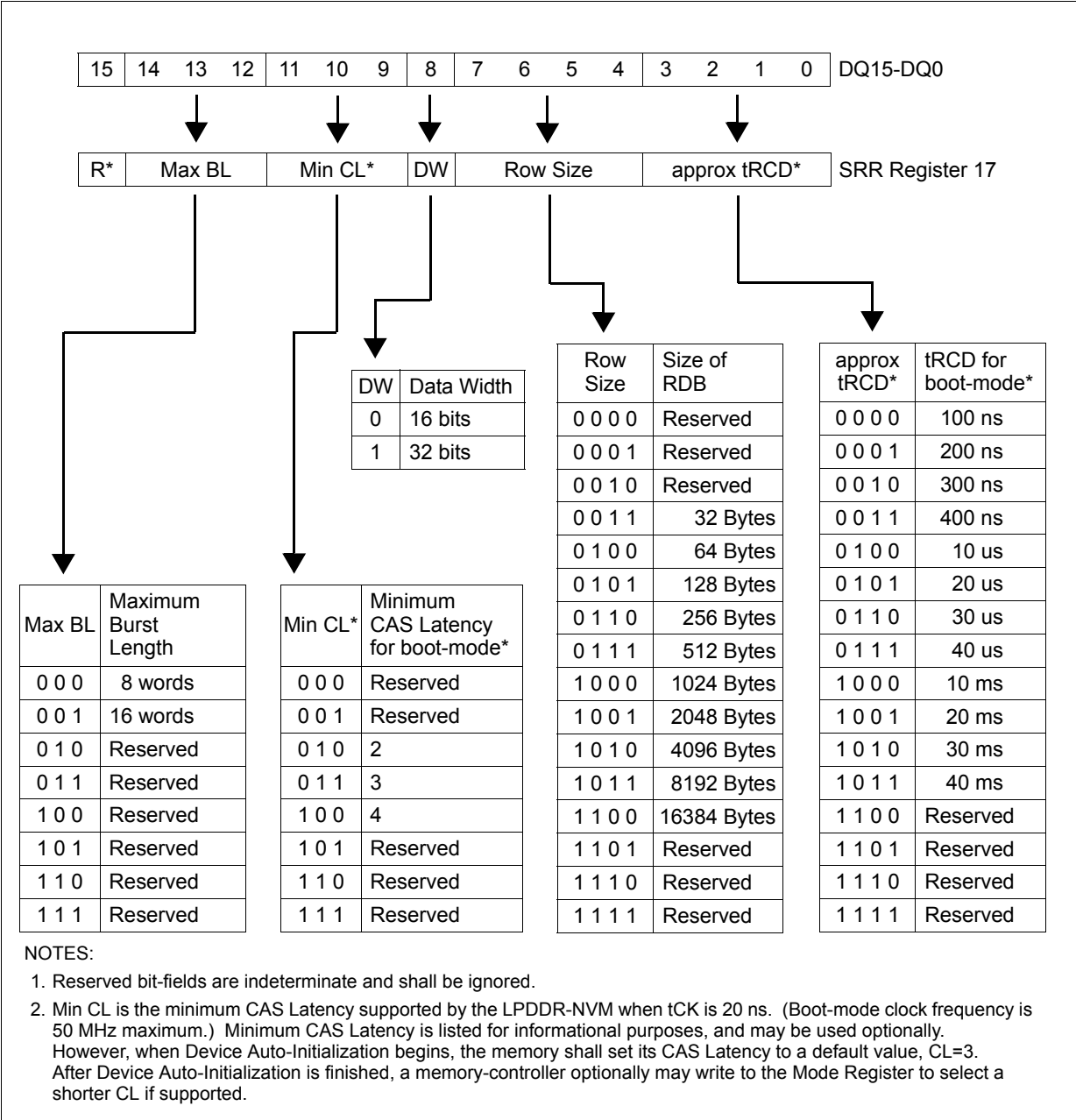


Figure 10: SRR Register 17

5.3.4.3 SRR REGISTERS 18 and 19 (Addresses 0012h-0013h)

The fields in Mode Register 11 may be read from SRR registers 18 and 19.

For example, during system cold-boot or during system warm-reset, the controller shall write “1” to the DAI field in Mode Register 11 to start the memory’s variable latency Device Auto-Initialization process. The controller then shall use the read-only SRR command sequence to poll the DAI status bit from DQ7 in SRR Register 18, waiting for the end of the memory’s Device Auto-Initialization process shown by DQ7=0 (Ready).

Figure 11 defines SRR Register 18. Figure 12 defines SRR Register 19.

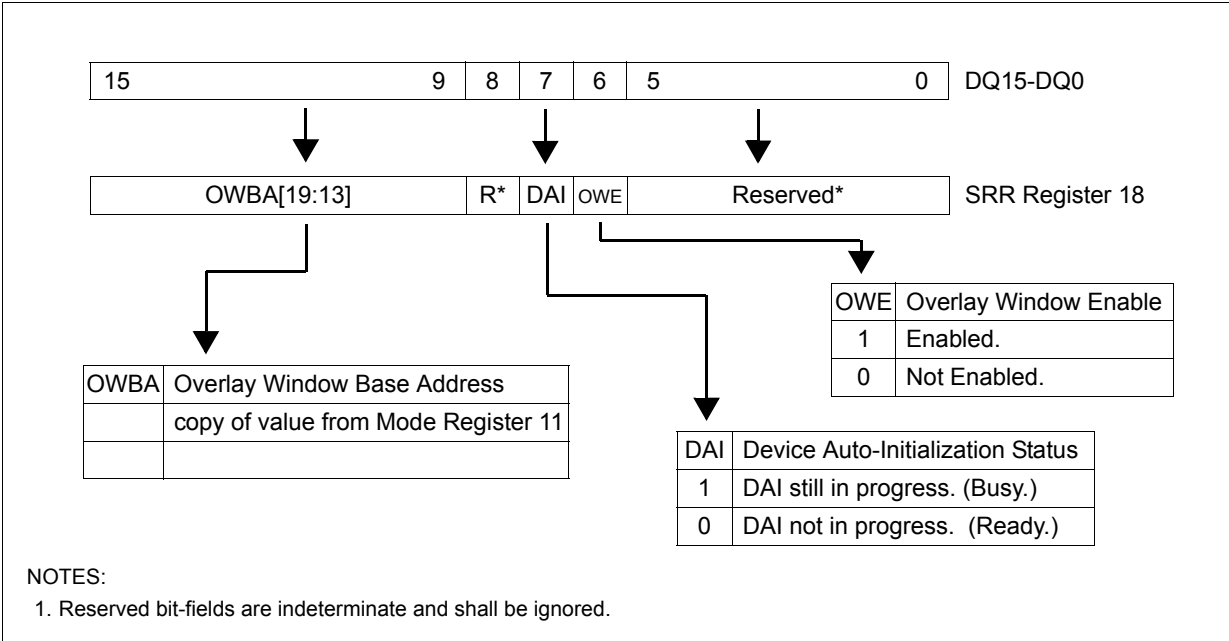


Figure 11: SRR Register 18

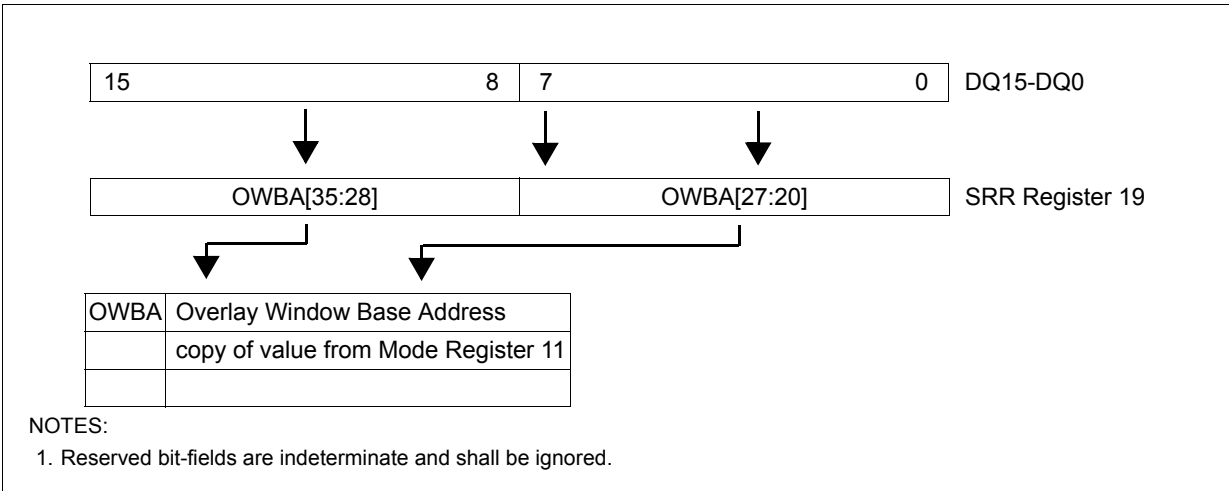


Figure 12: SRR Register 19

## 6 COMMANDS

All commands (address and control signals) are registered on the positive edge of clock (crossing of CK going high and CK going low). Figure 13 shows basic timing parameters for all commands.

Table 4, Table 5 and Table 6 provide a quick reference of available commands.

Table 7 and Table 8 provide the current state / next state information. This is followed by a verbal description of each command.

**Table 4 TRUTH TABLE - COMMANDS [Notes 1-6]**

| NAME (FUNCTION)                                        | $\overline{\text{CS}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | BA    | An - A0           | NOTES |
|--------------------------------------------------------|------------------------|-------------------------|-------------------------|------------------------|-------|-------------------|-------|
| DESELECT (NOP)                                         | H                      | X                       | X                       | X                      | X     | X                 | 2     |
| NO OPERATION (NOP)                                     | L                      | H                       | H                       | H                      | X     | X                 | 2     |
| ACTIVE (select RAB and RDB and activate row)           | L                      | L                       | H                       | H                      | Valid | Row <sub>A</sub>  |       |
| READ (select RDB and column and start read burst)      | L                      | H                       | L                       | H                      | Valid | Col               |       |
| WRITE (select RDB and column and start write burst)    | L                      | H                       | L                       | L                      | Valid | Col               |       |
| BURST TERMINATE                                        | L                      | H                       | H                       | L                      | X     | X                 | 3     |
| PREACTIVE (load partial row-address into selected RAB) | L                      | L                       | H                       | L                      | Valid | Row <sub>PA</sub> |       |
| Reserved (NOP)                                         | L                      | L                       | L                       | H                      | X     | X                 | 6     |
| MODE REGISTER SET                                      | L                      | L                       | L                       | L                      | Valid | Op-code           | 4     |

NOTES:

1. All states and sequences not shown are illegal or reserved.
2. Deselect and NOP are functionally interchangeable.
3. Burst Terminate applies to only Read bursts. This command is undefined and should not be used for Write bursts.
4. BA0 and BA1 value select among the three mode registers, or designate the beginning of the SRR command sequence.
5. CKE is HIGH for all commands shown. When CKE is LOW, see Table 6.
6. Allowed during LPDDR-NVM initialization sequence but not recommended afterward. LPDDR-NVM allows (but does not require) LPDDR-SDRAM initialization sequence before starting Device Auto-Initialization.

**Table 5 TRUTH TABLE - DM Operations**

| FUNCTION      | DM | DQ    | NOTES |
|---------------|----|-------|-------|
| Write Enable  | L  | Valid | 1     |
| Write Inhibit | H  | X     | 1     |

NOTES:

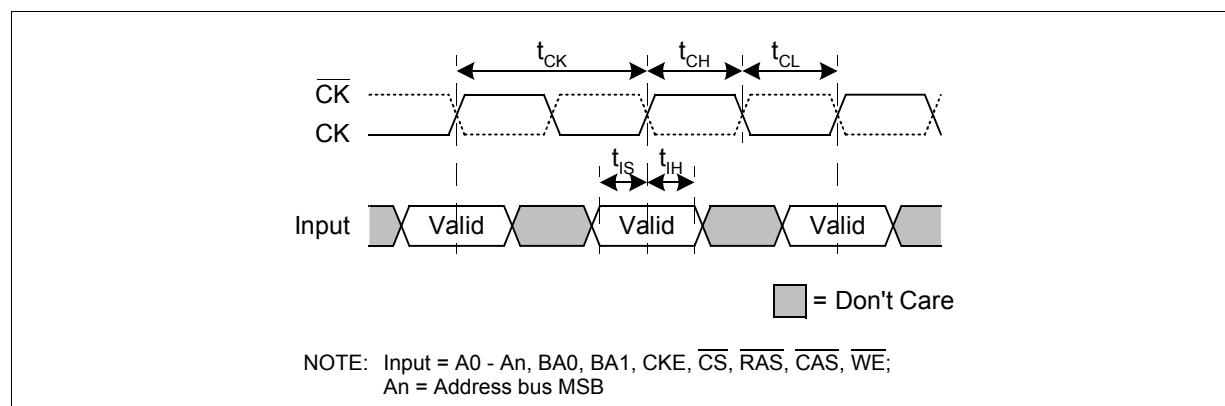
1. Used to mask write data, provided coincident with the corresponding data.

**Table 6 TRUTH TABLE - CKE [Notes 1 - 8]**

| CKE n-1 | CKE n | Current State              | COMMAND n       | ACTION n                | NOTES   |
|---------|-------|----------------------------|-----------------|-------------------------|---------|
| L       | L     | Power Down                 | X               | Maintain Power Down     | 8       |
| L       | H     | Power Down                 | NOP or DESELECT | Exit Power Down         | 5, 6, 7 |
| H       | L     | All RDBs Idle              | NOP or DESELECT | Idle Power Down Entry   | 5       |
| H       | L     | RDB(s) Active              | NOP or DESELECT | Active Power Down Entry | 5       |
| H       | H     | See the other Truth Tables |                 |                         |         |

## NOTES:

1. CKEn is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
2. Current state is the state of LPDDR-NVM immediately prior to clock edge n.
3. COMMANDn is the command registered at clock edge n, and ACTIONn is the result of COMMANDn.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT and NOP are functionally interchangeable.
6. Power Down exit time ( $t_{XP}$ ) should elapse before a command other than NOP or DESELECT is issued.
7. The clock must toggle at least once during the  $t_{XP}$  period.
8. Clock frequency may be reduced, and/or the clock may be stopped, during 'Idle Power-down' or 'Active Power-down' states.

**Figure 13: Basic Timing Parameters for Commands****Table 7 TRUTH TABLE - CURRENT STATE BAn - COMMAND TO BAn [Notes 1 - 11]**

| CURRENT STATE of BAn | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | COMMAND (ACTION) for BAn (same BA value)         | NOTES |
|----------------------|-----------------|------------------|------------------|-----------------|--------------------------------------------------|-------|
| Any                  | H               | X                | X                | X               | DESELECT (NOP / continue previous operation)     |       |
|                      | L               | H                | H                | H               | No Operation (NOP / continue previous operation) |       |