

Preliminary publication of JEDEC Semiconductor Memory Ballot

This Ballot was developed by JEDEC Committee JC-45 and approved by the JEDEC Board of Directors. It is published here in preliminary form, prior to being integrated into JEDEC Standard JESD21C and published in final form.

Title of Ballot: DDR3 DIMM Label

Council Ballot Number: JCB-09-045

Committee Ballot Number: 45.1-08-138a

Committee Item Number: 2099.01b

Date of Council Approval: August 2009

Background: This proposal was balloted as JC-45-08-138a on March 3, 2009 and expired on May 24, 2009. The voting results were reported at the June, 2009 JC-65 Committee meeting at which time the ballot was approved for Board of Directors submittal.

Since the DDR3 DIMM Label specification was approved, at least one new speed grades have been discussed. This proposal formalizes names and label standards for DDR3-1866 and DDR3-2133 devices. In addition, a letter is assigned for the LR-DIMM type.

JC-45 Item #2099.01: DDR3 DIMM Labels

Information in **RED** is the scope of this ballot.

DDR3 "End-User" DIMM Label Format:

The following label shall be applied to all DDR3 memory modules targeted at end-user type products to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A readable point size should be used, and the number can be printed in one or more rows on the label. Hyphens may be dropped when lines are split, or when font changes sufficiently separate fields. Unused letters in each field, such as ggggg, are to be omitted when not needed.

Voltage options in field 'v' describe the nominal voltage VDD of the SDRAMs and support components (excluding the SPD). Values for these voltages are 'operable' which means the device characteristics such as timing are supported at this voltage, or 'endurant' which means that the device may be powered to that voltage level without damage, however should not be used as operation is not guaranteed at the higher voltage.

ggggg eRxff PC3v-wwwwwm-aa-bb-ccd

Where:

ggggg = Module total capacity, in bytes
 256MB, 512MB, 1GB, 2GB, 4GB, etc.

eR = Number of ranks of memory installed
 1R = 1 rank of DDR3 SDRAM installed
 2R = 2 ranks
 4R = 4 ranks

xff = Device organization (bit width) of DDR3 SDRAMs used on this assembly
 x4 = x4 organization (4 DQ lines per SDRAM)
 x8 = x8 organization
 x16 = x16 organization

v = SDRAM and support component supply voltage (VDD)
 Blank = 1.5 V operable
 L = 1.35 V operable, 1.5 V operable
 U = 1.TBD V operable, 1.TBD V endurant

wwwww = Module bandwidth in MB/s
 6400 = 6.40 GB/s (DDR3-800 SDRAMs, 8 byte primary data bus)
 8500 = 8.53 GB/s (DDR3-1066 SDRAMs, 8 byte primary data bus)
 10600 = 10.66 GB/s (DDR3-1333 SDRAMs, 8 byte primary data bus)
 12800 = 12.80 GB/s (DDR3-1600 SDRAMs, 8 byte primary data bus)
14900 = 14.93 GB/s (DDR3-1866 SDRAMs, 8 byte primary data bus)
17000 = 17.06 GB/s (DDR3-2133 SDRAMs, 8 byte primary data bus)

m = Module Type
 E = Unbuffered DIMM ("UDIMM"), with ECC (x72 bit module data bus)
 F = Fully Buffered DIMM ("FB-DIMM")
L = Load Reduction DIMM ("LR-DIMM")
 M = Micro-DIMM
 N = Mini-RDIMM
 R = Registered DIMM ("RDIMM")
 S = Small Outline DIMM ("SO-DIMM")
 U = Unbuffered DIMM ("UDIMM"), no ECC (x64 bit module data bus)

aa = DDR3 SDRAM CAS Latency in clocks at maximum operating frequency
 bb = JEDEC SPD Revision Encoding and Additions level used on this DIMM
 cc = Reference design file used for this design (if applicable)