

Preliminary publication of JEDEC Semiconductor Memory Ballot

This Ballot was developed by JEDEC Committee JC-45 and approved by the JEDEC Board of Directors. It is published here in preliminary form, prior to being integrated into JEDEC Standard JESD21C and published in final form.

Title of Ballot: DDR3 Unbuffered Mini-DIMM Appendix-B

Council Ballot Number: JCB-11-034

Committee Ballot Number: 45.1-11-122

Committee Item Number: 2207.10

Date of Council Approval: May 2011

Background: This proposal was balloted as JC-45.1-11-122 on February 3, 2011 and expired on February 24, 2011. The voting results were reported at the March, 2011 JC-45 Committee meeting at which time the ballot was approved for Board of Directors submittal.

Appendix B - Raw Card B

DDR3 Mini-UDimm Design File

Applicable Design File	Applicable BOM
PC3-Mini-UDIMM_V050_RC_B0_20110103.brd	PC3-Mini-UDIMM_V050_RC_B0_20110201_BOM.pdf
Note: "Reference" design file updates will be released as needed. This Mini-UDIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated.	

Module Configuration

DIMM		SDRAM		# of SDRAMs	# of Physical Ranks	# of Address bits Row/Col/Bank	MO-244 variation
Capacity	Organization	Density	Organization				
1GB	128M x 72	512Mbit	64M x 8	18	2	13/10/3	AB
2GB	256M x 72	1Gbit	128M x 8	18	2	14/10/3	AB
4GB	512M x 72	2Gbit	256M x 8	18	2	15/10/3	AB
8GB	1G x 72	4Gbit	512M x 8	18	2	16/10/3	AB
16GB	2G x 72	8Gbit	1G x 8	18	2	16/11/3	AB

SDRAM Configuration

Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM	SDRAM Package Type	Package Type	MO-207 variation
9.0 mm x 12.5 mm	8	78 Ball FBGA	Planar	DT-z

Supported Speeds

Registration	Voltage	PC3-6400	PC3-8500	PC3-10600	PC3-12800	Notes
B0	DDR3	P	P	P		

Note: X will reflect passed committee ballot at the time when specification is issued at BOD ballot

Note: P means the proposed speed for committee ballot.

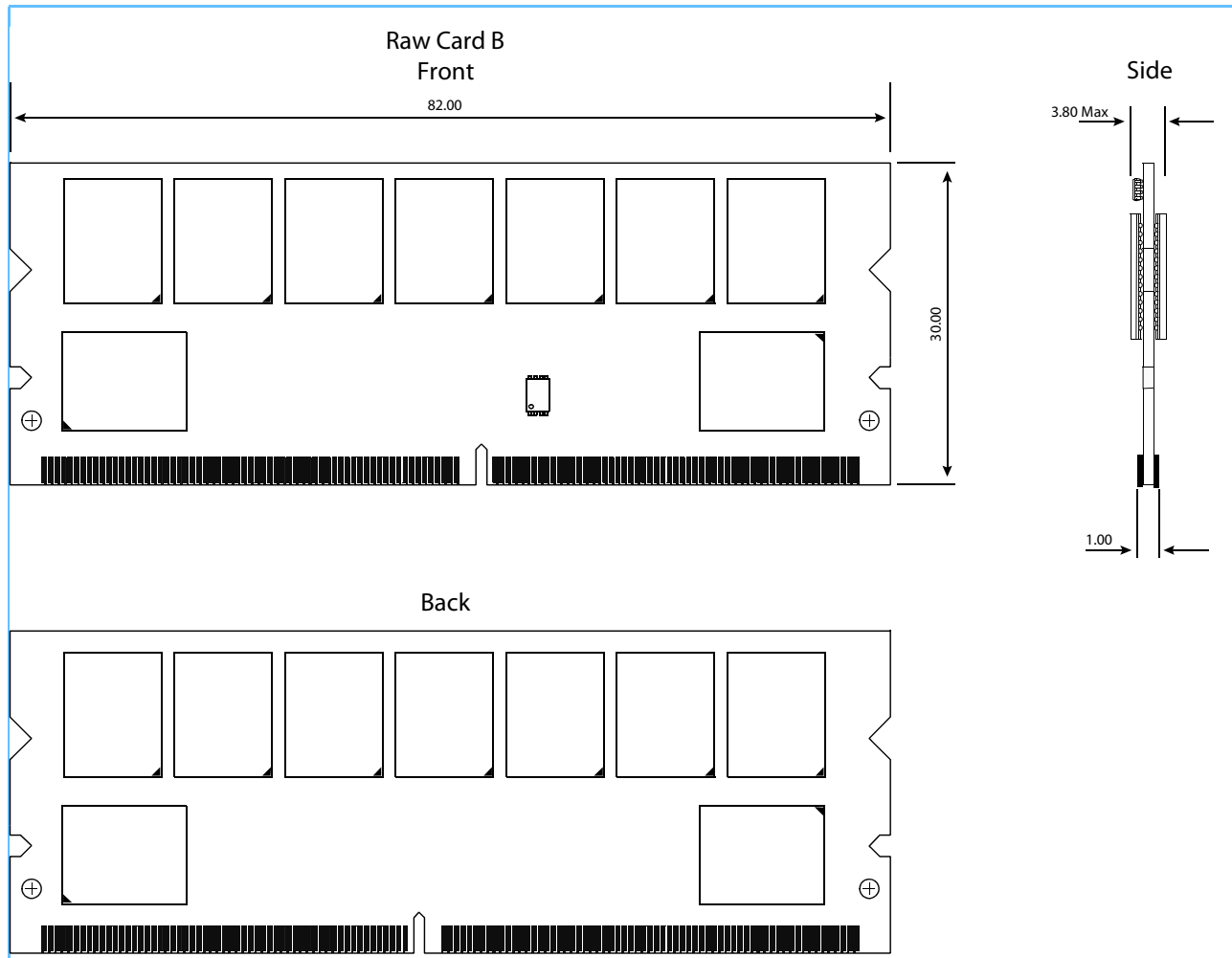
Design Rules and Deviations

None

Proposed

General Layout

x72 DIMM, populated as two physical ranks of x8 DDR3 SDRAMs

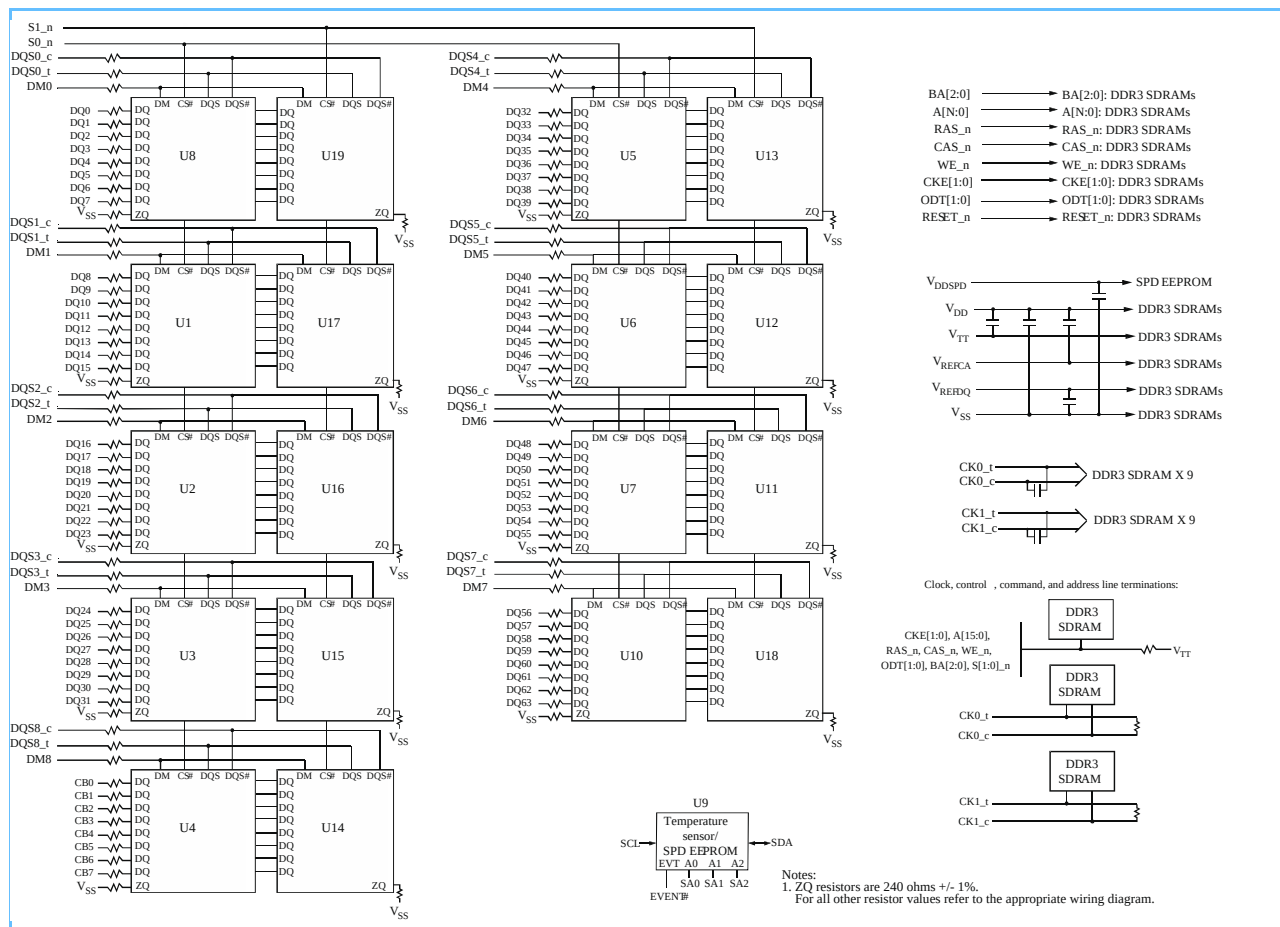


Note 1: All dimensions are typical unless otherwise stated. (Millimeters)

Proposed

Functional Block Diagram

x72 DIMM, populated as two physical ranks of x8 DDR3 SDRAMs



Proposed

Input Loading Matrix

Signal Names	Input Device	Loads
CK0_t, CK0_c, CK1_t, CK1_c	DDR3 SDRAM	9
RESET_n	DDR3 SDRAM	18
CKE0, ODT0, CKE1, ODT1	DDR3 SDRAM	9
Addr, BA, RAS_n, CAS_n, WE_n	DDR3 SDRAM	18
S0_n, S1_n	DDR3 SDRAM	9
DQ, CB, DQS_t, DQS_c	DDR3 SDRAM	2
DM, TDQS_t, TDQS_c	DDR3 SDRAM	2
SCL, SDA, SA	EEPROM	1
EVENT_n	Thermal sensor	1*
*Integrated thermal sensor optional.		

Proposed