

Preliminary publication of JEDEC Semiconductor Memory Ballot

This Ballot was developed by JEDEC Committee JC-45 and approved by the JEDEC Board of Directors. It is published here in preliminary form, prior to being integrated into JEDEC Standard JESD21C and published in final form.

Title of Ballot: DDR3 Mini-UDIMM RC F0(x8 2R, Stacked) specification

Council Ballot Number: JCB-11-102

Committee Ballot Number: 45.3-11-523

Committee Item Number: 2229.01

Date of Council Approval: Feb 2012

Background: This proposal was balloted as JC-45.3-11-523 on November 9, 2011 and expired on November 30, 2011. The voting results were reported at the December, 2011 JC-45 Committee meeting at which time the ballot was approved for Board of Directors submittal.

Annex F - Raw Card F

DDR3 mini-UDIMM Design File

Applicable Design File	Applicable BOM
PC3-Mini-UDIMM-V080_RC_F0_20111101	PC3-Mini-UDIMM-V080_RC_F0_20111101-BOM
Note: "Reference" design file updates will be released as needed. This UDIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated.	

Module Configuration

DIMM		SDRAM		# of SDRAMs	# of Physical Ranks	# of Address bits row/col/Bank	MO-244 variation
Capacity	Organization	Density	Organization				
1GB	128Mx72	512Mbit	64M x 8	18	2	13/10/3	DB
2GB	256Mx72	1Gbit	128M x 8	18	2	14/10/3	DB
4GB	512Mx72	2Gbit	256M x 8	18	2	15/10/3	DB
8GB	1Gx72	4Gbit	512M x 8	18	2	16/10/3	DB

SDRAM Configuration

Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM	SDRAM Package Type	Package Type	MO-207 variation
10.7 x 11.0	8	78 Ball FBGA ²	DDP ¹	DT-z

Note 1: DDP is a stacked die package.

Note 2: This is an 82 ball version of MO-207, variation DW-z that adds only 4 mechanical support balls.

Supported Speeds

Speed	PC3-6400	PC3-8500	PC3-10600	PC3-12800	PC3-14900	PC3-17000	Notes
DDR3	P	P	P	P			1, 2
DDR3L	P	P	P				1, 2

Note 1: X reflects speed grades approved from previous ballots.

Note 2: P denotes speed grades being proposed for this most recent ballot

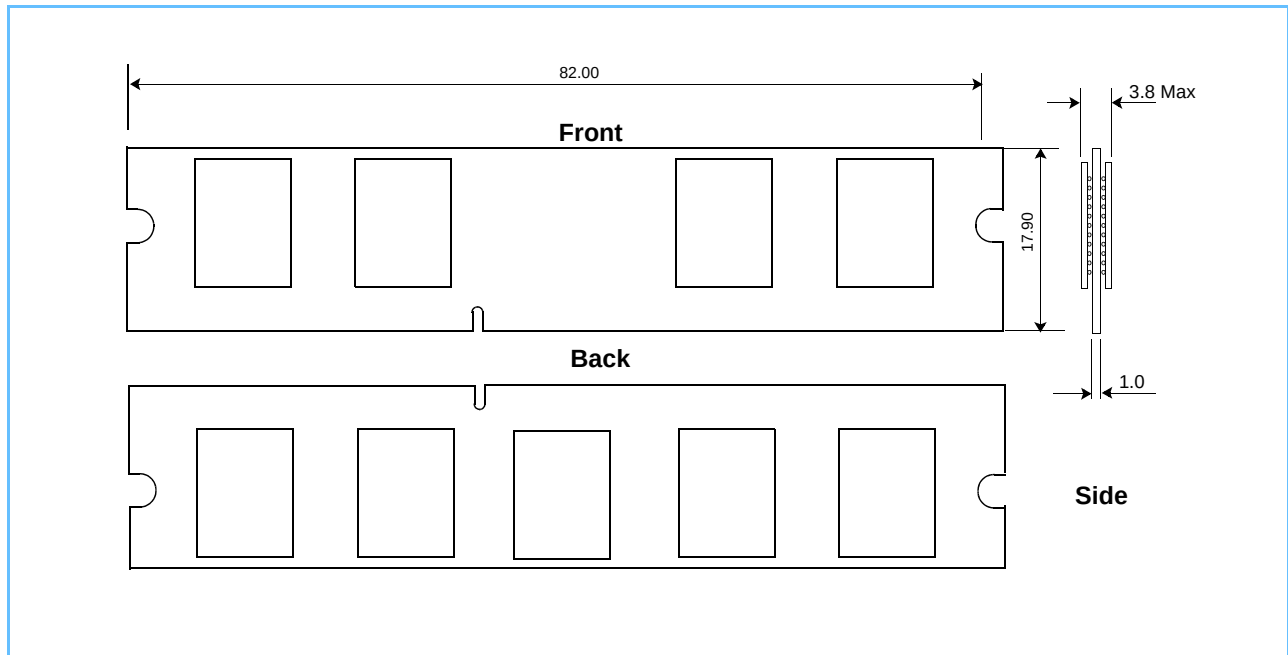
Design Rules and Deviations

1) This design uses 0.2 mm vias.

Proposed

General Layout

x72 DIMM, populated as two physical ranks of stacked x8 DDR3 SDRAMs

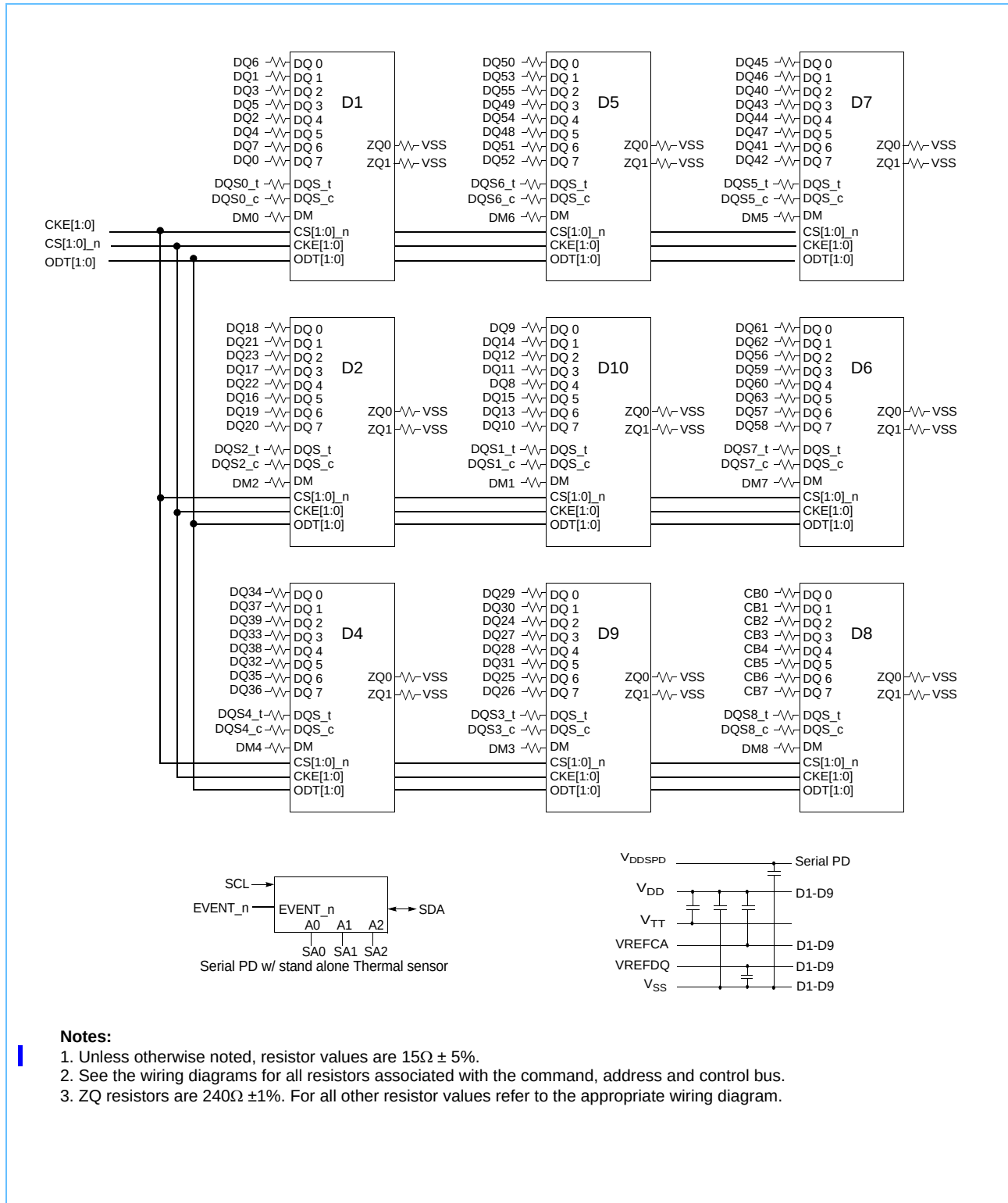


Note 1: All dimension are typical unless otherwise stated. (Millimeters)

Proposed

Functional Block Diagram

x72 DIMM, populated as two physical ranks of stacked x8 DDR3 SDRAMs



Proposed