

Preliminary publication of JEDEC Semiconductor Memory Ballot

This Ballot was developed by JEDEC Committee JC-45 and approved by the JEDEC Board of Directors. It is published here in preliminary form, prior to being integrated into JEDEC Standard JESD21C and published in final form.

Title of Ballot: DDR3 Mini-RDIMM Appendix D (x8 2R, Planar)

Council Ballot Number: JCB-12-063

Committee Ballot Number: 45.1-12-284

Committee Item Number: 2207.14

Date of Council Approval: Nov 2012

Background: This proposal was balloted as JC-45.1-12-284 on August 14, 2012 and expired on September 5, 2012. The voting results were reported at the September, 2012 JC-45 Committee meeting at which time the ballot was approved for Board of Directors submittal.

Annex D - Raw Card D

DDR3 Mini-RDimm Design File

Applicable Design File	Applicable BOM
PC3-Mini-RDIMM_V100_RC_D0_20120127.brd	PC3-Mini-RDIMM_V100_RC_D0_20120127_BOM.pdf
Note: "Reference" design file updates will be released as needed. This mini-RDIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated.	

Module Configuration

DIMM		SDRAM		# of SDRAMs	# of Physical Ranks	# of Address bits Row/Col/Bank	MO-244 variation
Capacity	Organization	Density	Organization				
1GB	128M x 72	512Mbit	64M x 8	18	2	13/10/3	AB
2GB	256M x 72	1Gbit	128M x 8	18	2	14/10/3	AB
4GB	512M x 72	2Gbit	256M x 8	18	2	15/10/3	AB
8GB	1G x 72	4Gbit	512M x 8	18	2	16/10/3	AB
16GB	2G x 72	8Gbit	1G x 8	18	2	16/11/3	AB

SDRAM Configuration

Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM	SDRAM Package Type	Package Type	MO-207 variation
9.0 mm x 12.5 mm	8	78 Ball FBGA	Planar	DT-z

Supported Speeds

	PC3-6400	PC3-8500	PC3-10600	PC3-12800	Notes
DDR3	P	P	P	P	1, 2
DDR3L	P	P	P	P	1, 2

Note1: X reflects speed grades that have passed the BOD.

Note 2: P reflects proposed speed grades for this ballot. JEDEC office to replace P with X prior to publication.

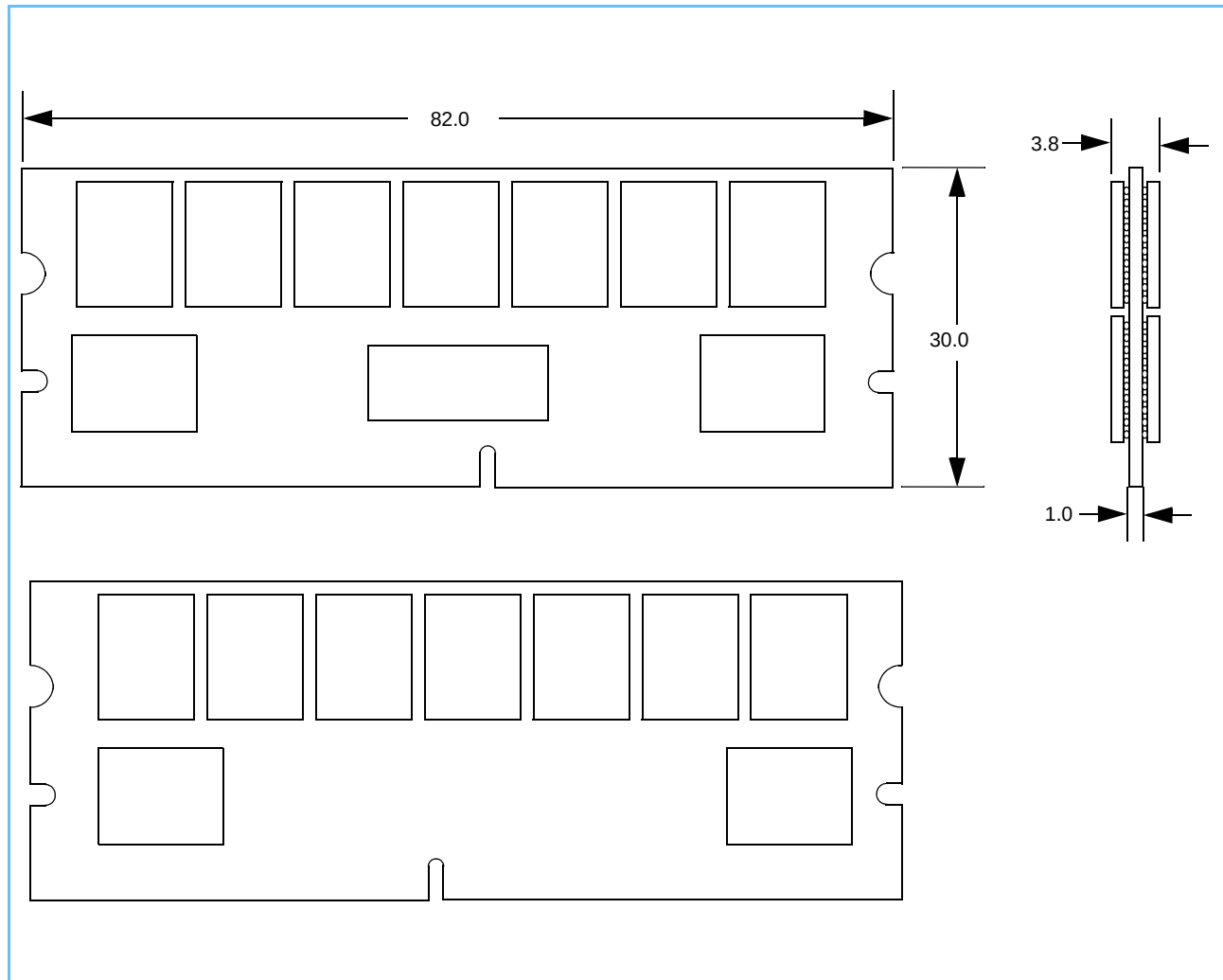
Design Rules and Deviations

None

Proposed

General Layout

x72 DIMM, populated as two physical ranks of x8 DDR3 SDRAMs

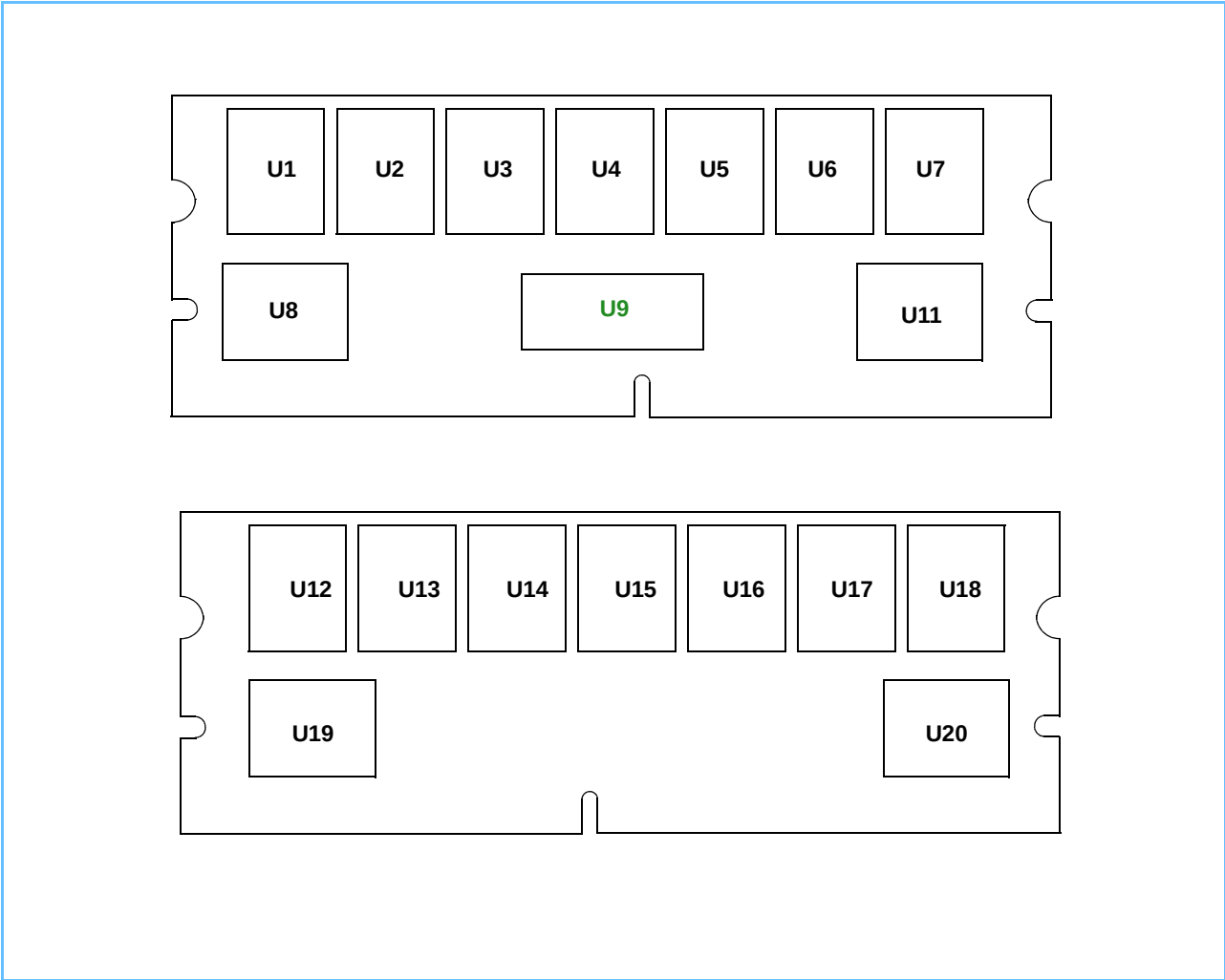


Note 1: All dimensions are typical unless otherwise stated. (Millimeters)

Proposed

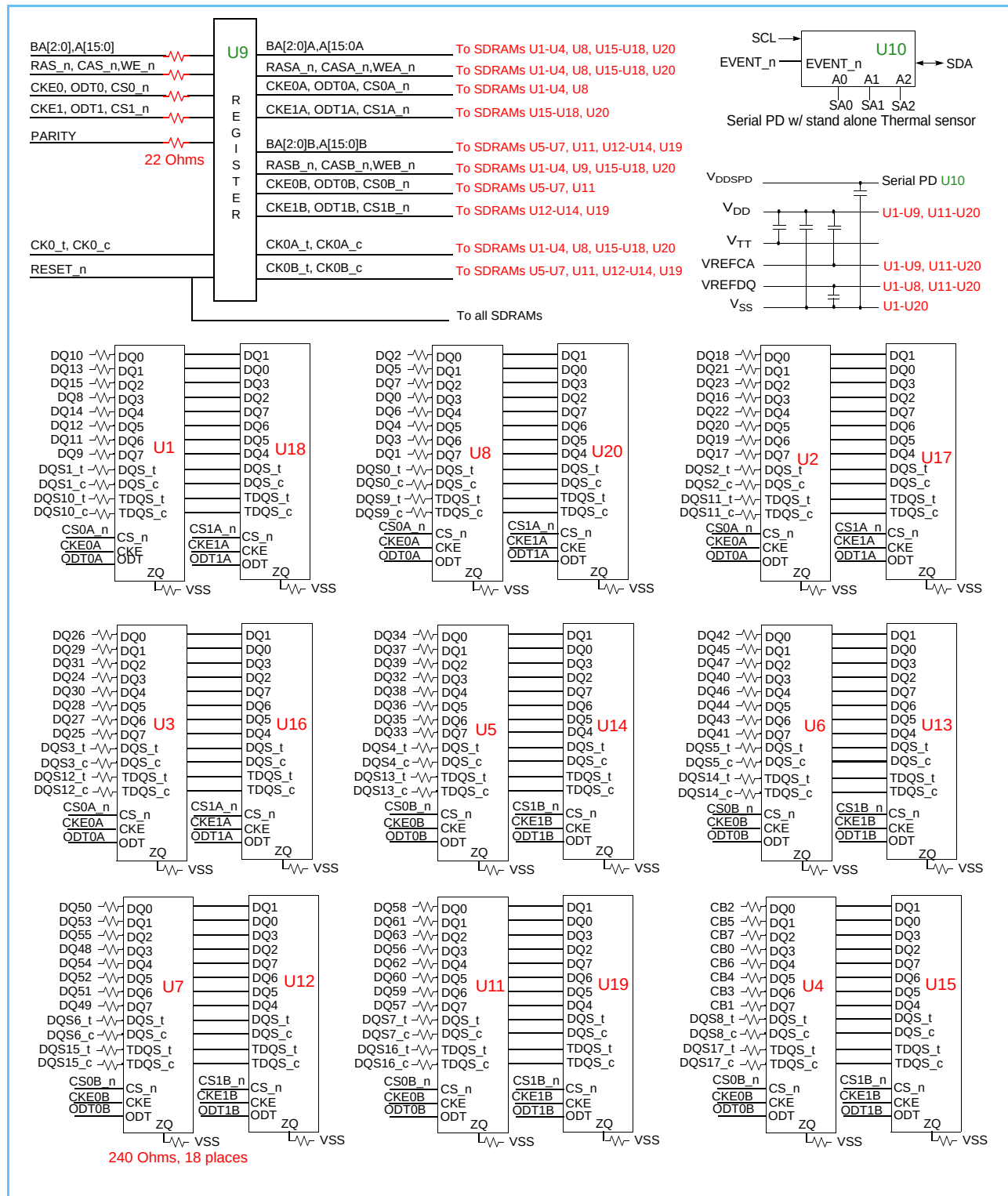
Functional Block Diagram

x72 DIMM, populated as two physical ranks of x8 DDR3 SDRAMs (Part 1 of 2)



Proposed

x72 DIMM, populated as two physical ranks of x8 DDR3 SDRAMs (part 2 of 2)



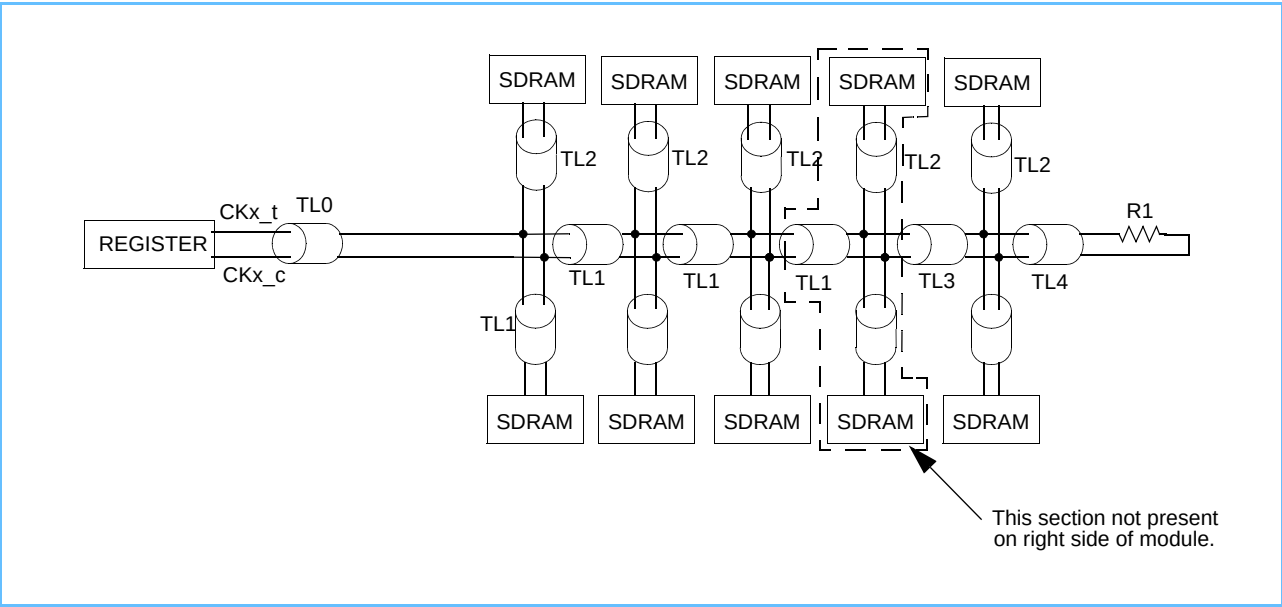
Input Loading Matrix

Signal Names	Input Device	Loads
CK0_t, CK0_c, CK1_t, CK1_c	DDR3 SDRAM	1
RESET_n	DDR3 SDRAM	19
CKE0, ODT0, CKE1, ODT1	DDR3 SDRAM	1
Addr, BA, RAS_n, CAS_n, WE_n	DDR3 SDRAM	1
S0_n, S1_n	DDR3 SDRAM	1
DQ, CB, DQS_t, DQS_c	DDR3 SDRAM	2
DM, TDQS_t, TDQS_c	DDR3 SDRAM	2
SCL, SDA, SA2, SA1, SA0	EEPROM	1
EVENT_n	Thermal sensor	1*
*Integrated thermal sensor optional.		

Proposed

Clock Net Structures

Net Structure Routing for CK0_t, CK0_c, CK1_t, CK1_c



Trace Lengths for Clock Routing to SDRAM Load Net Structures

Type	TL0 (mm)	TL1 (mm)		TL2 (mm)	TL3 (mm)	TL4 (mm)	R1 (Ohms) ±5%
		Min	Max				
Left Side	31.4	15.4	15.4	2.6	26.4	5.6	75
Right Side	42.4	17.4	17.5	2.6	31.5	5.8	75

1. All dimensions without a range specified to have a tolerance of 0.8mm

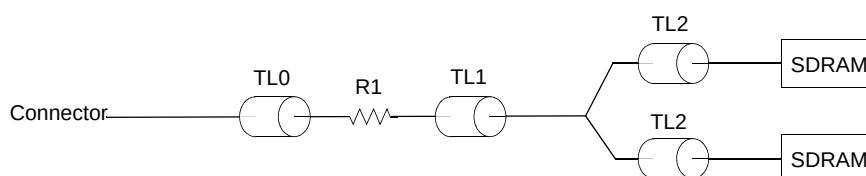
Proposed

Data Net Structures

DQ[63:0], CB[7:0], DQS[17:0]_t, DQS[17:0]_c

Special attention has been paid to balancing data nets (including Check Bits) within a DDR SDRAM, within a particular DIMM, and across the DIMM family. Data nets have been placed in order to bound the data strobe nets. Because data travels with the data strobe, the placement of the strobe in the middle of the narrow window aids in data timing. Although it is not necessary to ensure consistent delays between SDRAMs and/or card types, doing so facilitates system design, system simulation, and DIMM specifications. Recommended delays for all nets, as described in the following tables.

Net Structure Routing for DQ[63:0], CB[7:0], DQS[17:0]_t, DQS [17:0]_c



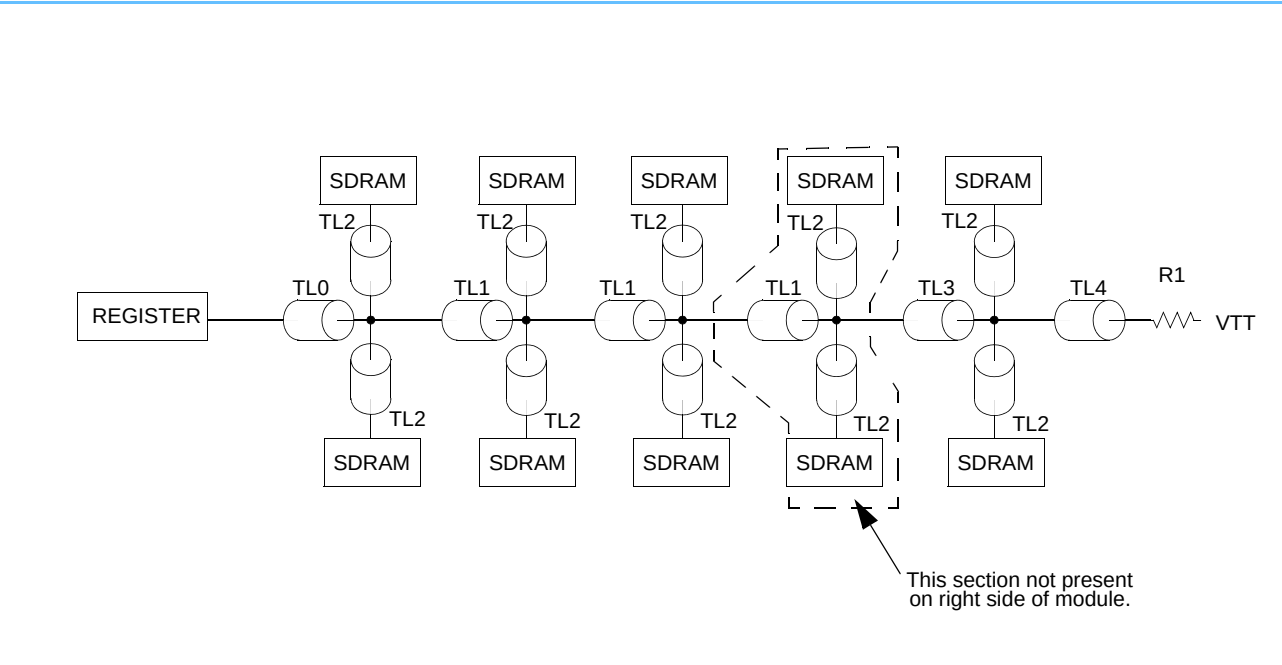
Trace Lengths for DQ[63:0], CB[7:0], DQS[17:0]_t, DQS[17:0]_c

DQ Bus	TL0 (mm)		TL1 (mm)		TL2 (mm)		TL0 + TL1 + TL2 (mm)		R1 (ohms) ±5%
	Min	Max	Min	Max	Min	Max	Min	Max	
DQ0-7, DQS0_t, DQS0_c, DQS9_t, DQS9_c,	3.1	3.5	8.4	11.4	0.8	1.7	15.9	16.2	15
DQ8-15, DQS1_t, DQS1_c, DQS10_t, DQS10_c,	3.3	3.5	15.4	18.9	0.8	2.0	23.5	23.6	15
DQ16-23, DQS2_t, DQS2_c, DQS11_t, DQS11_c,	3.2	3.4	14.8	17.9	0.7	1.8	22.4	22.6	15
DQ24-31, DQS3_t, DQS3_c, DQS12_t, DQS12_c,	3.3	3.5	16.5	19.3	0.9	2.1	24.2	24.4	15
DQ32-39, DQS4_t, DQS4_c, DQS13_t, DQS13_c,	3.2	3.4	17.6	20.5	0.8	1.7	25.0	25.2	15
DQ40-47, DQS5_t, DQS5_c, DQS14_t, DQS14_c,	3.3	3.6	15.1	18.3	0.8	1.9	22.2	23.1	15
DQ48-55, DQS6_t, DQS6_c, DQS15_t, DQS15_c,	3.1	3.4	16.3	19.5	0.6	2.7	24.1	24.2	15
DQ56-63, DQS7_t, DQS7_c, DQS16_t, DQS16_c,	3.3	4.3	10.5	14.5	1.1	2.1	19.5	19.6	15
CB0-CB7, DQS8_t, DQS8_c, DQS0_t, DQS17_c,	3.1	3.4	26.5	28.8	0.6	2.6	32.3	32.6	15

Proposed

Address and Command Net Structures

A[15:0], BA[2:0], RAS_n, CAS_n, WE_n



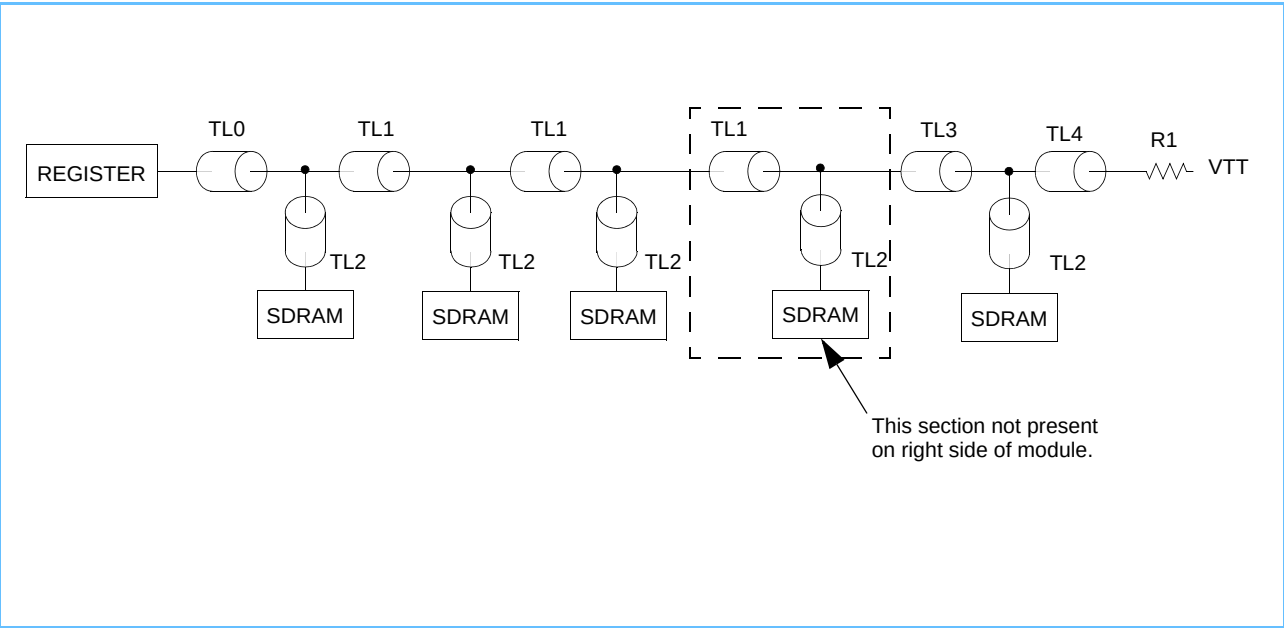
Trace Lengths for Address & Command Net Structures

Type	TL0 (mm)		TL1 (mm)		TL2 (mm)		TL0+TL2 (mm)		TL3 (mm)		TL4 (mm)		R1 (ohms) 5%
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Left Side	25.9	28.2	11.9	14.0	1.8	4.1	29.8	30.1	27.0	27.1	5.0	15.0	33
Right Side	38.9	41.2	12.0	12.1	1.8	4.2	42.9	43.1	28.0	28.1	5.0	15.0	33

Proposed

Control Net Structures

CS[1:0]_n, CKE[1:0], ODT[1:0]



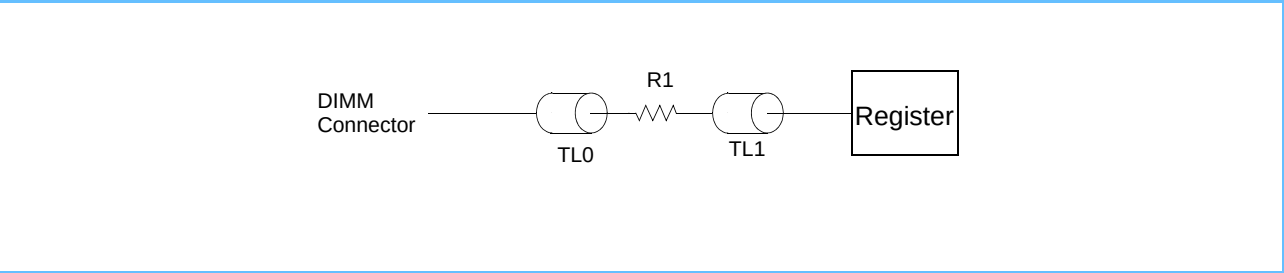
Trace Lengths for Control Net Structures

Type	TL0 (mm)		TL1 (mm)		TL2 (mm)		TL0+TL2 (mm)		TL3 (mm)		TL4 (mm)		R1 (ohms) ±5%
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Left side	34.3	34.5	18.4	18.6	0.5	0.6	34.0	35.0	29.9	30.1	10.0	16.0	33
Right Side	49.4	49.5	18.2	18.4	0.5	0.6	50.0	51.0	32.8	33.0	11.0	14.0	33

Proposed

Register Input Net Structures

A[15:0], BA[2:0], RAS_n, CAS_n, WE_n, ParIn, CS[1:0]_n, ODT[1:0]

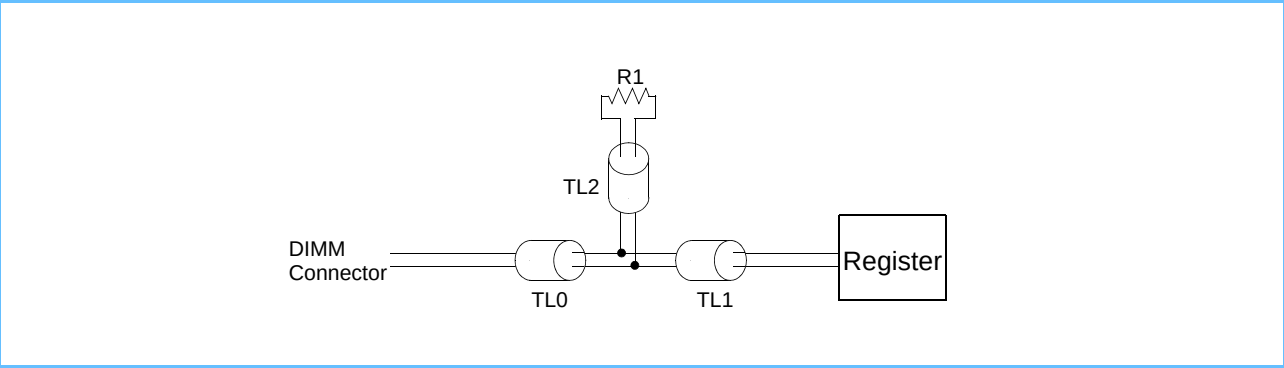


Trace Lengths for Register Input Net Structures

Type	TL0 (mm)		TL1 (mm)		TL0 + TL1 (mm)		R1 (ohms) 5%
	Min	Max	Min	Max	Min	Max	
Address, Command, Control	3.0	4.3	27.6	29.0	31.9	32.0	22

Proposed

Clock Input Structures
CK[0]



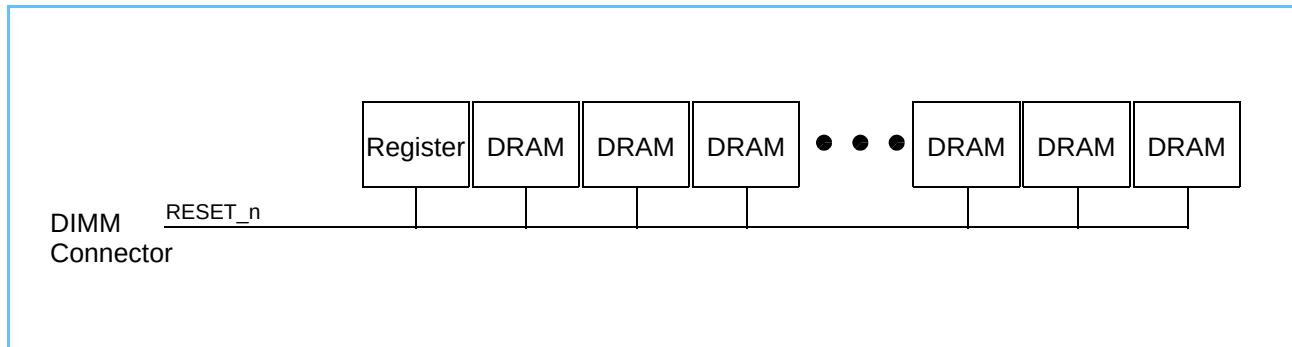
Trace Lengths for Clock Input Net Structures

Type	TL0 (mm)	TL1 (mm)	TL2 (mm)	TL0 + TL1 (mm)	R1 (Ohms) 5%
Clock	1.9	18.7	0.8	20.6	120

Proposed

RESET_n Structures

RESET_n

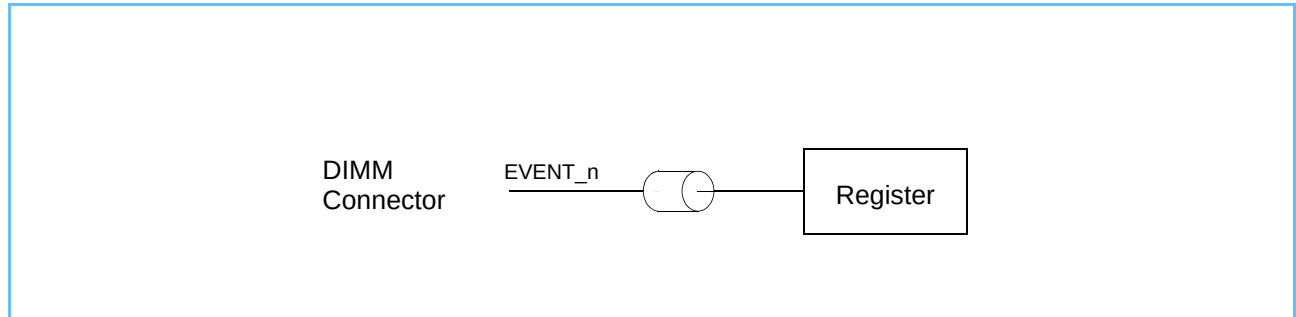


Total length of RESET_n net is 225 mm +/-10%

Proposed

EVENT_n Net Structures

EVENT_n



Total length of EVENT_n net is 21.5 mm +/-5 mm.

Proposed

Cross Section Recommendations

Most DIMM printed circuit board designs use eight layers of glass epoxy material. PCBs should contain solid ground plane and power plane layers as far as possible.

Note: The PCB edge connector contacts shall be gold-plated.

Example Eight Layer Stackup

	Solder Mask	0.015 mm	
L1	Copper	0.045 mm	Signal 0.5 oz. + Plating
	Prepreg	0.10 mm	
L2	Copper	0.015 mm	Vdd/Vss 0.5 oz.
	Core	0.10 mm	
L3	Copper	0.015 mm	Signal 0.5 oz.
	Prepreg	0.15 mm	
L4	Copper	0.015 mm	Vdd 0.5 oz.
	Core	0.1 mm	
L5	Copper	0.015 mm	Signal 0.5 oz.
	Prepreg	0.15 mm (*)	
L6	Copper	0.015 mm	Signal 0.5 oz.
	Core	0.10 mm	
L7	Copper	0.015 mm	Vdd/Vss 0.5 oz.
	Prepreg	0.10 mm	
L8	Copper	0.045 mm	Signal 0.5 oz. + Plating
	Solder Mask	0.015 mm	

Overall Thickness(without Mask) = 1.0mm +/- 0.1mm

(*)Note :

Even if you need to adjust the stackup, the distance between L5 and L6 should be kept >0.13 mm to reduce the crosstalk between L5 and L6 traces.

Proposed

8 layers Geometry/Impedance Table

Layer	Single Ended		Differential	
	Width	Target Z0	Width/Space	Target Zdiff
L1, L8	0.1 mm	60 ohms +/- 10%	0.1 / 0.1 mm	88 ohms +/- 15%
L3, L5, L6	0.08 mm	55 ohms +/- 10%	0.08 / 0.1 mm	88 ohms +/- 15%
L5 & L6	0.08 mm	55 ohms +/- 10%	0.1 / 0.1 mm	88 ohms +/- 15%
L8	0.1 mm	60 ohms +/- 10%	0.1 / 0.1 mm	88 ohms +/- 15%

1. All trace widths are subject to adjustment by PCB vendor, as required to align impedance targets.
2. Only the 55 Ohm and 60 Ohm single ended impedances are firm specification.
3. All other impedance targets are provided for reference only.