

Preliminary publication of JEDEC Semiconductor Memory Ballot

This Ballot was developed by JEDEC Committee JC-45 and approved by the JEDEC Board of Directors. It is published here in preliminary form, prior to being integrated into JEDEC Standard JESD21C and published in final form.

Title of Ballot: DDR4 UDIMM Design Specification Annex D

Council Ballot Number: JCB-14-002

Committee Ballot Number: 45.3-13-455

Committee Item Number: 2231.09

Date of Council Approval: Feb 2014

Background: This proposal was balloted as JC-45.3-13-455 on November 12, 2013 and expired on December 4, 2013. The voting results were reported at the December, 2014 JC-45 Committee meeting at which time the ballot was approved for Board of Directors submittal.

Annex D - Raw Card D

DDR4 Unbuffered DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
D0	PC4-UDIMM_V080_RC_D0_20131028.brd	PC4-UDIMM_V080_RC_D0_20131028_BOM.xlsx

Note: "Reference" design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.

Module Configuration

DIMM		SDRAM		# of SDRAM die Min/Max	# of Logical Ranks per DIMM Min/Max	# of Package Ranks per DIMM Min/Max	# of Address bits row/col	MO-309 variation
Maximum Capacity	Organization	Die Density	Organization					
2GB	256Mx72	2Gbit	256M x 8	9/9	1	1	14/10 ¹	AAxA
4GB	512Mx72	4Gbit	512G x 8	9/9	1	1	15/10 ¹	AAxA
8GB	1Gx72	8Gbit	1G x 8	9/9	1	1	16/10	AAxA
16GB	2Gx72	16Gbit	2G x 8	9/9	1	1	17/10	AAxA

1. Address A16 is the highest address bit used based on it being multiplexed with RAS_n

SDRAM Configuration

Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM BA/BG	SDRAM Package Type	Package Type	MO-207 variation
11.0 x 13.0	2/2	78 Ball FBGA	SDP	DW-z

Note: SDP is a Single Die per Package.

Supported Speeds

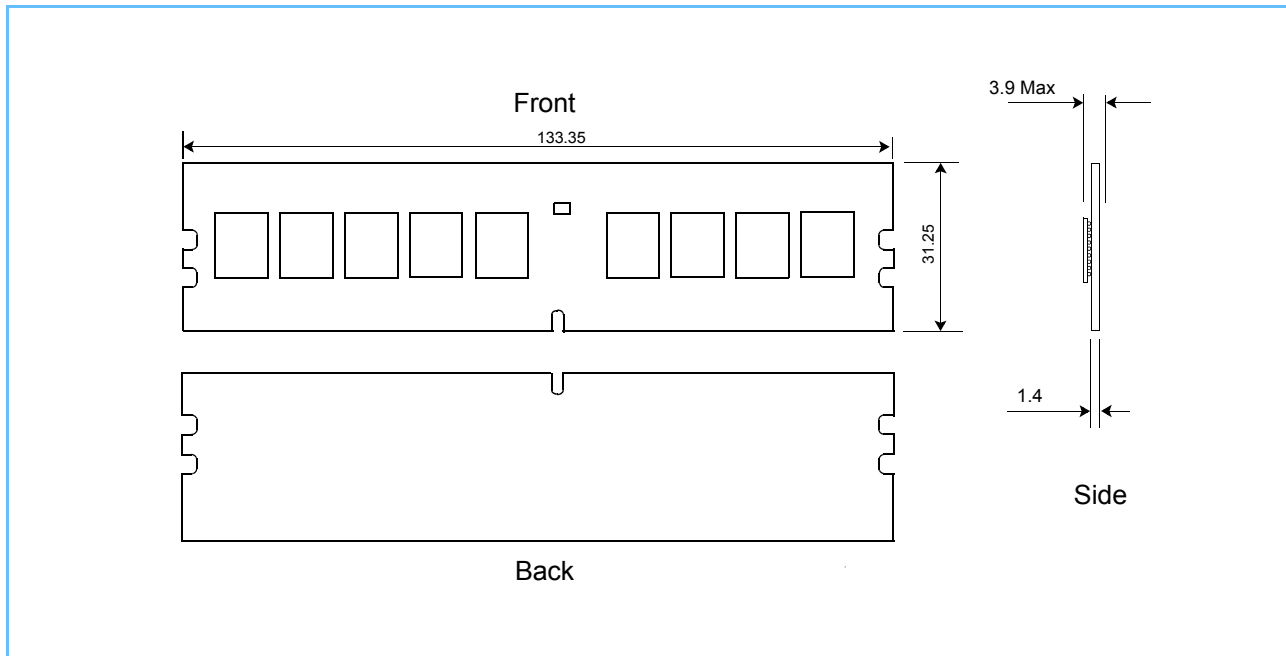
Raw Card	Speed	PC4-1333	PC4-1600	PC4-1866	PC4-2133	PC4-2400	PC4-2666	PC4-3200	Notes
D0	DDR4	P	P	P	P				1, 2

Note 1: X reflects speed grades approved from previous ballots.
Note 2: P denotes speed grades being proposed for this most recent ballot

Design Deviations

1. None.

General Layout



Note 1: Refer to MO-309 for more detailed information.

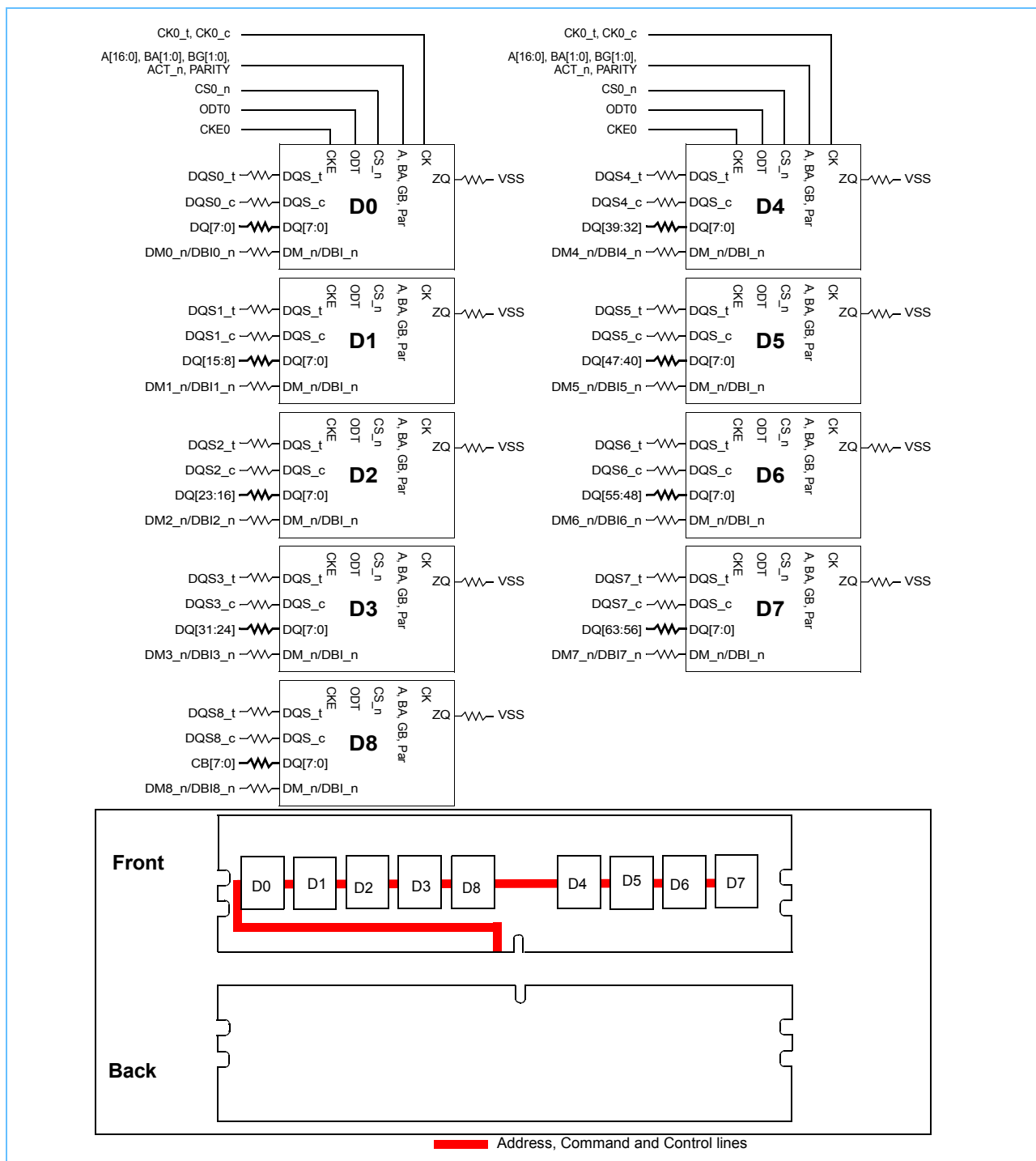
Note 2: Variation is AAxA (A Module height, A Module thickness, x plating, A Key Position).

Note 3: Module thickness may vary with DRAM thickness and passive components.

Proposed

Functional Block Diagram

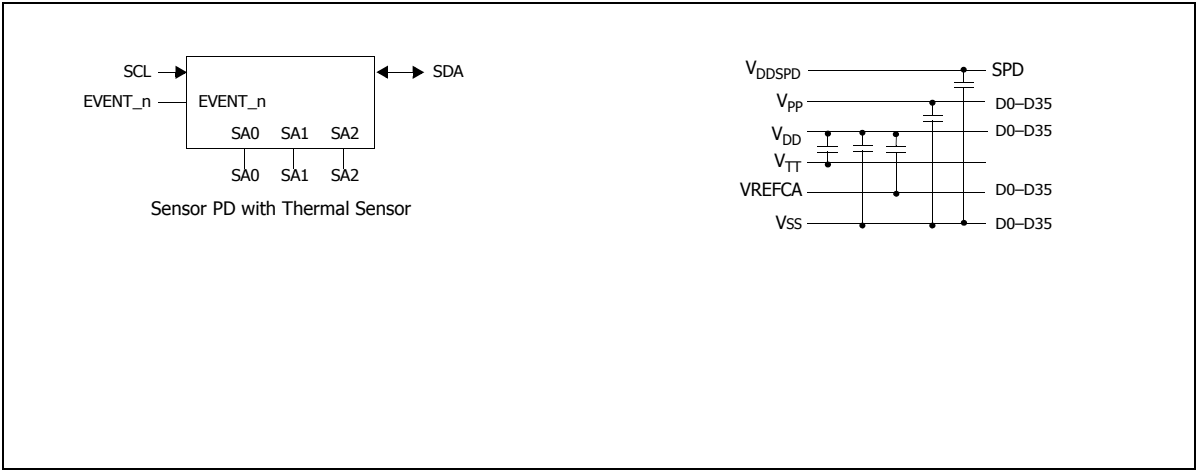
x72 DIMM, populated as one package rank of x8 DDR4 SDRAMs (Part 1 of 1)



Note 1: CK1_t, CK1_c terminated with $120\Omega \pm 5\%$ resistor.

Note 2: Unless otherwise noted resistors are $15\Omega \pm 5\%$.

Note 3: ZQ resistors are $240\Omega \pm 1\%$. For all other resistor values refer to the appropriate wiring diagram.



Proposed