3.2.2 ROM, Word Wide

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3.2.2.1 – 32K TO 256K BY 16 ROM IN DIP

CAPACITY—32K TO 256K WORDS OF 16 BITS,
PACKAGE—40 PIN DIP, 0.6" WIDE
PIN ASSIGNMENTS—Fig. 3.2.2–1

3.2.2.2 – 32K TO 256K BY 16 ROM IN SCC

CAPACITY—32K TO 256K WORDS OF 16 BITS,
PACKAGE—44 PAD (PIN) RCC, 0.650" X 0.650"
PIN ASSIGNMENTS—Fig. 3.2.2–2

3.2.2.3 – 16K TO 256K BY 16 ADDRESS/DATA MX ROM IN DIP

CAPACITY—16K TO 256K WORDS OF 16 BITS,
LOGIC FEATURES—Address and Data MULTIPLEXED onto common pins.
PACKAGE—28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENTS—Figs. 3.2.2–3

3.2.2.4 – 16K TO 256K BY 16 ADDRESS/DATA MX ROM IN RCC

CAPACITY—16K TO 256K WORDS OF 16 BITS,
LOGIC FEATURES—Address and Data MULTIPLEXED onto common pins.
PACKAGE—32 PIN (PAD) RCC, 0.450" X 0.550"
PIN ASSIGNMENTS—Figs. 3.2.2–4

3.2.2.5 – 256K and 512K BY 16 ROM IN QFP

CAPACITY—256K & 512K WORDS OF 16 BITS,
LOGIC FEATURES—These devices can be used with either an 8 or a 16 bit data interface by the appropriate logic control (also see Par. 3.2.2.5).
PACKAGE—44 PIN QFP, 14 mm square with a 1 mm pin pitch
PIN ASSIGNMENT—Fig. 3.2.2–5

3.2.2.6 – 512K TO 128M BY 16 ROM IN DIP AND SOP

CAPACITY—512K, 1M, 2M, 4M, 8M, 16M, 32M, 64M, & 128M WORDS OF 16 BITS
PACKAGE—42, 44, 48 or 52 PIN DIP or SOP, 0.600" WIDE
PIN ASSIGNMENTS—512K TO 2M, Fig. 3.2.2–8
PIN ASSIGNMENTS—4M TO 128M, Fig. 3.2.2–6

3.2.2.7 – 512K and 1M BY 16 ROM IN SCC

CAPACITY—512K & 1M WORDS OF 16 BITS
PACKAGE—44TERMINAL SCC, 0.650" X 0.650"
PIN ASSIGNMENTS—Fig. 3.2.2–7

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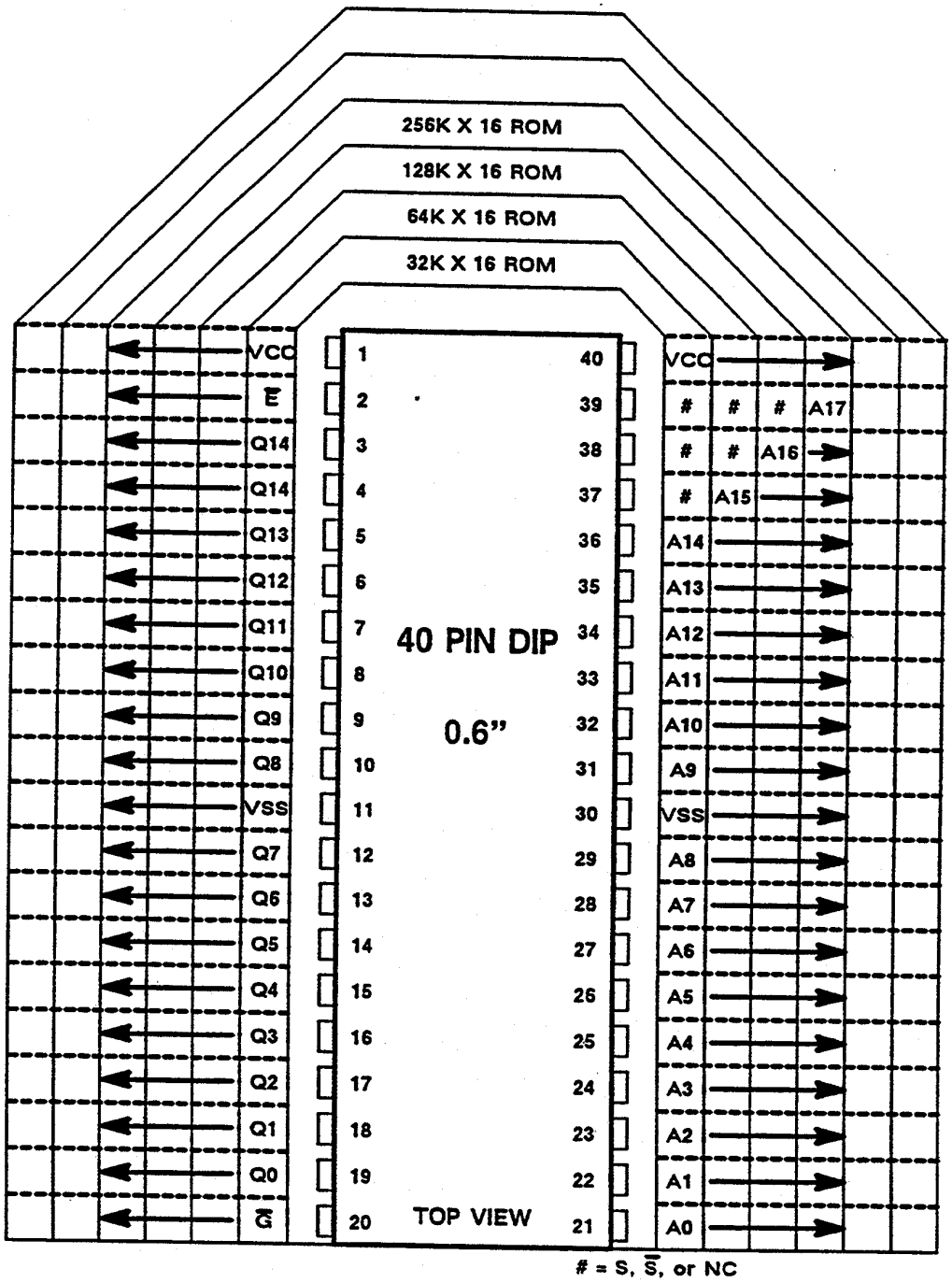


FIGURE 3.2.2-1
32K TO 256K BY 16 ROM IN DIP

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