

3.11.3 BYTE WIDE SDRAM

(NOTE: The pages in this section were renumbered in Release 9. The figures start on P 3.11.3-5)

3.11.3.1 - 2M BY 8 or 9 SDRAM IN TSOP2

CAPACITY--2M WORDS OF 8 or 9 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5

ELECTRICAL INTERFACE--TTL or LVTTTL

PACKAGE--44 Pin TSOP2, 7.62 mm WIDE, 0.8mm PIN PITCH (2M X 8 part only)

PACKAGE--44 Pin TSOP2, 10.16 WIDE, 0.8mm PIN PITCH

PACKAGE--44 Pin SOJ, 10.16 WIDE, 0.8mm PIN PITCH

PIN ASSIGNMENT--Fig. 3.11.3-1

3.11.3.2 - 8M BY 8 SDRAM IN TSOP2

CAPACITY--8M WORDS OF 8 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5

PACKAGE--54 Pin TSOP2, 10.16 mm WIDE, 0.8mm PIN PITCH

PIN ASSIGNMENT--Fig. 3.11.3-2

3.11.3.3 - 32M BY 8 SDRAM PIN ROTATION (OBSOLETE, DO NOT USE)

CAPACITY--32M WORDS OF 8 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5

PACKAGE--TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED

PIN ASSIGNMENT--Fig. 3.11.3-3

NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time. (THIS STANDARD WAS DECLARED OBSOLETE IN 1998)

3.11.3.4 - 8M, 16M, 32M, 64M, & 128M BY 8 DDR SDRAM IN TSOP2

CAPACITY--8M, 16M, 32M, 64M, & 128M WORDS OF 8 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR devices. In Release 11, P19 was redefined to be NU only and QFC was deleted from the Standard.

PACKAGE--66 Pin TSOP2, 10.16 mm WIDE, 0.65 mm PIN PITCH

PIN ASSIGNMENT--Fig. 3.11.3-4

PIN FUNCTION LOCATIONS--This device has the power and data pins located at one end of the package and the control and address pins on the other end.

3.11.3.5 - 16M, 32M, 64M, & 128M BY 8 SDRAM IN TSOP2

CAPACITY--16M, 32M, 64M, & 128M WORDS OF 8 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5

PACKAGE--54 Pin TSOP2, 10.16 mm or 12.70 mm WIDE, 0.8 mm PIN PITCH

PIN ASSIGNMENT--Fig. 3.11.3-5

PIN FUNCTION LOCATIONS--This device has the power and data pins located at one end of the package and the control and address pins on the other end.

3.11.3.6 - 8M, 16M, & 32M BY 8 SDR SDRAM IN TSOP2

CAPACITY--8M, 16M, & 32M WORDS OF 8 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for SDR devices.

PACKAGE--66 Pin TSOP2, 10.16 mm WIDE, 0.65 mm PIN PITCH

PIN ASSIGNMENT--Fig. 3.11.3-6

PIN FUNCTION LOCATIONS--This device has the power and data pins located at one end of the package and the control and address pins on the other end.

3.11.3.7 - 8M, 16M, & 32M BY 8 STACKABLE SDR SDRAM IN LSOJ

CAPACITY--8M, 16M, & 32M WORDS OF 8 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for SDR SDRAM.

PACKAGE--66 Pin STACKABLE LSOJ, 10.16 mm WIDE, 0.65 mm PIN PITCH

PIN ASSIGNMENT--Fig. 3.11.3-7

PIN FUNCTION LOCATIONS--This device has the power and data pins located at one end of the package and the control and address pins on the other end.

3.11.3.8 - 8M, 16M, 32M, 64M, & 128M BY 8 STACKABLE DDR SDRAM IN LSOJ

CAPACITY--8M, 16M, 32M, & 64M WORDS OF 8 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--66 Pin STACKABLE LSOJ, 10.16 mm WIDE, 0.65 mm PIN PITCH

PIN ASSIGNMENT--Fig. 3.11.3-8

PIN FUNCTION LOCATIONS--This device has the power and data pins located at one end of the package and the control and address pins on the other end.

3.11.3.9 - 2M BY 8 SDR SDRAM IN USON

CAPACITY--2M WORDS OF 8 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for SDR SDRAM.

PACKAGE--46 PAD USON, 7 mm WIDE, 0.5 mm Pad Pitch

PIN ASSIGNMENT--Fig. 3.11.3-9

3.11.3.10 - 8M BY 8 SDR SDRAM IN USON

CAPACITY--8M WORDS OF 8 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for SDR SDRAM.

PACKAGE--54 PAD USON, 10 mm WIDE, 0.8 mm Pad Pitch

PIN ASSIGNMENT--Fig. 3.11.3-10

3.11.3.11 - 8M BY 8 VIRTUAL CHANNEL SDRAM IN TSOP2

CAPACITY--16M WORDS OF 4 BITS

LOGIC FEATURES--This device utilizes the Virtual Channel SDRAM architecture

PACKAGE--54 Pin TSOP2, 10.16 mm WIDE, 0.8 mm PIN PITCH

PIN ASSIGNMENT--Fig. 3.11.3-11

PIN FUNCTION LOCATIONS--This device has the power and data pins located at one end of the package and the control and address pins on the other end.

3.11.3.12 - 8M, 16M, & 32M BY 8 VIRTUAL CHANNEL DDR SDRAM IN TSOP2

CAPACITY--8M, 16M, & 32M WORDS OF 8 BITS

LOGIC FEATURES--This device utilizes the Virtual Channel DDR SDRAM architecture

PACKAGE--66 Pin TSOP2, 10.16 mm WIDE, 0.65 mm PIN PITCH

PIN ASSIGNMENT--Fig. 3.11.3-12

PIN FUNCTION LOCATIONS--This device has the power and data pins located at one end of the package and the control and address pins on the other end. ,
QFC was deleted from the Standard.

3.11.3.13 - 8M, 16M, & 32M BY 8 SDR SDRAM IN LFBGA

CAPACITY--8M, 16M, & 32M WORDS OF 8 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for SDR SDRAM.

PACKAGE--15 X 10 Ball LFBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.3-13

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 9, & 10 only.

3.11.3.14 - 8M, & 16M BY 8 DDR SDRAM IN LFBGA

CAPACITY--8M, & 16M WORDS OF 8 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--15 X 10 Ball LFBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.3-14

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 9, & 10 only.

3.11.3.15 - 8M, & 16M BY 8 SDR SDRAM IN LFBGA

CAPACITY--8M, & 16M WORDS OF 8 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for SDR SDRAM.

PACKAGE--15 X 10 Ball LFBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.3-15

BALL LOCATIONS--The package has been depopulated to columns 3, 4, 7, & 8 only.

3.11.3.16 - 8M, 16M, 32M, & 64M BY 8 DDR SDRAM IN 60 Ball LFBGA

CAPACITY--8M, 16M, 32M, & 64M WORDS OF 8 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--15 X 10 Ball LFBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.3-16

BALL LOCATIONS--The package has been depopulated with 60 Balls in columns 3, 4, 7, & 8 only.

3.11.3.17 - 16M, 32M, & 64M BY 8 Low Power SDR SDRAM IN 54 Ball FBGA

CAPACITY--16M, 32M, & 64M WORDS OF 8 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for SDR SDRAM and is optimized for Low Power operation.

PACKAGE--9 X 9, 54 Ball FBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.3-17

BALL LOCATIONS--The package has been depopulated with 54 Balls in columns 1, 2, 3, 7, 8, & 9 only.

3.11.3.18 - 32M, & 64M BY 8 SDR SDRAM IN 60 Ball LFBGA

CAPACITY--32M, & 64M WORDS OF 8 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for SDR SDRAM.

PACKAGE--12 X 9 Ball FBGA, 0.8/1.0 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.3-18

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 3, 7, 8, & 9 only with columns 1 & 9 partially populated.

3.11.3.19 - 16M, 32M, 64M, & 128M BY 8 DDR SDRAM IN 60 Ball FBGA

CAPACITY--16M, 32M, 64M, & 128M WORDS OF 8 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--12 X 9, 60 Ball LFBGA, 0.8/1.0 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.3-19

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 3, 7, 8, & 9 only with columns 1 & 9 partially populated.

3.11.3.20 - 16M, 32M, 64M, & 128M BY 8 DDR SDRAM IN 60 Ball FBGA, with Optional Support Balls

CAPACITY--16M, 32M, 64M, & 128M WORDS OF 8 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--16 X 9, 60 Ball FBGA, 0.8/1.0 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.3-20

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 3, 7, 8, & 9 only with columns 1 & 9 partially populated.

3.11.3.21 - 32M, 64M, 128M, 256M, & 512M BY 8 DDR2 SDRAM IN 60 Ball TFBGA

CAPACITY--32M, 64M, 128M, 256M, & 512M WORDS OF 8 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--11 X 9, 60 Ball TFBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.3-21

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 3, 7, 8, & 9 only with columns 1 & 9 partially populated.

3.11.3.22 - 8M, 16M, 32M, & 64M BY 8 SDRAM IN sTSOP

CAPACITY--8M, 16M, 32M, & 64M WORDS OF 8 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5

PACKAGE--54 Pin sTSO2, 10.16 mm WIDE, 0.4 mm PIN PITCH

PIN ASSIGNMENT--Fig. 3.11.3-22

PIN FUNCTION LOCATIONS--This device has the power and data pins located at one end of the package and the control and address pins on the other end.

3.11.3.23 - 32M, 64M, 128M, 256M, & 512M BY 8 BY 2 DDR2 SDRAM IN STACKED FBGA

CAPACITY--32M, 64M, 128M, 256M, & 512M WORDS OF 4 BITS BY TWO CHIPS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--11 X 9, 60 Ball STACKED FBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.3-23

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 3, 7, 8, & 9 only with columns 1 & 9 partially populated.

3.11.3.24 - 32M, 64M, 128M, 256M, & 512M BY 8 BY 2 DDR2 SDRAM FOR STACKED FBGA REQUIRING SUPORT BALLS

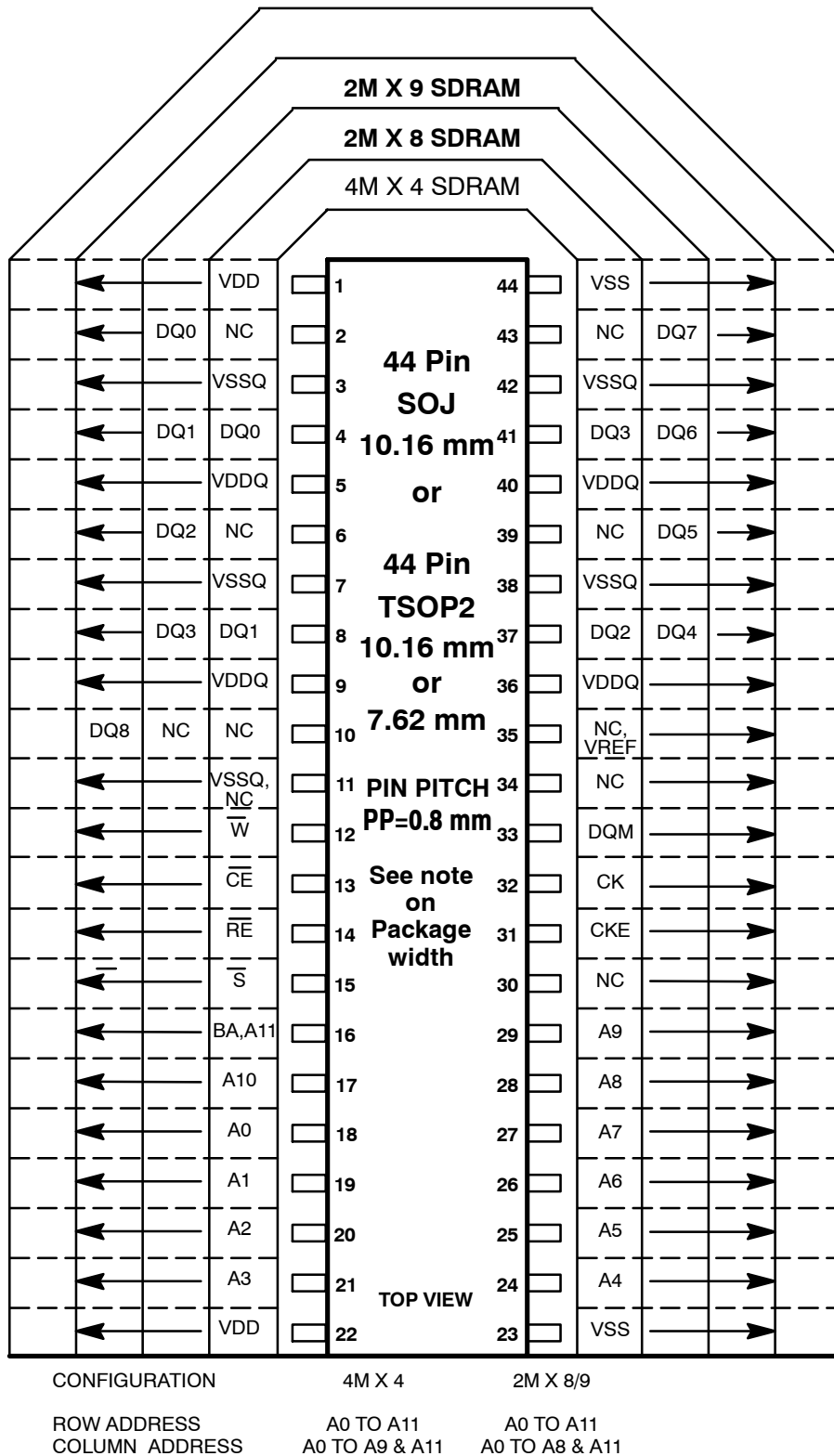
CAPACITY--32M, 64M, 128M, 256M, & 512M WORDS OF 8 BITS BY TWO CHIPS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--11 X 9, 60 Ball STACKED FBGA, 0.8 mm Ball Pitch,

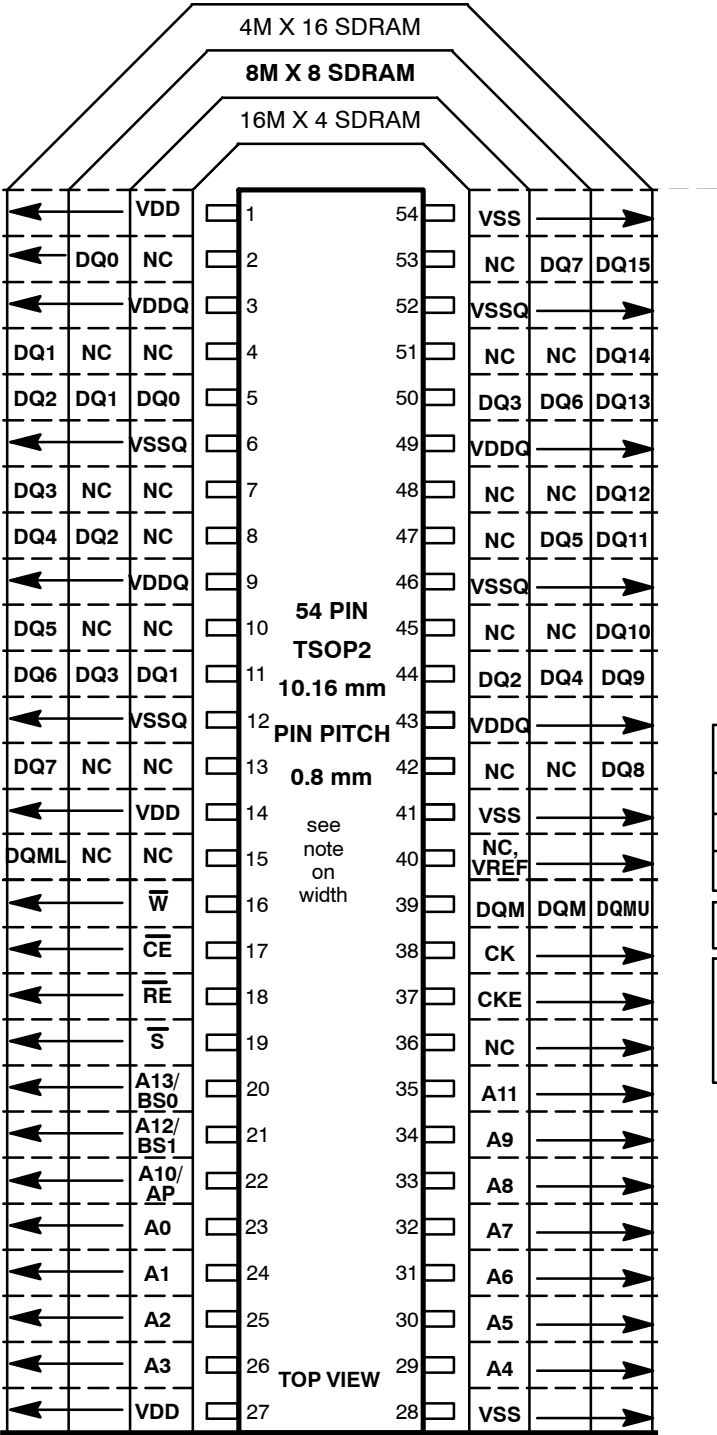
PIN ASSIGNMENT--Fig. 3.11.3-24

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 3, 7, 8, & 9 only with columns 1 & 9 partially populated.



- Notes:
- 1) The VREF option on P35 was added when the 0.3" package was approved.
 - 2) The JEDEC Std. No 30 designator for the TSOP2 package is PDSO-G. The 4M X 4 and 2M X 8 parts are also approved for delivery in a 7.62 mm package.

FIGURE 3.11.3-1
2M BY 8 OR 9 SDRAM IN TSOP2



	ROW ADDR.	COL ADDR
X4	A0⇒A13	A0⇒A9
X8	A0⇒A13	A0⇒A8
X16	A0⇒A13	A0⇒A7

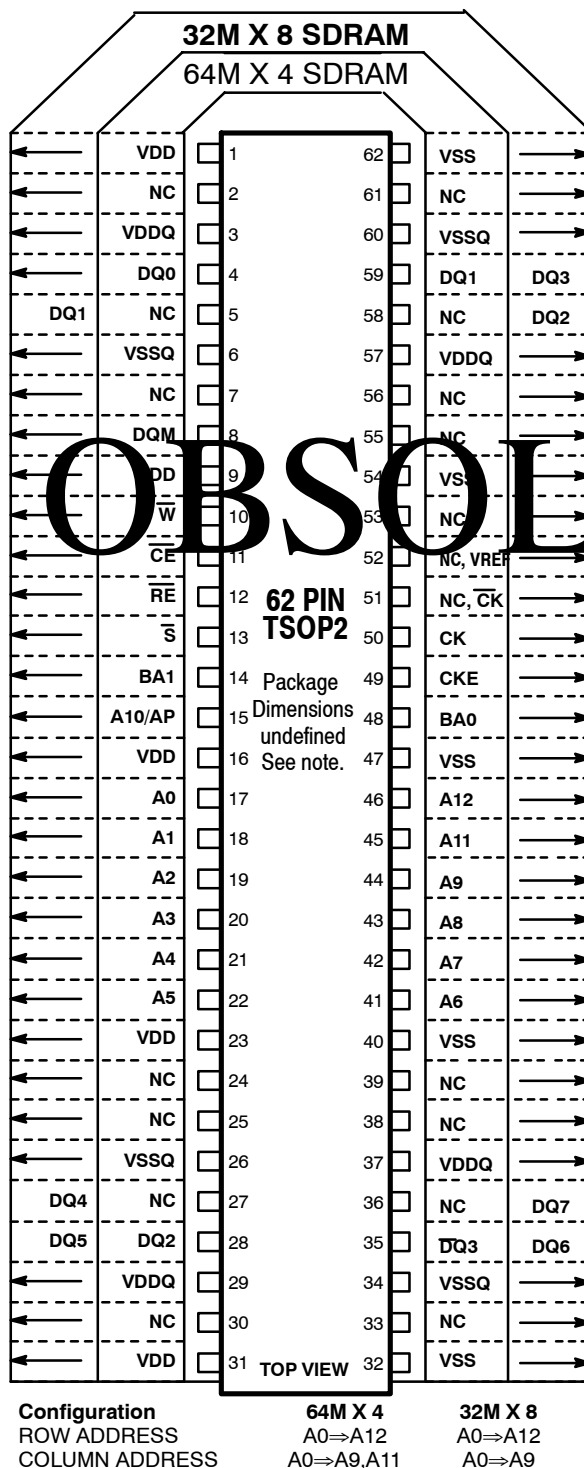
A10	AUTO PRECHARGE
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BANKS	BANK SELECT ADDRESS
4	A13/A12
2	A13

* PACKAGE NOTES:

The JEDEC Std. 30 term for the TSOP-2 package is PDSO-G.

FIGURE 3.11.3-2
8M BY 8 SDRAM IN TSOP2



NOTES

1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

2. CBR refresh is the only standardized method of refreshing non-synchronous DRAMs with densities of 256Mb and higher.

3. The standard refresh interval (tREF) for 256Mb DRAMs is 64ms (7.8 μs per row with 8K rows, 3.9 μs with 16K rows).

4. (NC, VREF) is VREF on devices that require an external voltage reference.

5. The VDDQ designator is used when the power supply pins for the DQ I/O drivers are internally dc isolated from the other VDD power supply pins.

6. The VSSQ designator is used when the ground reference pins for the DQ I/O drivers are internally isolated from the primary ground references (VSS).

7. BA0 is the Least Significant Bank Addr.

8. BA1 is the Most Significant Bank Addr.

9. A10/AP is row addr. A10, autoprecharge and precharge all banks input.

* NOTE: The JEDEC Std. 0 term for the TSOP-2 package is PDSO-G.

Note: This pin rotation is obsolete and will not be assigned to a package

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

FIGURE 3.11.3-3
32M BY 8 SDRAM PIN ROTATION IN TSOP2

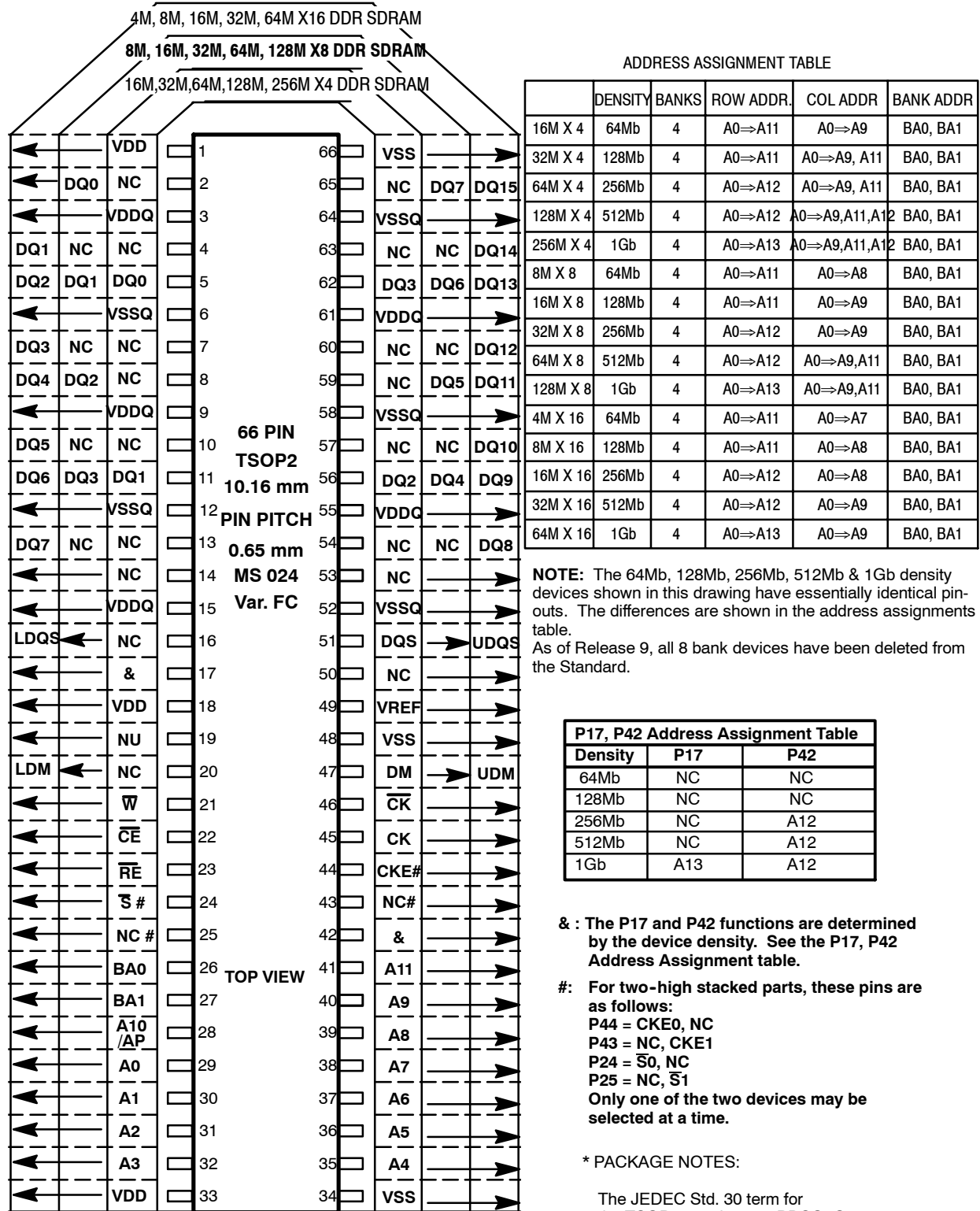


FIGURE 3.11.3-4
8M, 16M, 32M, 64M, & 128M BY 8 DDR SDRAM IN TSOP2

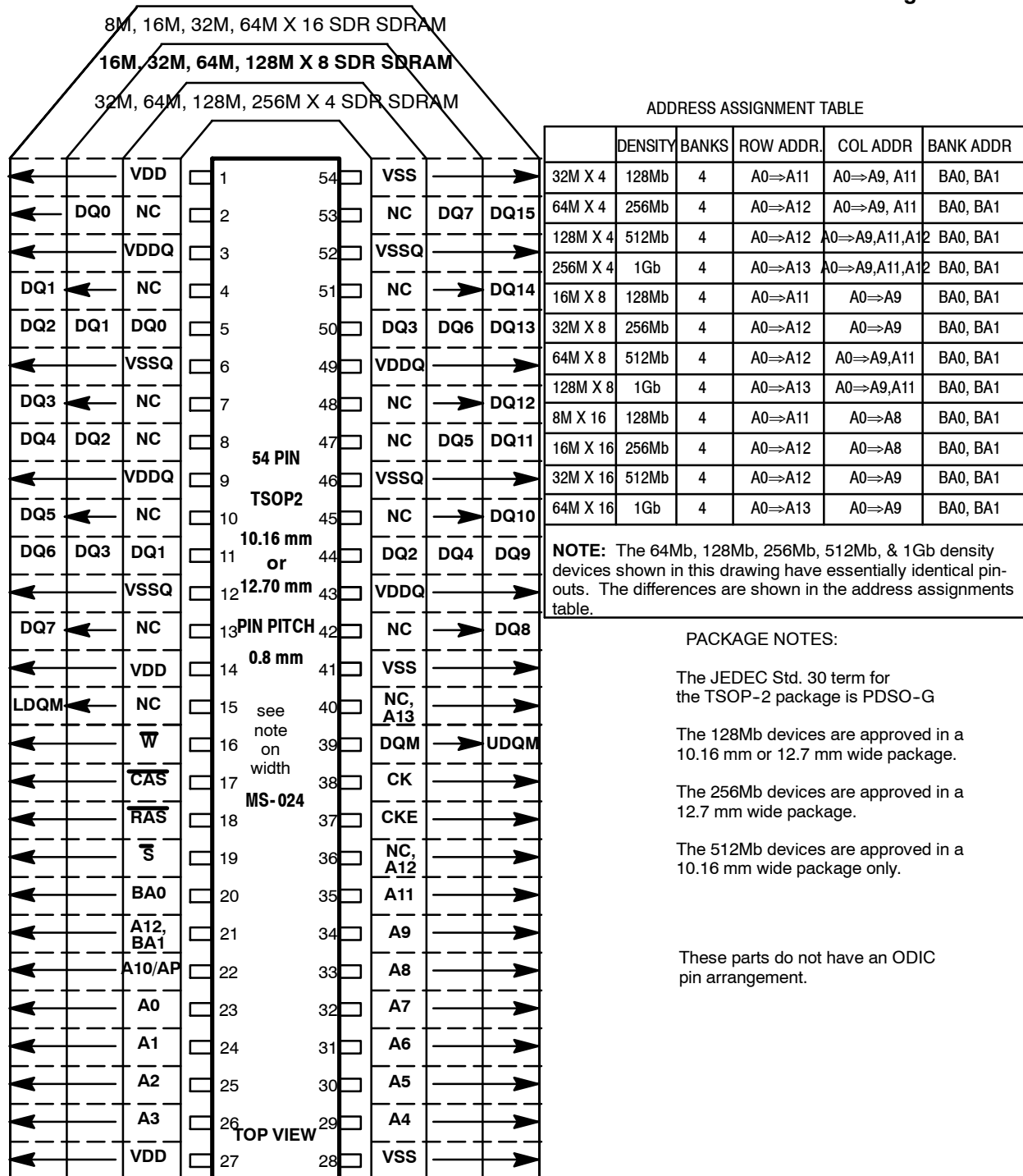


FIGURE 3.11.3-5
16M, 32M, 64M, & 128M X 8 SDRAM IN TSOP2

Release 8r9r10r12