

3.11.4 WORD WIDE SDRAM

3.11.4.1 - 256K BY 16 AND 1M BY 16 & 18 SDRAM IN TSOP2

CAPACITY--256K WORDS OF 16 BITS AND 1M WORDS OF 16 OR 18

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5

ELECTRICAL INTERFACE--TTL or LOWER LEVEL INTERFACE CONSISTENT WITH THE
VALUE OF VDD CHOSEN.

PACKAGE--50 Pin SOJ, 10.16 mm WIDE, 0.8mm PIN PITCH

PACKAGE--50 Pin TSOP2, 0.400" WIDE (10.16 mm), 0.8mm PIN PITCH

PIN ASSIGNMENT--Fig. 3.11.4-1

NOTE: The 256K part has the same pinout as the SGRAM part shown in Fig. 3.10.3-3 with the exception of the DSF function on P 33.

3.11.4.2 - 2M & 4M BY 16 SDRAM IN TSOP2

CAPACITY--2M or 4M WORDS OF 16 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5

PACKAGE--54 Pin TSOP2, 10.16 mm WIDE, 0.8mm PIN PITCH

PIN ASSIGNMENT--Fig. 3.11.4-2

3.11.4.3 - 16M BY 16 SDRAM IN TSOP2 PIN ROTATION (OBSOLETE, DO NOT USE)

CAPACITY--16M WORDS OF 16 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5

--This standard is for a 4 Bank version only.

PACKAGE--TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED

PIN ASSIGNMENT--Fig. 3.11.4-3

NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time. (THIS STANDARD WAS DECLARED OBSOLETE IN 1998)

3.11.4.4 - 128K, & 256K BY 32, 2 BANK SDRAM IN QFP, TQFP, or PQFP

128K, 256K, & 512K BY 32, 4 BANK SDRAM IN LQFP

CAPACITY--128K, 256K, or 512K WORDS OF 32 BITS BY 2 BANKS

128K, 256K, or 512K WORDS OF 32 BITS BY 4 BANKS

LOGIC FEATURES--Multiplexed Address

--Synchronous address & control interface.

PACKAGE--100 PIN QFP, TQFP, OR LQFP 20 mm X 14 mm, 0.65 mm PP (Depending on configuration)

PIN ASSIGNMENTS--FIG. 3.11.4-4

NOTE: This part has the same pinout as the SDRAM part shown in Fig. 3.10.3-4 with the exception of the DSF function on P 33.

3.11.4.5 - 2M BY 32 SDRAM IN TSOP2

CAUTION: See note in Fig. 3.11.4-5 regarding the use of this device.

CAPACITY--2M WORDS OF 32 BITS

LOGIC FEATURES--Multiplexed Address

--Synchronous address & control interface.

PACKAGE--84 PIN TSOP2, 10.16 mm WIDE, 0.5 mm PP

PIN ASSIGNMENTS--FIG. 3.11.4-5

3.11.4.6 - 8M BY 32 SDRAM IN TSOP2 PIN ROTATION (OBSOLETE, DO NOT USE)

CAPACITY--8M WORDS OF 32 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5

--This standard is for a 4 Bank version only.

PACKAGE--TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED

PIN ASSIGNMENT--Fig. 3.11.4-6

NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time. (THIS STANDARD WAS DECLARED OBSOLETE IN 1998)

3.11.4.7 - 2M BY 32 & 36, 4M & 8M BY 32 SDRAM IN TSOP2

CAPACITY--2M WORDS OF 32 OR 36 BITS, 4M & 8M WORDS OF 32 BITS.

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5

--This standard is for a 2 & 4 Bank versions.

PACKAGE--86 PIN TSOP2, 10.16 mm Wide, 0.5 mm PP

PIN ASSIGNMENT--Fig. 3.11.4-7

3.11.4.8 - 4M, 8M, 16M, 32M, & 64M BY 16 DDR SDRAM IN TSOP2

CAPACITY--4M, 8M, 16M, 32M, & 64M WORDS OF 16 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR devices. In Release 11, P19 was redefined to be NU only and QFC was deleted from the Standard.

PACKAGE--66 Pin TSOP2, 10.16 mm WIDE, 0.65 mm PIN PITCH

PIN ASSIGNMENT--Fig. 3.11.4-8

PIN FUNCTION LOCATIONS--This device has the power and data pins located at one end of the package and the control and address pins on the other end.

3.11.4.9 - 8M, 16M, 32M, & 64M BY 16 SDRAM IN TSOP2

CAPACITY--8M, 16M, 32M, & 64M WORDS OF 16 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5

PACKAGE--54 Pin TSOP2, 10.16 mm or 12.70 mm WIDE, 0.8 mm PIN PITCH

PIN ASSIGNMENT--Fig. 3.11.4-9

PIN FUNCTION LOCATIONS--This device has the power and data pins located at one end of the package and the control and address pins on the other end.

3.11.4.10 - 4M, 8M, & 16M BY 16 SDR SDRAM IN TSOP2

CAPACITY--4M, 8M, & 16M WORDS OF 8 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for SDR devices.

PACKAGE--66 Pin TSOP2, 10.16 mm WIDE, 0.65 mm PIN PITCH

PIN ASSIGNMENT--Fig. 3.11.4-10

PIN FUNCTION LOCATIONS--This device has the power and data pins located at one end of the package and the control and address pins on the other end.

3.11.4.11 - 4M, 8M, & 16M BY 16 STACKABLE SDR SDRAM IN LSOJ

CAPACITY--4M, 8M, & 16M WORDS OF 16 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for SDR SDRAM.

PACKAGE--66 Pin STACKABLE LSOJ, 10.16 mm WIDE, 0.65 mm PIN PITCH

PIN ASSIGNMENT--Fig. 3.11.4-11

PIN FUNCTION LOCATIONS--This device has the power and data pins located at one end of the package and the control and address pins on the other end.

3.11.4.12 - 4M, 8M, 16M, 32M, & 64M BY 16 STACKABLE DDR SDRAM IN LSOJ

CAPACITY--4M, 8M, 16M, 32M, & 64M WORDS OF 16 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--66 Pin STACKABLE LSOJ, 10.16 mm WIDE, 0.65 mm PIN PITCH

PIN ASSIGNMENT--Fig. 3.11.4-12

PIN FUNCTION LOCATIONS--This device has the power and data pins located at one end of the package and the control and address pins on the other end.,
QFC was deleted from the Standard.

3.11.4.13 - 4M BY 16 SDR SDRAM IN USON

CAPACITY--4M WORDS OF 16 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for SDR SDRAM.

PACKAGE--54 PAD USON, 10 mm WIDE, 0.8 mm Pad Pitch

PIN ASSIGNMENT--Fig. 3.11.4-13

3.11.4.14 - 4M BY 16 VIRTUAL CHANNEL SDRAM IN TSOP2

CAPACITY--4M WORDS OF 16 BITS

LOGIC FEATURES--This device utilizes the Virtual Channel SDRAM architecture

PACKAGE--54 Pin TSOP2, 10.16 mm WIDE, 0.8 mm PIN PITCH

PIN ASSIGNMENT--Fig. 3.11.4-14

PIN FUNCTION LOCATIONS--This device has the power and data pins located at one end of the package and the control and address pins on the other end.

3.11.4.15 - 4M, 8M, & 16M BY 16 VIRTUAL CHANNEL DDR SDRAM IN TSOP2

CAPACITY--4M, 8M, & 16M WORDS OF 16 BITS

LOGIC FEATURES--This device utilizes the Virtual Channel DDR SDRAM architecture

PACKAGE--66 Pin TSOP2, 10.16 mm WIDE, 0.65 mm PIN PITCH

PIN ASSIGNMENT--Fig. 3.11.4-15

PIN FUNCTION LOCATIONS--This device has the power and data pins located at one end of the package and the control and address pins on the other end.,
QFC was deleted from the Standard.

3.11.4.16 - 4M, 8M, & 16M BY 16 SDR SDRAM IN LFBGA

CAPACITY--4M, 8M, & 16M WORDS OF 16 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for SDR SDRAM.

PACKAGE--15 X 10 Ball LFBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.4-16

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 9, & 10 only.

3.11.4.17 - 4M, & 8M BY 16 DDR SDRAM IN LFBGA

CAPACITY--4M, & 8M WORDS OF 16 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--15 X 10 Ball LFBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.4-17

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 9, & 10 only.

3.11.4.18 - 4M, & 8M BY 16 SDR SDRAM IN LFBGA

CAPACITY--4M, & 8M WORDS OF 16 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for SDR SDRAM.

PACKAGE--15 X 10 Ball LFBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.4-18

BALL LOCATIONS--The package has been depopulated to columns 3, 4, 7, & 8 only.

3.11.4.19 - 4M, & 8M BY 16 DDR SDRAM IN LFBGA

CAPACITY--4M, 8M, 16M, & 32M WORDS OF 16 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--15 X 10 Ball LFBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.4-19

BALL LOCATIONS--The package has been depopulated to 60 Balls in columns 3, 4, 7, & 8 only.

3.11.4.20 - 4M BY 16/18 SLDRAM IN TSOP2

CAPACITY--4M WORDS OF 16 OR 18 BITS

LOGIC FEATURES--This device will conform to the functional characteristics defined for SLDRAM.

PACKAGE--80 PIN TSOP2, 10.16 mm WIDE, 0.5 mm Pin Pitch

PIN ASSIGNMENT--Fig. 3.11.4-20

3.11.4.21 - 4M TO 64M BY 16/18 SLDRAM IN R-PZIP

CAPACITY--4M, 8M, 16M, 32M, OR 64M WORDS OF 16 OR 18 BITS

LOGIC FEATURES--This device will conform to the functional characteristics defined for SLDRAM.

PACKAGE--64 PIN R-PZIP, 0.8 mm Pin Pitch

PIN ASSIGNMENT--Fig. 3.11.4-21

3.11.4.22 - 128K, 256K, & 512K BY 32, 4 BANK DDR SDRAM IN LQFP/TQFP

CAPACITY--128K, 256K, 512K, & 1M WORDS OF 32 BITS BY 4 BANKS

LOGIC FEATURES--Multiplexed Address

--DDR MULTIPLE CAPACITIES OF 32 BITS BY 4 BANKS

--Synchronous address & control interface.

--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

--PACKAGE--100 PIN QFP, TQFP, OR LQFP 20 mm X 14 mm,

--PACKAGE--100 PIN L-PQFP & T-PQFP FOR 1M Device

--0.65 mm PP (Depending on configuration)

PIN ASSIGNMENTS--FIG. 3.11.4-22

NOTE: This part has the same pinout as the SGRAM part shown in Fig. 3.10.3-8 with the exception of the DSF function on P 33.

3.11.4.23 - 2M & 4M BY 32 DDR SDRAM (4 BANK) IN FBGA

CAPACITY--4M WORDS OF 32 BITS Organized as 4 Banks

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM. It can be optionally used as an SGRAM.

PACKAGE--12 X 12 Ball LFBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.4-23

BALL LOCATIONS--The package has all balls populated except as the noted option for the central 16 thermal balls.

3.11.4.24 - 4M, 8M, 16M, & 32M BY 16, Low Power, SDR SDRAM IN FBGA

CAPACITY--4M, 8M, 16M, & 32M WORDS OF 16 BITS Organized as 4 Banks

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

It is optimized for Low Power operation

PACKAGE--9 X 9, 54 Ball FBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.4-24

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 3, 7, 8, & 9 only.

3.11.4.25 - 16M & 32M BY 16 SDR SDRAM IN FBGA

CAPACITY--16M & 32M WORDS OF 16 BITS Organized as 4 Banks

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for SDR SDRAM.

PACKAGE--12 X 9 Ball LFBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.4-25

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 3, 7, 8, & 9 only with columns 1 & 9 partially populated.

3.11.4.26 - 8M, 16M, 32M, & 64M BY 16 DDR SDRAM IN FBGA

CAPACITY--8M, 16M, 32M, & 64M WORDS OF 16 BITS.

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--12 X 9, 60 Ball FBGA, 0.8/1.0 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.4-26

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 3, 7, 8, & 9 only with columns 1 & 9 partially populated.

3.11.4.27 - 2M & 4M BY 32 SDR SDRAM IN LFBGA

CAPACITY--4M WORDS OF 32 BITS Organized as 4 Banks

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for SDR SDRAM.

PACKAGE--15 X 10, 90 Ball LFBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.4-27

BALL LOCATIONS--The package has been depopulated to columns 2, 3, 4, 7, 8, & 9 only.

3.11.4.28 - 2M, 4M, 8M, & 16M BY 32 SDR, Low Power SDRAM IN FBGA

CAPACITY--2M, 4M, 8M, & 16M WORDS OF 32 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for SDR SDRAM.

PACKAGE--15 X 9, 90 Ball FBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.4-28

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 3, 7, 8, & 9 only.

3.11.4.29 - 8M, 16M, 32M, & 64M BY 16 DDR SDRAM IN FBGA with Optional Support Balls

CAPACITY--8M, 16M, 32M, & 64M WORDS OF 16 BITS.

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--12 X 9, 60 Ball FBGA, 0.8/1.0 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.4-29

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 3, 7, 8, & 9 only with columns 1 & 9 partially populated.

3.11.4.30 - 16M, 32M, 64M, 128M, & 256M BY 16 DDR2 SDRAM IN TFBGA

CAPACITY--16M, 32M, 64M, 128M, & 256M WORDS OF 16 BITS.

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--15 X 9, 60 Ball FBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.4-30

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 3, 7, 8, & 9 only with columns 1 & 9 partially populated.

3.11.4.31 - 4M, 8M, 16M, & 32M BY 16 SDRAM IN sTSOP

CAPACITY--4M, 8M, 16M, & 32M WORDS OF 16 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5

PACKAGE--54 Pin sTSO2, 10.16 mm WIDE, 0.4 mm PIN PITCH

PIN ASSIGNMENT--Fig. 3.11.4-31

PIN FUNCTION LOCATIONS--This device has the power and data pins located at one end of the package and the control and address pins on the other end.

3.11.4.32 - 16M, 32M, 64M, 128M, & 256M BY 16 BY 2 DDR2 SDRAM IN STACKED FBGA

CAPACITY--16M, 32M, 64M, 128M, & 256M WORDS OF 16 BITS BY TWO CHIPS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--15 X 9, 90 Ball STACKED FBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.4-32

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 3, 7, 8, & 9 only with columns 1 & 9 partially populated.

3.11.4.33 - 16M, 32M, 64M, 128M, & 256M BY 16 BY 2 DDR2 SDRAM FOR STACKED FBGA REQUIRING SUPORT BALLS

CAPACITY--16M, 32M, 64M, 128M, & 256M WORDS OF 16 BITS BY TWO CHIPS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--15 X 9, 90 Ball STACKED FBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.4-33

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 3, 7, 8, & 9 only with columns 1 & 9 partially populated.

3.11.4.34 - 4M BY 32 DDR2 SDRAM IN 144-BALL LF-XBGA

CAPACITY--4M WORDS OF 32 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--12 X 12 Ball LFBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.4-34

BALL LOCATIONS--The package has all balls populated except as the noted option for the central 16 thermal balls.

3.11.4.35 - 8M8 BY 16 DDR SDRAM in 78-Ball BGA

CAPACITY--8M WORDS OF 16 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--13 X 10, 78 Ball BGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.4-35

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 3, 8, 9, & 10 only.

3.11.4.36 - 8M, 16M & 32M BY 32 Low Power DDR SDRAM IN 90-BALL FBGA

CAPACITY--8M, 16M, and 32M WORDS OF 32 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--15 X 9 Ball FBGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.4-36

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 3, 7, 8, & 9 only.

3.11.4.37 - 256M, 512M, 1G, & 2G BY 32 DDR2 SDRAM IN 128-BALL BGA

CAPACITY--256M, 512M, 1G, and 2G WORDS OF 32 BITS

LOGIC FEATURES--This device will contain all of the logic features described in Sec. 3.11.5 for DDR SDRAM.

PACKAGE--16 X 12 Ball BGA, 0.8 mm Ball Pitch,

PIN ASSIGNMENT--Fig. 3.11.4-37

BALL LOCATIONS--The package has been depopulated to columns 1, 2, 3, 4, 9, 10, 11, & 12 only.

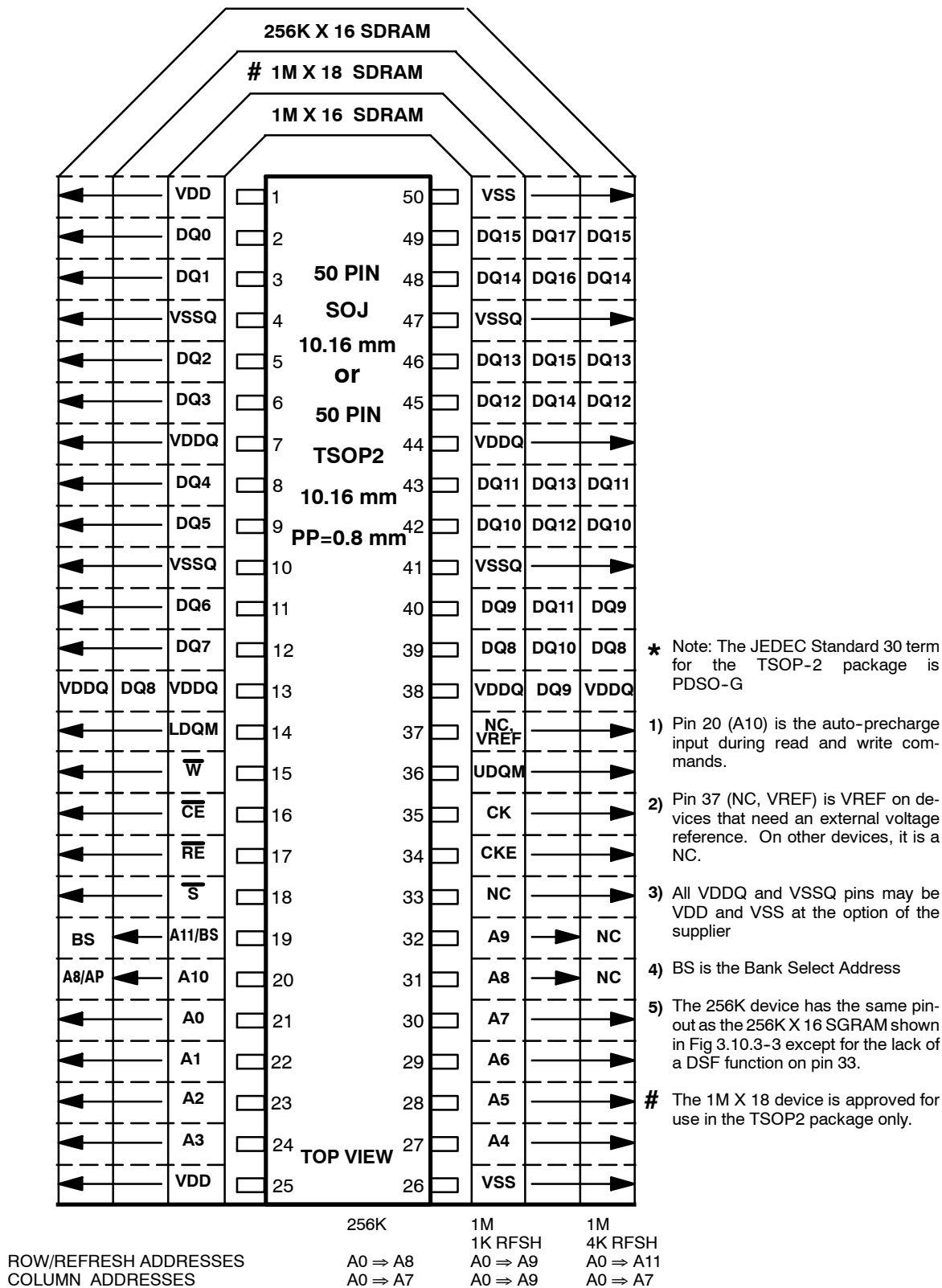


FIGURE 3.11.4-1
256K X 16 & 1M X 16/18 SDRAM IN SOJ & TSOP-2

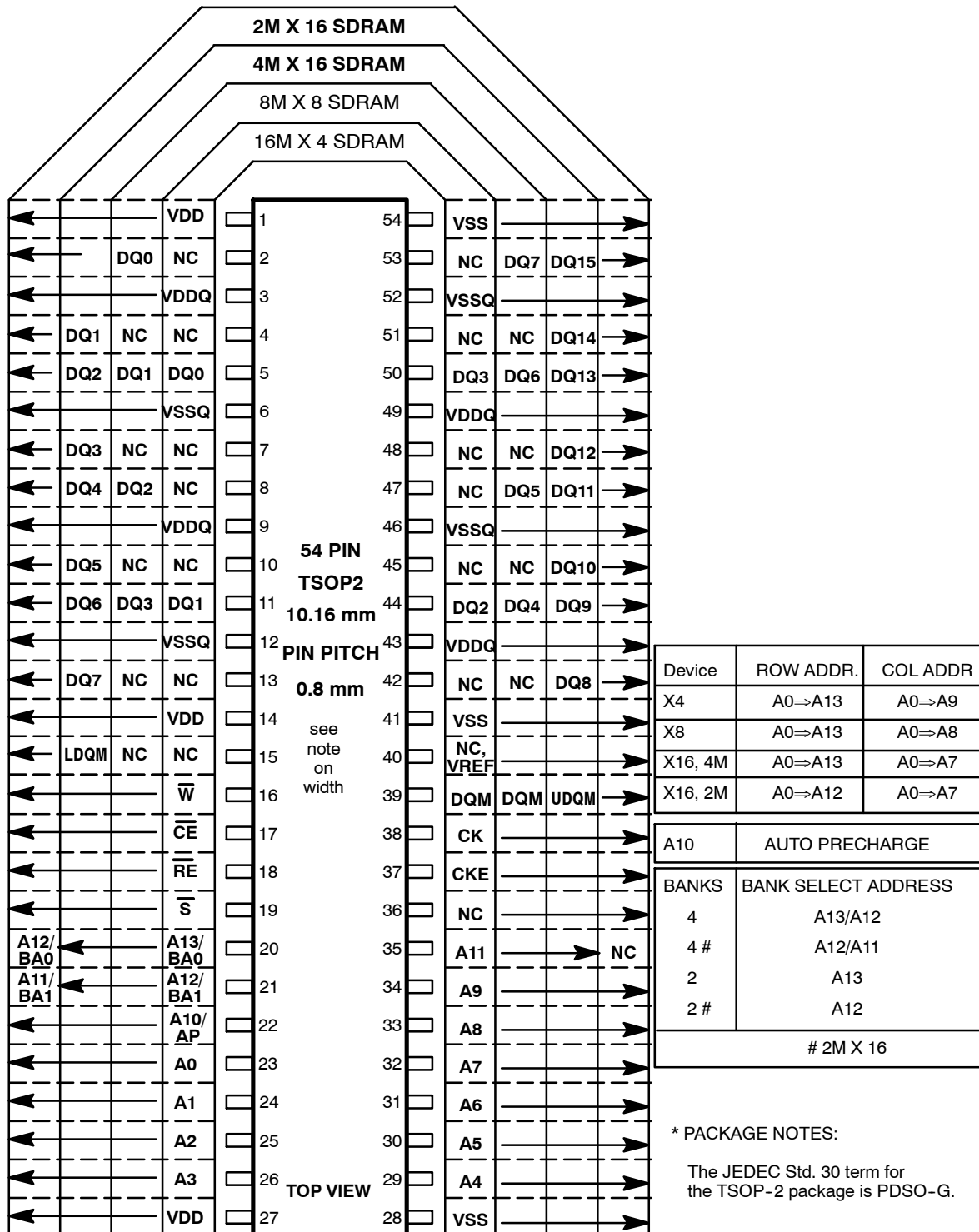
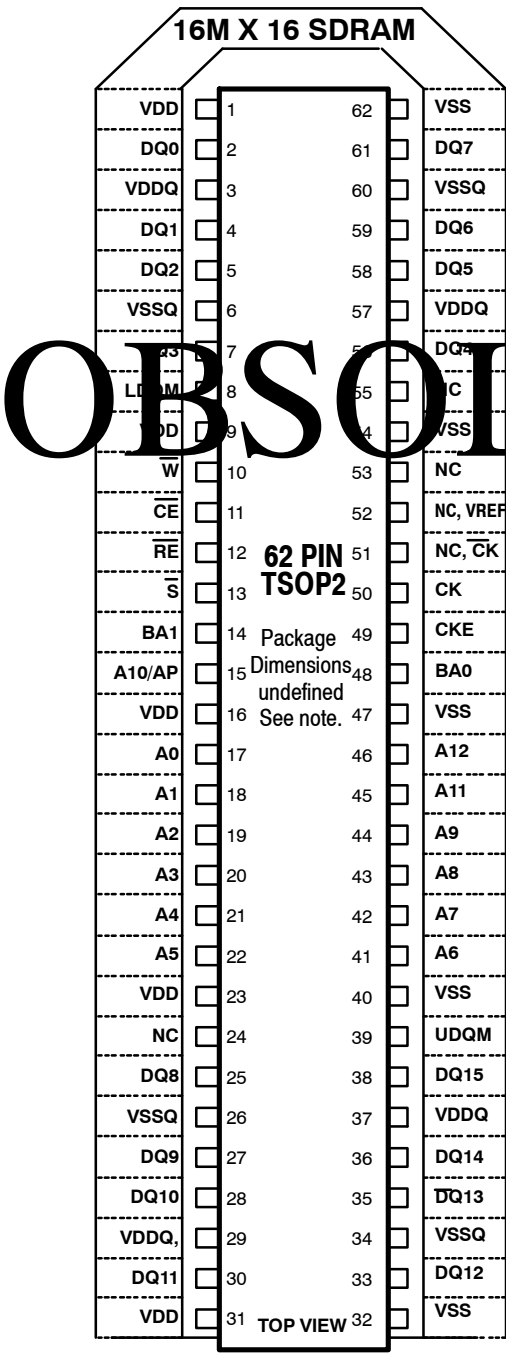


FIGURE 3.11.4-2
2M & 4M BY 16 SDRAM IN TSOP2



- NOTES
1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.
 2. The standard refresh interval (tREF) for 256Mb SDRAMs is 64ms.
 3. (NC, VREF) is VREF on devices that require an external voltage reference.
 4. BA0 is the least significant bank address
 5. BA1 is the most significant bank address
 6. A10/AP is row address A10, autoprecharge and precharge all banks.
 7. (NC, CK) is NC for devices using a single ended clock. CK is used for devices using a differential clock.
 8. (NC, VREF) is VREF on devices that require an external voltage reference.
 9. This standard is for a 4 Bank version only.

* NOTE: The JEDEC Std.
30 term for the TSOP-2
package is PDSO-G.

Note: This pin rotation is obsolete and will not be assigned to a package

Configuration 16M X 16
ROW ADDRESS A0-A12
COLUMN ADDRESS A0-A8

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

FIGURE 3.11.4-3
16M BY 16 SDRAM PIN ROTATION IN TSOP2

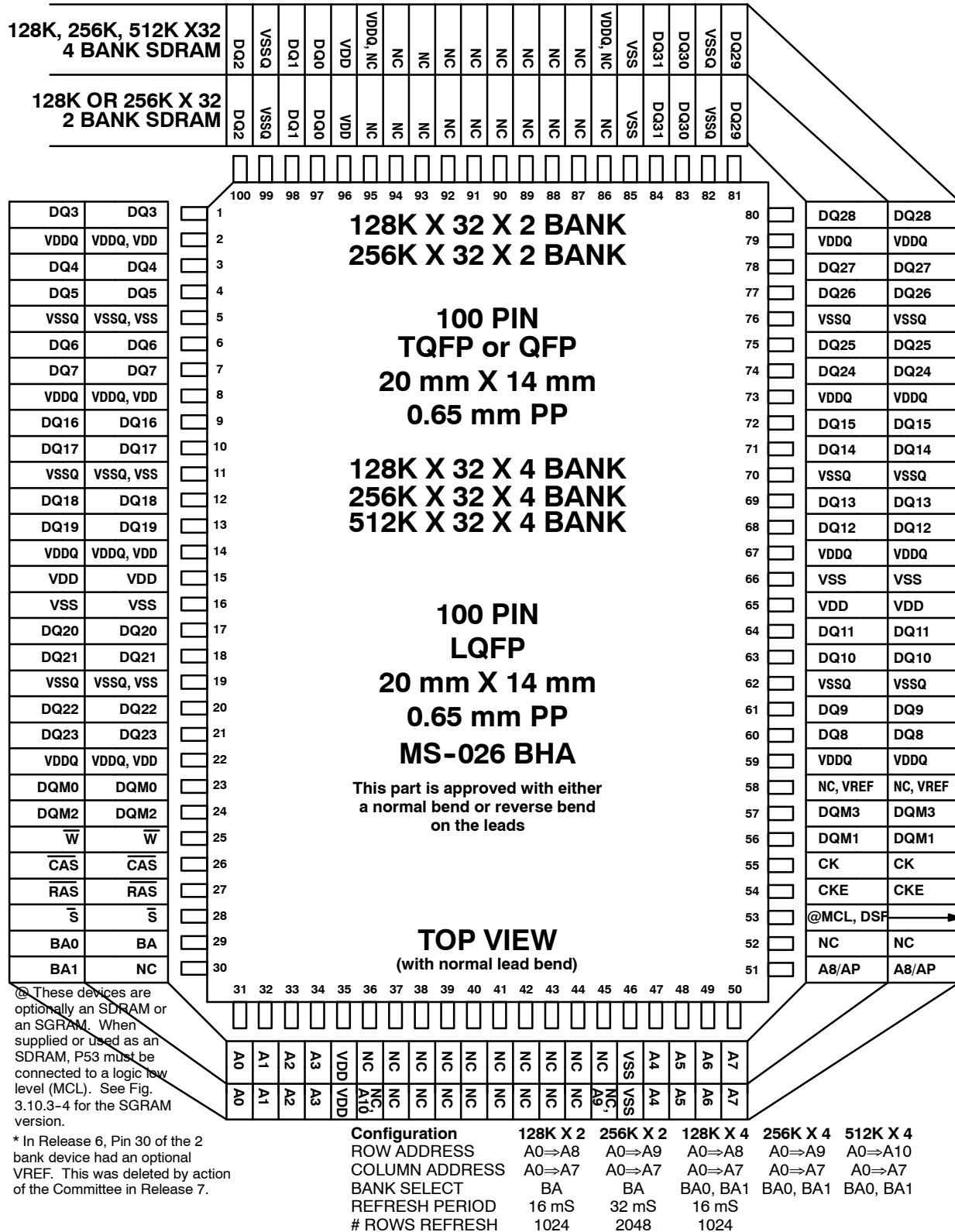
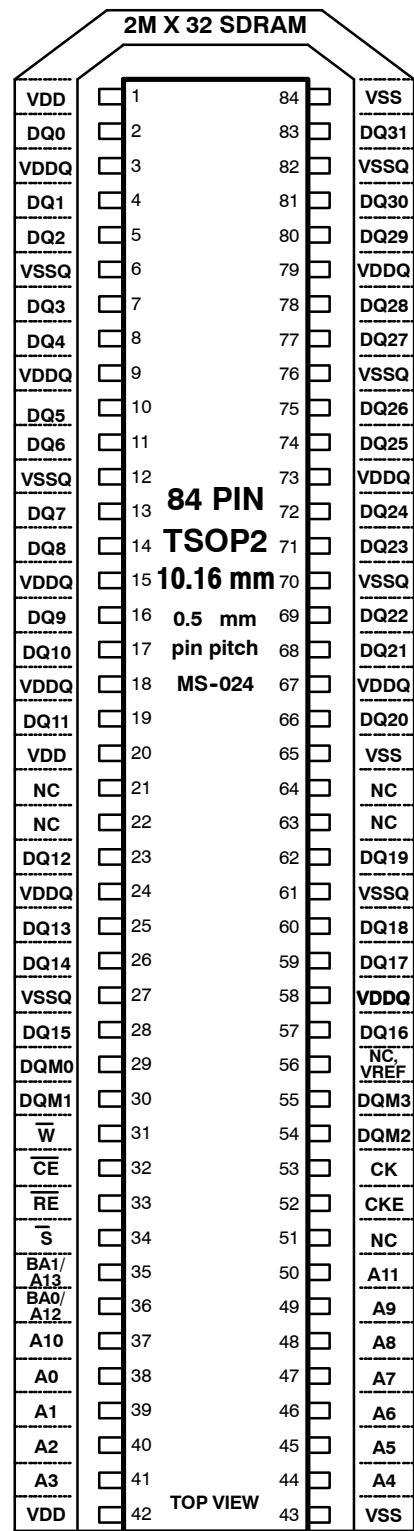


FIGURE 3.11.4-4
128K, 256K & 512K BY 32 BY 2 & 4 BANK SDRAM IN QFP

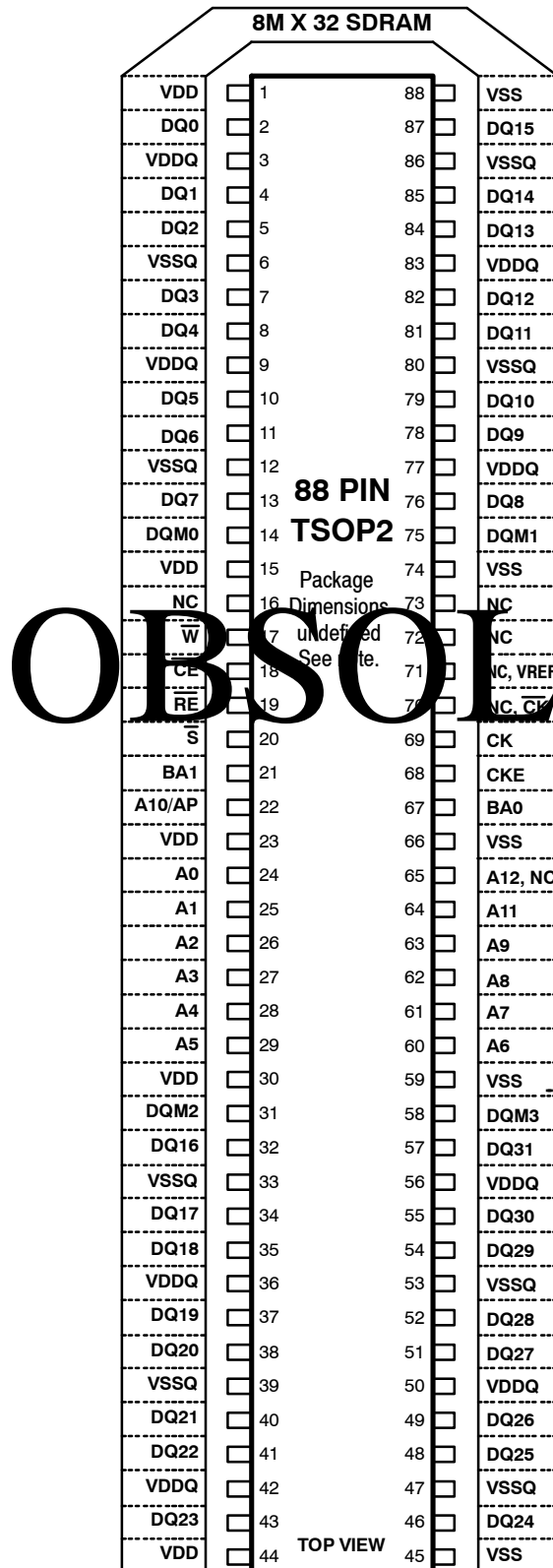


NOTE:
In addition to this pinout for a 2M X 32 SDRAM, there is another one that has the DQ pins at the outer ends of the package and the control pins in the center and superceeds this one. The other device should be used for all new designs. It is found in figure 3.11.4-7.

The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO-G

ADDRESS ORGANIZATION		
NUMBER BANKS	2	4
ROW ADDR.	A0⇒A13	A0⇒A13
COL. ADDR.	A0⇒A6	A0⇒A6
AUTO-PRECHARGE	A10	A10
BANK ADDRESS	A13	A12, A13

FIGURE 3.11.4-5
2M BY 32 SDRAM IN TSOP2



NOTES

1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.
2. The standard refresh interval (t_{REF}) for 256Mb SDRAMs is 64ms.
3. (NC, VREF) is VREF on devices that require an external voltage reference.
4. BA0 is the least significant bank address
5. BA1 is the most significant bank address
6. A10/AP is row address A10, autoprecharge and precharge all banks.
7. (NC, CK) is NC for devices using a single ended clock. CK is used for devices using a differential clock.
8. (NC, VREF) is VREF on devices that require an external voltage reference.
9. This standard is for a 4 Bank version only.

The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO-G

Configuration	8M X 32	8M X 32
Number RA	13	12
ROW ADDRESS	A0⇒A12	A0⇒A11
COLUMN ADDRESS	A0⇒A7	A0⇒A8

Note: This pin rotation is obsolete and will not be assigned to a package

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

FIGURE 3.11.4-6
8M BY 32 SDRAM PIN ROTATION IN TSOP2

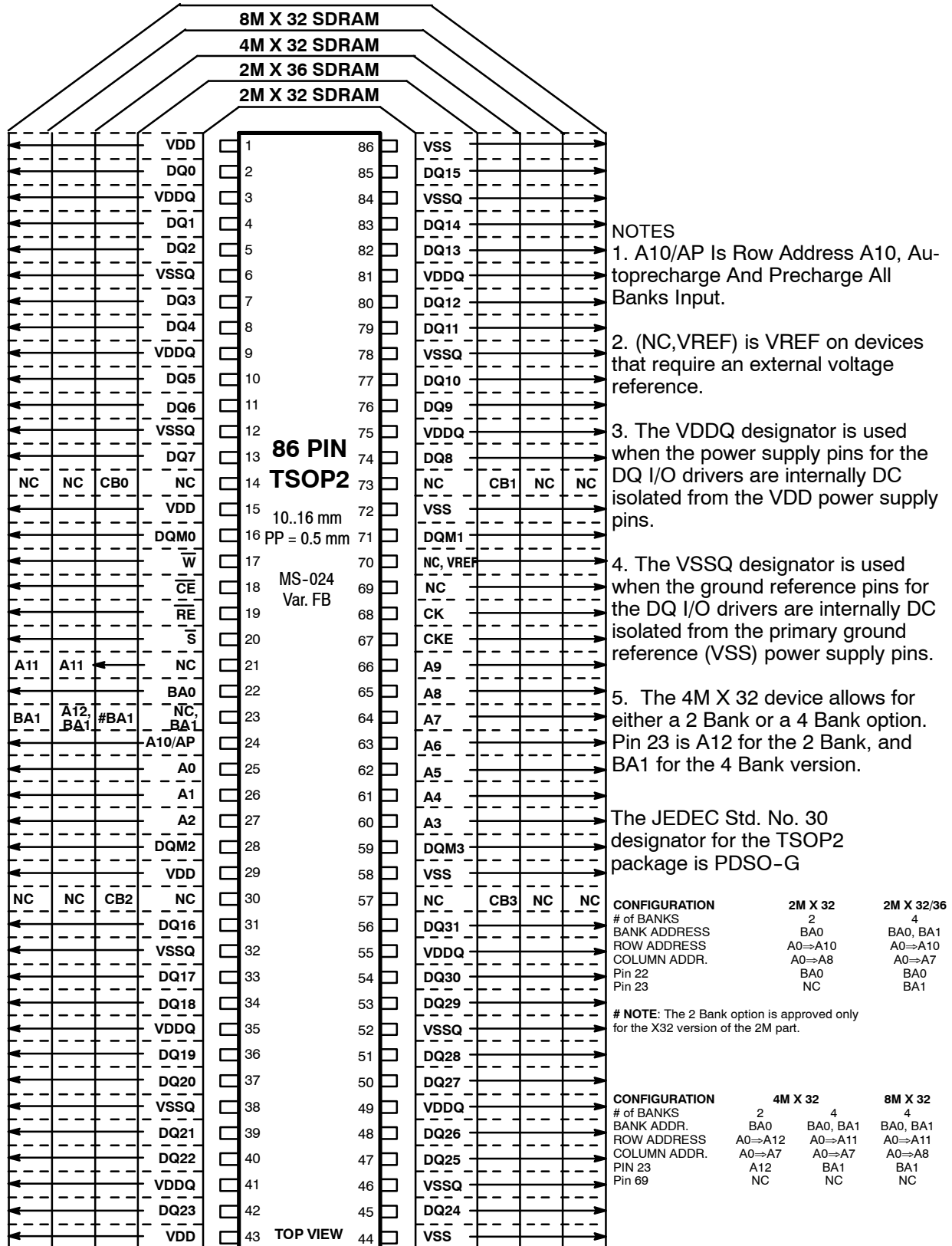


FIGURE 3.11.4-7
2M BY 32 & 36, 4M & 8M BY 32 SDRAM IN TSOP2