

3.11.5.1 - General SDRAM Functions

The Standards in this section are general functions that are applicable to both SDR and DDR SDRAM except where that function is specifically covered for a class of devices in one of the following sections.

3.11.5.1.1 - SDRAM FUNCTION TRUTH TABLE

This table defines the interface states required to execute the standard SDRAM operational functions. The original publication of this standard in Release 4 contained errors that are corrected in Release 5

3.11.5.1.2 - SDRAM FUNCTION TRUTH TABLE FOR CKE

This table defines the interface states required to execute the standard SDRAM operational functions with respect to the CKE input. The original publication of this standard in Release 4 contained errors that are corrected in Release 5

3.11.5.1.3 - SDRAM & SGRAM MODE REGISTER ARCHITECTURE

This standard describes the architecture of the SDRAM & SGRAM internal MODE REGISTER and the codes that are allowable for use in it. This is applicable to both SDR & DDR devices.

3.11.5.1.4 through 3.11.5.1.17 — SDRAM OPERATIONAL CYCLES AND MODES

The following standards define and describe a number of operational cycles and modes of SDRAM. They are ordered roughly in the sequence in which they would be used in normal SDRAM operation.

3.11.5.1.4 - POWER ON SEQUENCE (RECOMMENDED)

This standard gives a recommended power, clock, and logic-level sequence to be used on power-up to prevent data bus contention.

3.11.5.1.5 - AUTO PRECHARGE

This standard gives the logic function used to active the AUTO-PRECHARGE function.

3.11.5.1.6 - PRECHARGE ALL BANKS

This standard gives the logic function used to activate the PRECHARGE-ALL-BANKS function.

3.11.5.1.7 - MODE REGISTER WRITE TIMING

This standard defines the logic sequence and timing required to write into the MODE REGISTER.

3.11.5.1.8 - AUTO REFRESH

This standard defines the logic state and interface sequence required to perform an AUTO REFRESH

3.11.5.1.9 - WRITE LATENCY

This standard defines WRITE LATENCY and illustrates it with a timing diagram.

3.11.5.1.10 - DQM LATENCY FOR READS AND WRITES

In this standard DQM LATENCY is defined and the relationships between the DQM signal and the interface data for READs and WRITEs is defined and shown in timing diagrams.

3.11.5.1.11 - PRECHARGE TIMING FOR READS

This standard describes the relationship between the assertion of a PRECHARGE command and data out from a READ command.

3.11.5.1.12 - COLUMN ADDRESS TO COLUMN ADDRESS DELAY

This standard defines constraints imposed on the CA to CA delay and illustrates them with a timing diagram.

3.11.5.1.13 - CKE TIMING FOR POWER DOWN

This standard describes the interface sequence required to place the SDRAM into the POWER-DOWN state using CKE.

3.11.5.1.14 - CKE TIMING FOR CLOCK SUSPEND

This standard describes the interface timing sequence when CKE is used to suspend the clock.

3.11.5.1.15 - SELF REFRESH ENTRY AND EXIT

This standard defines the logic states and timing sequence used to enter and exit the SELF-REFRESH mode.

3.11.5.1.16 - Burst Stop/Burst Terminate Command for SDRAMs/SGRAMs

The Burst Stop [also called “Burst Terminate”] command (BST) is an optional feature for SDRAM/SGRAM. If the Burst Stop command is included in an SDRAM or SGRAM, this section defines the functionality that is required.

3.11.5.1.17 - Full Page Burst Mode for SDRAM/SGRAM

Full page burst mode is an optional feature for SDRAM/SGRAM. If full page burst mode is included in an SDRAM or SGRAM, this section gives the required functionality.

3.11.5.1.18 - Burst Stop/Burst Terminate Command for SDRAMs/SGRAMs

The Burst Stop [also called “Burst Terminate”] command (BST) is an optional feature for SDRAM/SGRAM. If the Burst Stop command is included in an SDRAM or SGRAM, this section defines the functionality that is required.

3.11.5.1.1 - SDRAM FUNCTION TRUTH TABLE

CURRENT STATE	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
IDLE	H L L L L L L L	X H H H L L L L	X H H L H H L L	X H L X H L H L	X X BA BA, CA BA, RA BA, A10 X Op-code	NOP NOP ILLEGAL ² ILLEGAL ² Row (& Bank) active; Latch Row Address NOP ⁴ Auto-Refresh ⁵ Mode Register Access ⁵
ROW ACTIVE	H L L L L L L	X H H H L L L	X H L L H H L	X X H L L H L X	X X BA, CA, A10 BA, CA, A10 BA, RA BA, A10 X	NOP NOP Begin Read; Latch CA; Determine AP ⁷ Begin Write; Latch CA; Determine AP ⁷ ILLEGAL ² Precharge ⁸ ILLEGAL
READ	H L L L L L L	X H H H L L L	X H H L L H L	X H L H L H L X	X X BA BA, CA, A10 BA, CA, A10 BA, RA BA, A10 X	NOP (Continue Burst to End;⇒Row Active) ⁶ NOP(Continue Burst to End;⇒Row Active) ⁶ RESERVED (Term. Burst);⇒Row Active Term Burst, New Read, Determine AP ³ Term Burst, Start Write, Determine AP ^{3, 7} ILLEGAL ² Term Burst, Precharge Timing for Reads ILLEGAL
WRITE	H L L L L L L	X H H H L L L	X H H L L H L	X H L H L H L X	X X BA BA, CA, A10 BA, CA, A10 BA, RA BA, A10 X	NOP(Continue Burst to End;⇒Row Active) ⁶ NOP(Continue Burst to End;⇒Row Active) ⁶ RESERVED (Term Burst);⇒Row Active Term Burst, Start Read, Determine AP ^{3, 7} Term Burst, New Write, Determine AP ³ ILLEGAL ² Term Burst, Precharge ³ ILLEGAL
READ with AUTO Precharge	H L L L L L	X H H H H* L L	X H H L L H L	X H L H L X X	X X BA BA, CA, A10 X BA, RA, A10 X	NOP (Continue Burst to End;⇒Precharge) ⁶ NOP (Continue Burst to End;⇒Precharge) ⁶ ILLEGAL ² ILLEGAL ² ILLEGAL ILLEGAL ² ILLEGAL
WRITE with AUTO Precharge	H L L L L L	X H H H L L	X H H L L H L	X H L H L X X	X X BA BA, CA, A10 X BA, RA, A10 X	NOP (Continue Burst to End;⇒Precharge) ⁶ NOP (Continue Burst to End;⇒Precharge) ⁶ ILLEGAL ² ILLEGAL ² ILLEGAL ILLEGAL ² ILLEGAL

TABLE 3.11.5.1-1
SDRAM FUNCTION TRUTH TABLE

3.11.5.1.1 - SDRAM FUNCTION TRUTH TABLE (continued)

CURRENT STATE	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	An	ACTION
Precharging	H L L L L L L	X H H H L L L	X H H L H H L	X H L X H L X	X X BA BA, CA BA, RA BA, A10 X	NOP⇒idle after tRP NOP⇒idle after tRP ILLEGAL ² ILLEGAL ² ILLEGAL ² NOP ⁴ ILLEGAL
ROW Activating	H L L L L L L	X H H H L L L	X H H L H H L	X H L* X H L X	X X BA * BA, CA BA, RA BA, A10 X	NOP⇒Row Active after tRCD NOP⇒Row Active after tRCD ILLEGAL ² ILLEGAL ² ILLEGAL ² ILLEGAL ² ILLEGAL
WRITE Recovering	H L L L L L L	X H H H L L L	X H H L H H L	X H L X H L X	X X BA BA, CA BA, RA BA, A10 X	NOP NOP ILLEGAL ² ILLEGAL ² ILLEGAL ² ILLEGAL ² ILLEGAL
Refreshing	H L L L L L L	X H H L L L L	X H L H H L L	X X X X X X X	X X X X X X X	NOP⇒idle after tRC* NOP⇒idle after tRC * ILLEGAL ILLEGAL ILLEGAL
Mode Register Accessing	H L L L L L L	X H H H L L L	X H H L L L X	X H L X X X X	X X X X X X X	NOP NOP ILLEGAL ILLEGAL ILLEGAL ILLEGAL

ABBREVIATIONS

RA = Row Address
CA = Column Address

BA = Bank Address
AP = Auto Precharge

Term = Terminate
NOP = No Operation

NOTES:

1. All entries assume that CKE was active (HIGH) during the preceeding clock cycle and the current clock cycle.
 2. Illegal to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
 3. Must satisfy the "2n-rule", bus contention, but turn around, and/or write recovery requirements.
 4. NOP to bank precharging or in idle state. May precharge bank(s) indicated by BA (and A10).
 5. Illegal if any bank is not idle.
- ILLEGAL = Device operation and/or data-integrity are not guaranteed
6. If the device is programmed to use full page burst mode, the action is NOP, continue burst.
 7. The autoprecharge bit, AP, must be 0 in full page burst mode where the autoprecharge function is illegal
 8. Precharge All Banks determined by state of A10

* Elements of the table that were in error in the first printing of Release 4

TABLE 3.11.5.1-1
SDRAM FUNCTION TRUTH TABLE (Continued)

3.11.5.1.2 - SDRAM FUNCTION TRUTH TABLE for CKE

CURRENT STATE	CKE _{n-1}	CKE _n	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	A _n	ACTION
Self- refresh ⁶	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	EXIT Self-Refresh⇒ ABI
	L	H	L	H	H	H	X	EXIT Self-Refresh⇒ ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
Power- Down	H	X*	X	X	X	X	X	INVALID
	L	H*	H	X*	X*	X*	X	EXIT Power Down⇒ABI
	L	H*	L	H	H	H	X	EXIT Power Down⇒ABI
	L	H*	L	H	H*	L*	X	ILLEGAL
	L	H*	L	H*	L*	X*	X	ILLEGAL
	L	H*	L	L	X*	X*	X	ILLEGAL
	L	L	X	X*	X*	X	X	NOP(Maintain Low-Power Mode)
All Banks Idle ⁷	H	H	X	X	X	X	X	Refer to Table 1
	H	L	H	X	X	X	X	Enter Power-Down
	H	L	L	H	H	H	X	Enter Power-Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	X	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
Any State other than listed above	H	H	X	X	X	X	X	Refer to operations Table 1
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle ⁸
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle ⁸
	L	L	X	X	X	X	X	Maintain Clock Suspend.

ABBREVIATIONS

ABI = All Banks Idle

NOTES:

6. CKE Low-to-High transition will re-enable CK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.

7. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.

8. Must be legal command.

* Elements of the table that were in error in the first printing of Release 4

TABLE 3.11.5.1-2
SDRAM FUNCTION TRUTH TABLE for CKE

3.11.5.1.3 - SDRAM & SGRAM Mode Register

This Mode Register is located on the Synchronous DRAM (SDRAM or SGRAM) chip. Its purpose is to store the mode-of-operation data. This data is written after power-on and before normal operation. The data contains the Burst Length, the Burst Type, the $\overline{\text{CAS}}$ Latency (Defined separately for SDR and DDR devices), and whether it is to be operating in Test Mode, or Normal operating mode. During operation, this register (and therefore operation of the chip) may be changed, according to the requirements of the Mode-Register-Write Timing diagram. So, while operating in one mode, for example Burst of 4 in sequential addresses; it can change to Burst of 8 in Interleaved address mode.

SDRAM Mode Register architecture:

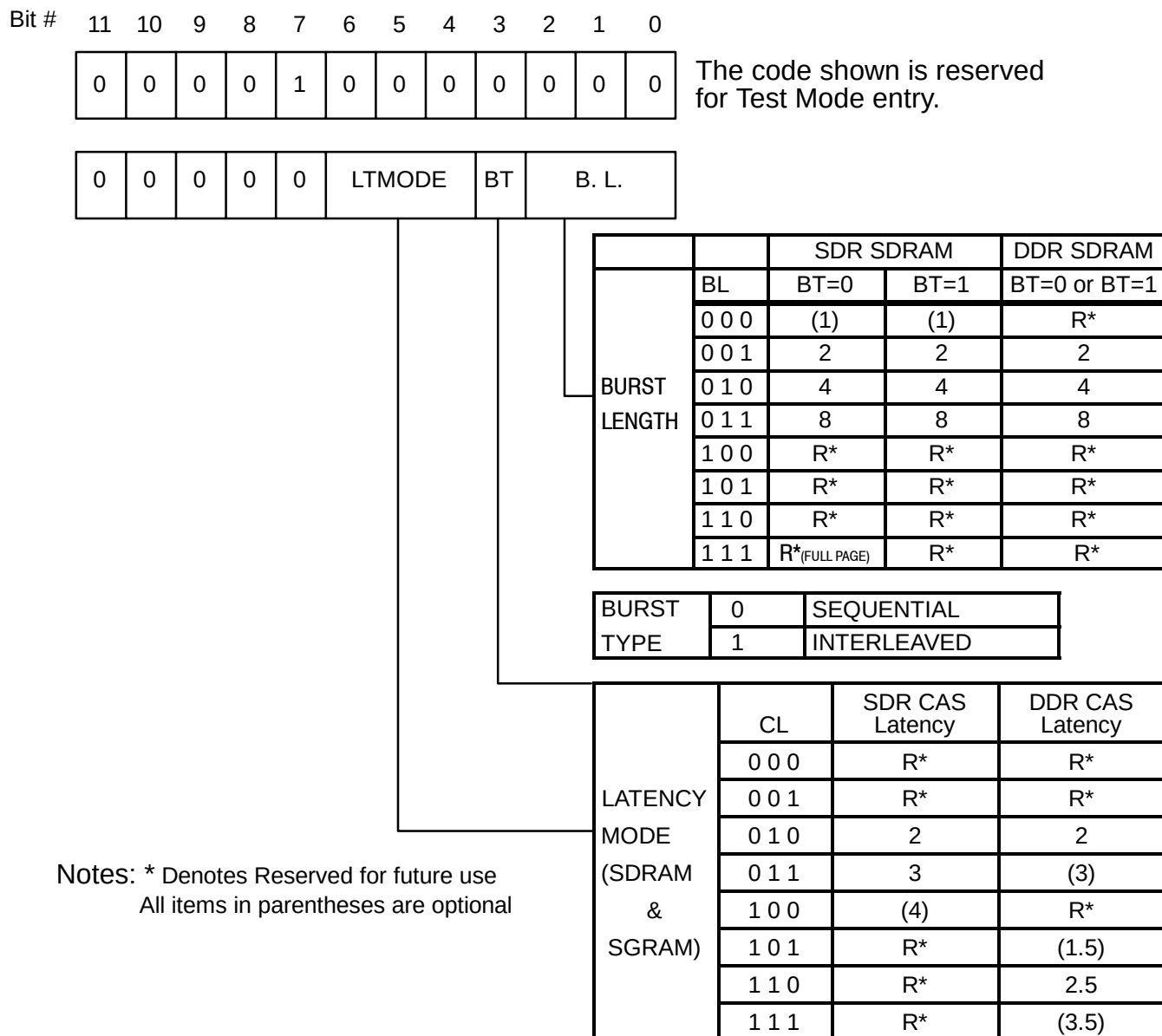


FIGURE 3.11.5.1-1
SDRAM & SGRAM MODE REGISTER ARCHITECTURE