

3.11.5.2 - DDR Specific SDRAM Functions

The Standards in this section are special functions that are applicable to DDR SDRAM except where that function specifically defines another class of device for which it is applicable.

3.11.5.2.1 - Bi-Directional DQS for DDR SDRAM

To enable Doubled Data Rate and the control of that data in DDR SDRAMs, a signal to be identified by the label DQS will be added to the existing definition of the SDRAM. This section defines the timing relationships of the DQS signal.

3.11.5.2.2 - Differential Clock for DDR SDRAMs & SGRAMs

A pin will be added to the definition of DDR SDRAM devices whose polarity will be inverted to that of CK and labeled CK $\overline{}$ or $\overline{CK}$. That pin along with CK must be used to supply a differential clock to the DDR SDRAM devices.

3.11.5.2.3 - Read Interrupting a Write Operation for DDR SDRAMs/SGRAMs

The following functionality establishes how a Read command may interrupt a Write burst and which input data is not written into the memory.

3.11.5.2.4 - Write Interrupting a Read Operation for DDR SDRAMs/SGRAMs

The following functionality establishes how a Write command may interrupt a Read burst.

3.11.5.2.5 - Precharge Timing for Reads for DDR SDRAMs/SGRAMs

When a burst Read command is issued to a DDR SDRAM/SGRAM, a Precharge command may be issued to the same bank before the Read burst is complete. The following functionality determines when a Precharge command may be given during a Read burst and when a new Bank Activate command may be issued to the same bank.

3.11.5.2.6 - Precharge Timing for Writes for DDR SDRAMs/SGRAMs

Precharge timing for Write operations in DRAMs requires enough time to allow "write recovery" which is the time required by a DRAM core to properly store a full "0" or "1" level before a Precharge operation. For DDR SDRAM/SGRAM, a timing parameter, tWR, is used to indicate the required amount of time between the last valid write operation and a Precharge command to the same bank.

3.11.5.2.7 - Burst Stop Command for DDR SDRAMs/SGRAMs

The Burst Stop [also called "Burst Terminate"] command (BST) is a mandatory feature for DDR SDRAMs/SGRAMs. This section describes the required functionality.

3.11.5.2.8 - DDR SDRAM/SGRAM Full Sequential Burst Ordering

This section gives, for DDR SDRAM & SGRAM, Y address ordering that is supported for sequential burst lengths (BL) of 2, 4, and 8:

3.11.5.2.9 - DDR SDRAM DQS Coincident with Data

The timing of the signal DQS relative to Read Data from the DDR SDRAM device is giving.

3.11.5.2.10 - Extended Mode Register Set for DDR SDRAM / SGRAM.

Extended mode register address space is provided by defining non-zero Bank address(s) for accesses that otherwise conform to the Mode Register Set (MRS) cycle. These Extended Mode Register Set cycles (EMRS) can be implemented as needed for function extensions to the standard.

3.11.5.2.11 - DLL Enable/Disable Mode for DDR SDRAM/SGRAM with EMRS

This section defines the DLL disable/enable bit in the Extended Mode Register.

3.11.5.2.12 - Refresh Requirements

This section provides the precise definition of the refresh requirements.

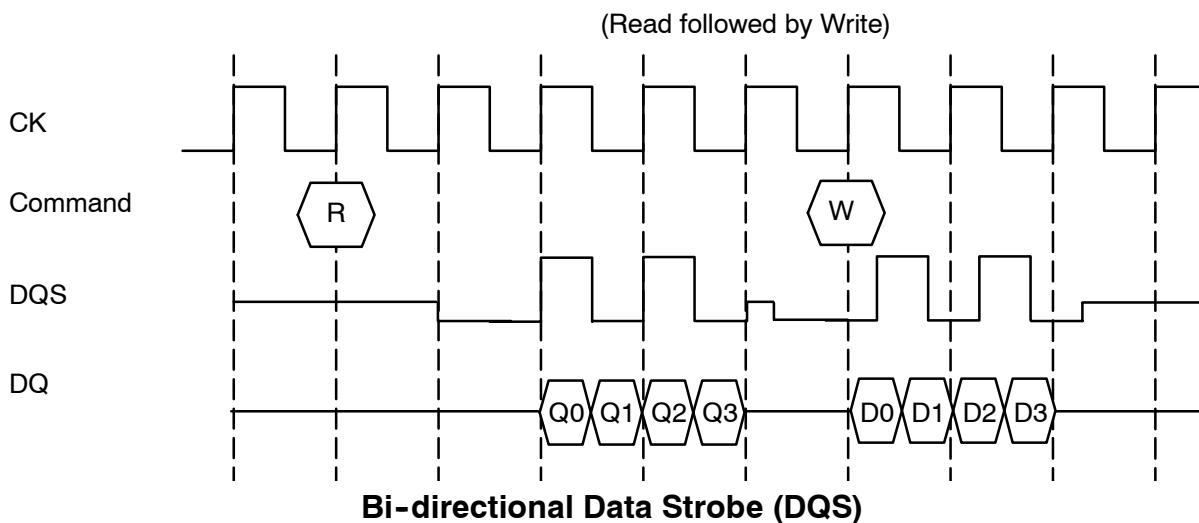
3.11.5.2.13 - MRS/EMRS for Low Power DDR SDRAM

This section provides the Mode Register Set and Extended Mode Register Set definition for Low Power DDR SDRAM.

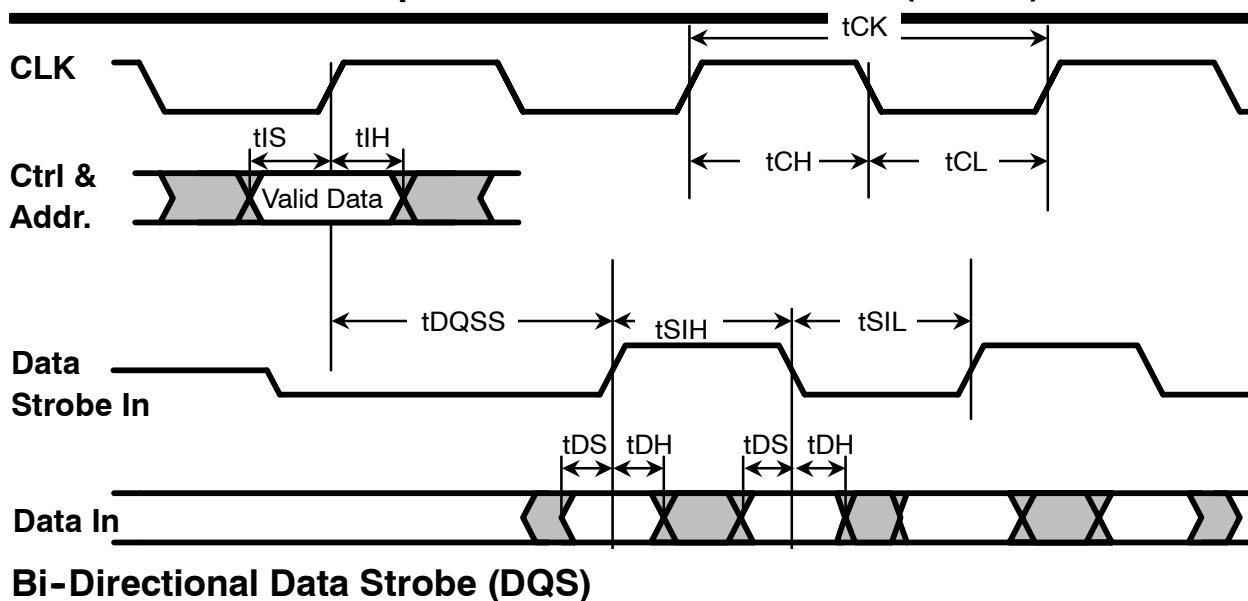
3.11.5.2.1 - Bi-Directional DQS for DDR SDRAM

To enable Doubled Data Rate and the control of that data in DDR SDRAMs, a signal to be identified by the label DQS will be added to the existing definition of the SDRAM.

Driven by the DDR SDRAM during output of Read data, and Driven by the Memory Controller during input of Write data, the rising and falling edges of that signal (DQS) will indicate the output of Read Data and the input of Write Data on the data output and input pins (DQ) of DDR SDRAM.

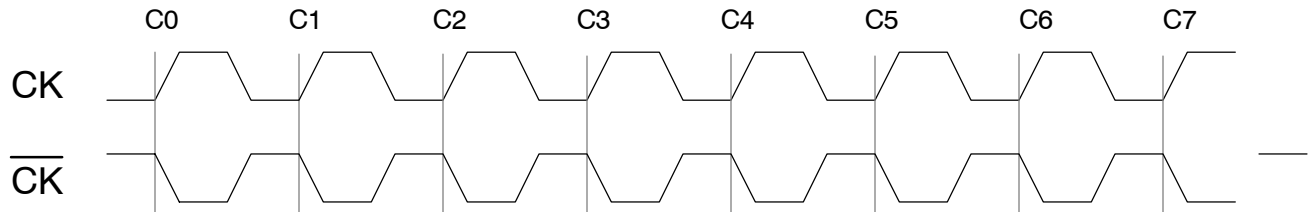


Example of BASIC WRITE TIMING (@DQS)



3.11.5.2.2 - Differential Clock for DDR SDRAMs & SGRAMs

A pin will be added to the definition of DDR SDRAM devices whose polarity will be inverted to that of CK and labeled CK $\bar{}$ or $\overline{CK}$. That pin along with CK must be used to supply a differential clock to the DDR SDRAM devices. The slew rates, and recommended terminations will be defined in subsequent standards. The voltage levels are defined in Section 3.11.6 for which standards have been published.



Differential Clock timing relationship (for reference only)

3.11.5.2.3 - Read Interrupting a Write Operation for DDR SDRAMs & SGRAMs

The following functionality establishes how a Read command may interrupt a Write burst and which input data is not written into the memory.

1. For Read commands interrupting a Write burst, the minimum Write to Read command delay is 2 clock cycles. The case where the Write to Read delay is 1 clock cycle (refer to Figure 1) is disallowed.
2. For Read commands interrupting a Write burst, the DM pin must be used to mask the input data words which immediately precede the interrupting Read operation and the input data word which immediately follows the interrupting Read operation as shown in Figures 2 and 3.
3. For all cases of a Read interrupting a Write, the DQ and DQS buses must be released by the driving chip (i.e., the memory controller) in time to allow the buses to turn around before the SDRAM/SGRAM drives them during a read operation.
4. If input Write data is masked by the Read command, the DQS input is ignored by the SDRAM/SGRAM.
5. It is illegal for a Read command to interrupt a Write with autoprecharge command.

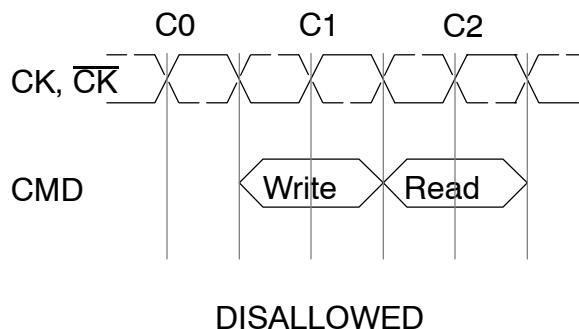
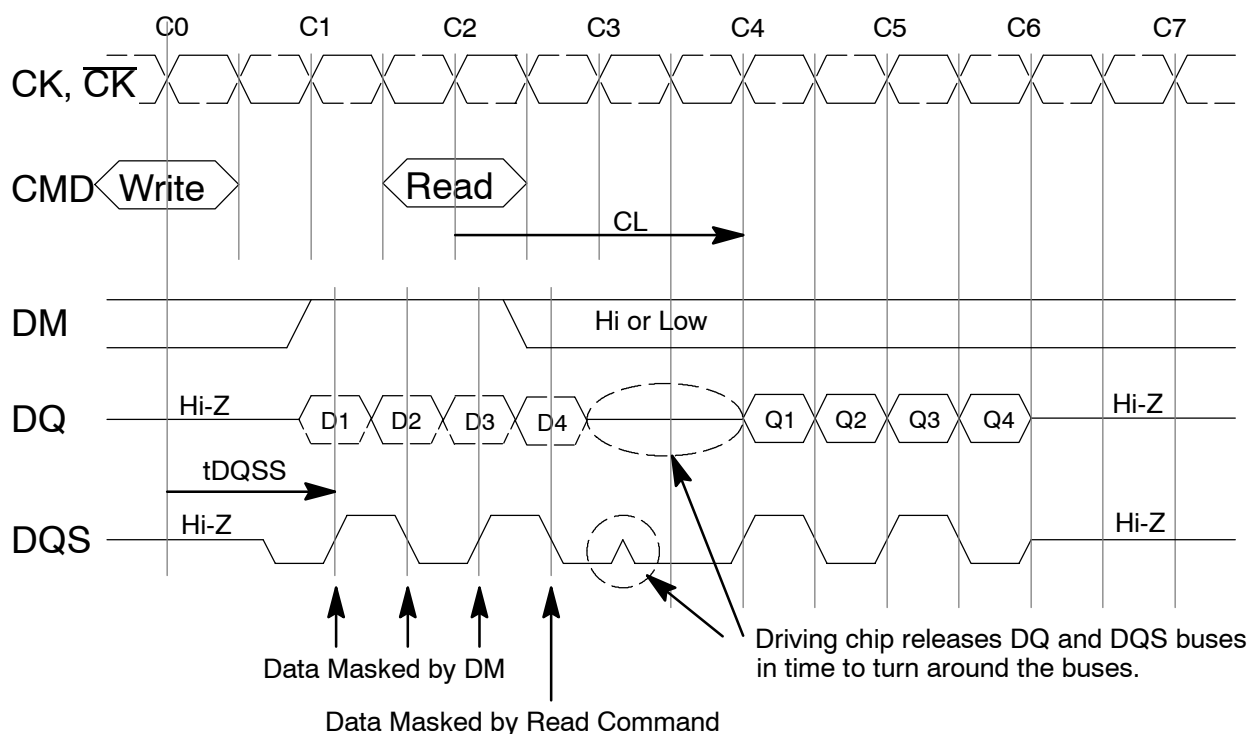


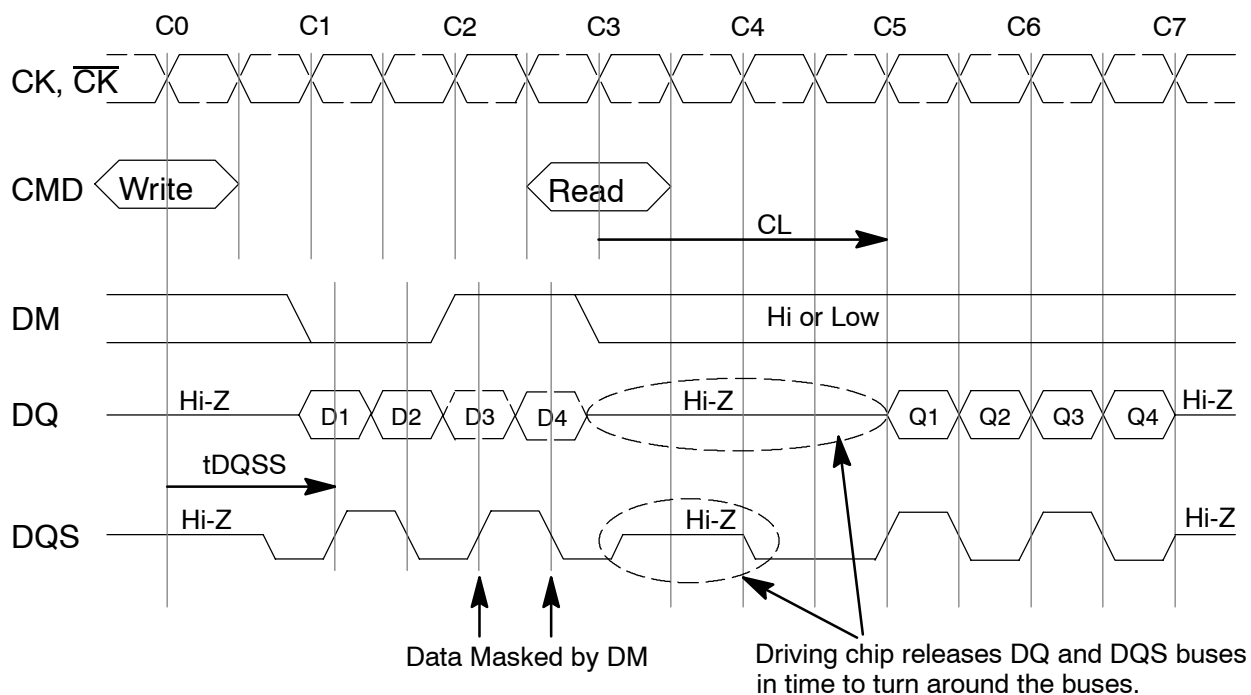
Figure 1: Read Interrupting a Write - Write to Read Delay = 1 Clock Cycle

3.11.5.2.3 (Cont) - Read Interrupting a Write Operation for DDR SDRAMs & SGRAMs



In this example, the Burst Length = 4 and the operations are not necessarily to the same bank.

Figure 2: Read Interrupting a Write - Write to Read Delay = 2 Clock Cycles



In this example, the Burst Length = 4 and the operations are not necessarily to the same bank.

Figure 3: Read Interrupting a Write - Write to Read Delay = 3 Clock Cycles

3.11.5.2.4 - Write Interrupting a Read Operation for DDR SDRAMs/SGRAMs

The following functionality establishes how a Write command may interrupt a Read burst.

1. For Write commands interrupting a Read burst, a Burst Terminate command is required to stop the read burst and tristate the DQ bus prior to valid input write data. Once the Burst Terminate command has been issued, the minimum delay to a Write command = $RU(CL)$ [CL is the CAS Latency and RU means round up to the nearest integer]. Refer to Figures 1 and 2.
2. It is illegal for a Write command to interrupt a Read with autoprecharge command.

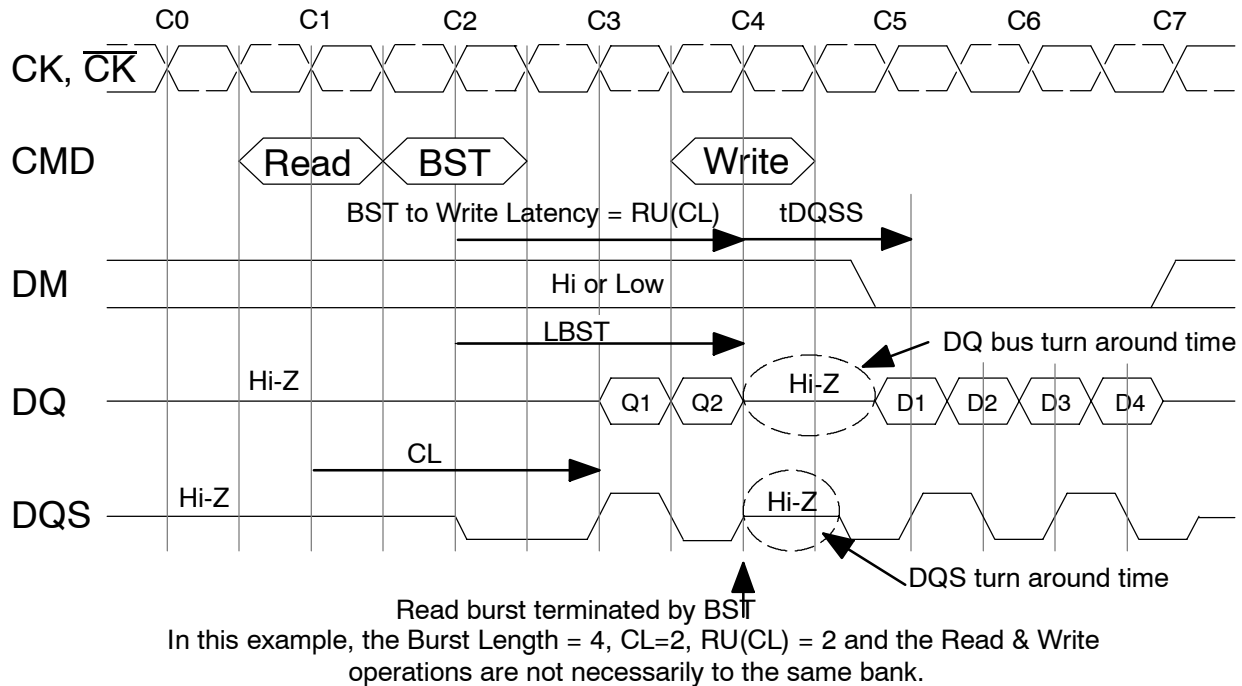


Figure 1: Write Interrupting a Read Burst ($\overline{CAS}$ Latency, CL, = X.0)

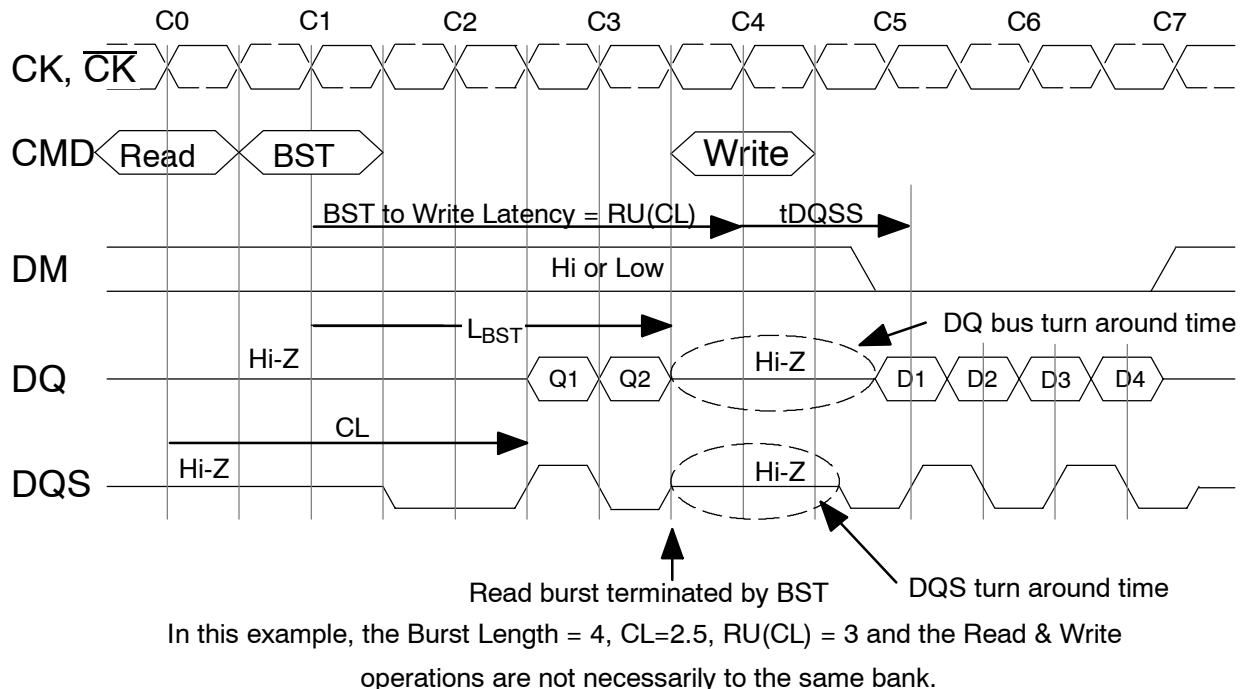


Figure 2: Write Interrupting a Read Burst ($\overline{CAS}$ Latency, CL, = X.5)

3.11.5.2.5 - Precharge Timing for Reads for DDR SDRAMs/SGRAMs

When a burst Read command is issued to a DDR SDRAM/SGRAM, a Precharge command may be issued to the same bank before the Read burst is complete. The following functionality determines when a Precharge command may be given during a Read burst and when a new Bank Activate command may be issued to the same bank.

1. For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be given on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the $\overline{\text{CAS}}$ Latency. A new Bank Activate command may be issued to the same bank after tRP (RAS Precharge time). Refer to Figure 1.
3. When a Precharge command interrupts a Read burst operation, the Precharge command may be given on the rising clock edge which is CL clock cycles before the last data from the interrupted Read burst where CL is the $\overline{\text{CAS}}$ Latency. Once the last data word has been output, the output buffers are set to the Hi-Z state. A new Bank Activate command may be issued to the same bank after tRP. Refer to Figure 2.
4. For a Read with autoprecharge command, a new Bank Activate command may be issued to the same bank after tRP where tRP begins on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the $\overline{\text{CAS}}$ Latency. During Read with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command would initiate a precharge operation without interrupting the Read burst as described in 1 above. Refer to Figure 3.
5. For all cases above, tRP is an analog delay that needs to be converted into clock cycles. The number of clock cycles between a Precharge command and a new Bank Activate command to the same bank equals tRP/tCK (where tCK is the clock cycle time) with the result rounded up to the nearest integer number of clock cycles. (Note that rounding to X.5 is not possible since the Precharge and Bank Activate commands can only be given on a *rising* clock edge).
5. In all cases, a Precharge operation cannot be initiated unless tRAS(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Read with autoprecharge commands where tRAS(min) must still be satisfied such that a Read with autoprecharge command has the same timing as a Read command followed by the earliest possible Precharge command which does not interrupt the burst.