

3.11.5.3 – Enhanced SDRAM (ESDRAM) Specific SDRAM Functions

The Standards in this section are special functions that are applicable to Enhanced SDRAM (ESDRAM). The standards cover both SDR and DDR devices as stated on the individual Standards.

3.11.5.3.1 – Read-AutoPrecharge Operation for SDR ESDRAM

In the Enhanced SDRAM (ESDRAM), a Read-Autoprecharge command will initiate multiple functions. This standard defines those functions.

3.11.5.3.2 – Read-AutoPrecharge Operation for DDR ESDRAM

In the DDR Enhanced SDRAM (DDR ESDRAM), a Read-Autoprecharge command will initiate multiple functions. This standard defines those functions.

3.11.5.3.3 – Cache Load Operation for SDR ESDRAM

In the Enhanced SDRAM (ESDRAM), a Cache Load command will initiate multiple functions. This standard defines those functions.

3.11.5.3.4 – Cache Load Operation for DDR ESDRAM

In the DDR Enhanced SDRAM (DDR ESDRAM), a Cache Load command will initiate multiple functions. This standard defines those functions.

3.11.5.3.5 – No Write Transfer, Mode of Operation for SDR ESDRAM

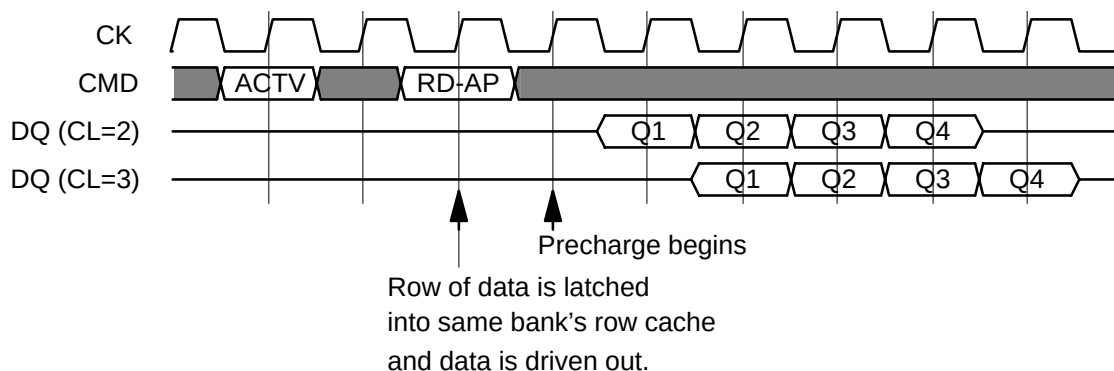
“No Write Transfer” mode is an optional mode of operation that allows an Enhanced SDRAM (ESDRAM) to concurrently keep a read page and a write page open per bank. This Standard defines the details of this operational mode.

3.11.5.3.6 – No Write Transfer, Mode of Operation for DDR ESDRAM

“No Write Transfer” mode is an optional mode of operation that allows a DDR Enhanced SDRAM (DDR ESDRAM) to concurrently keep a read page and a write page open per bank. This Standard defines the details of this operational mode.

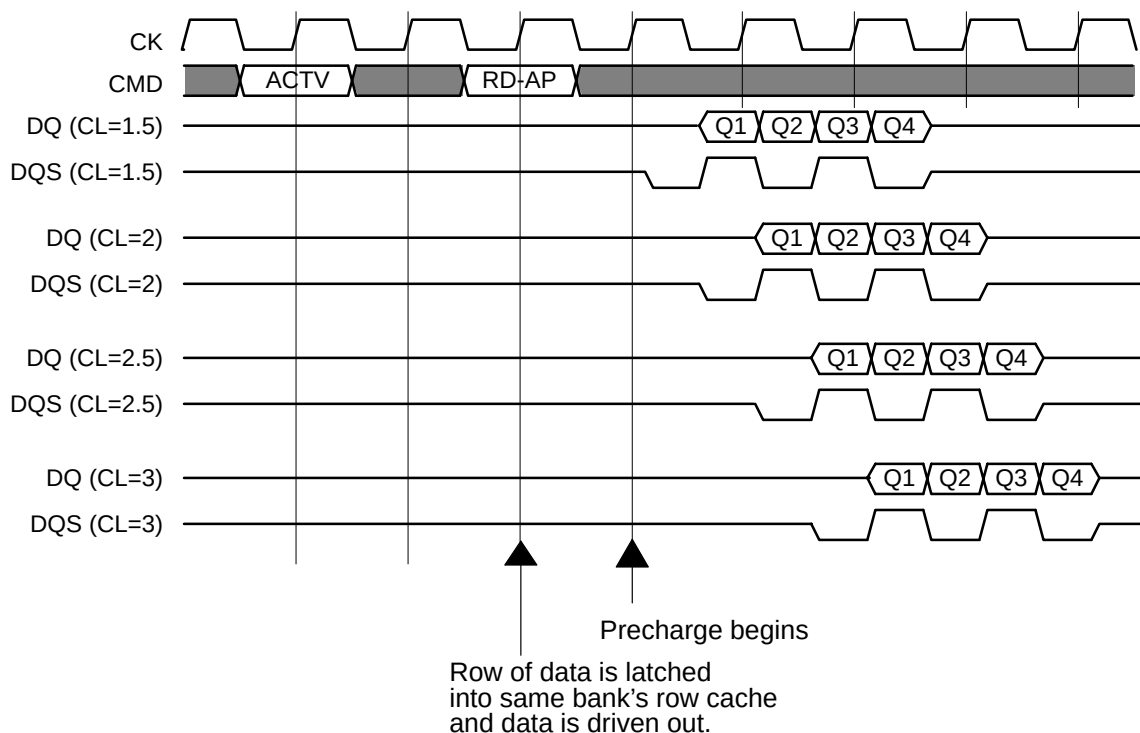
3.11.5.3.1 – Read-Auto Precharge Operation for SDR ESDRAM

The Enhanced SDRAM (ESDRAM) integrates a row cache per DRAM bank for the purposes of (1) holding read page data, (2) providing burst read output data, and (3) allowing background operations (e.g. precharge, refresh) to be performed. In such a device, a Read-Autoprecharge command will initiate a read (burst length defined by the Mode Register), load the row cache with the contents of the sense amp data from the addressed row of the selected active bank, and begin the precharge one clock cycle following the Read Autoprecharge command independent of the burst length. In the diagram below, a 4-word burst is shown.



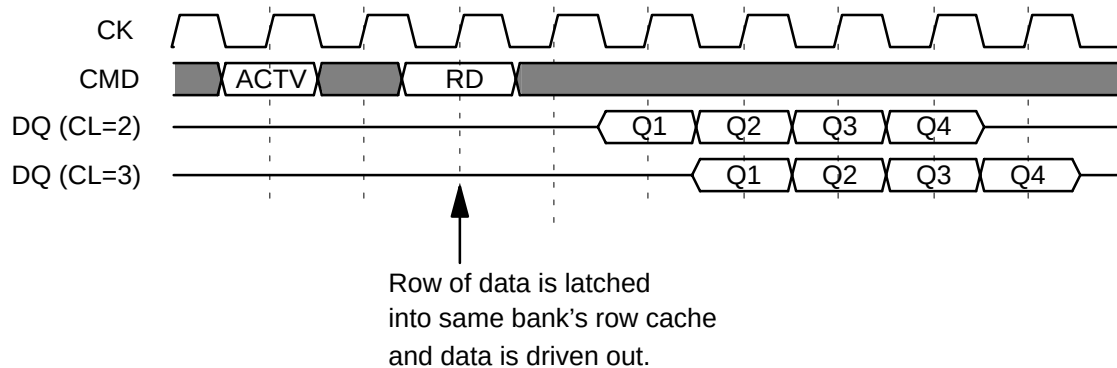
3.11.5.3.2 – Read-Auto Precharge Operation for DDR ESDRAM

The DDR Enhanced SDRAM (DDR ESDRAM) integrates a row cache per DRAM bank for the purposes of (1) holding read page data, (2) providing burst read output data, and (3) allowing background operations (e.g. precharge, refresh) to be performed. In such a device, a Read-Autoprecharge command will initiate a read (burst length defined by the Mode Register), load the row cache with the contents of the sense amp data from the addressed row of the selected active bank, and begin the precharge one clock cycle following the Read Autoprecharge command independent of the burst length. In the diagram below, a 4-word burst is shown.



3.11.5.3.3 – Cache Load Operation for SDR ESDRAM

The Enhanced SDRAM (ESDRAM) integrates a row cache per DRAM bank for the purposes of (1) holding read page data, (2) providing burst read output data, and (3) allowing background operations (e.g. precharge, refresh) to be performed. In such a device, a Read command will initiate a read (burst length defined by the Mode Register), load the row cache with the contents of the sense amp data from the addressed row of the selected active bank. In the diagram below, a 4-word burst is shown.



3.11.5.3.4 – Cache Load Operation for DDR ESDRAM

The DDR ESDRAM integrates a row cache per DRAM bank for the purposes of (1) holding read page data, (2) providing burst read output data, and (3) allowing background operations (e.g. precharge, refresh) to be performed. In such a device, a Read command will initiate a read (burst length defined by the Mode Register) and load the row cache with the contents of the sense amp data from the addressed row of the selected active bank. In the diagram below, a 4-word burst is shown. Although half-clock preamble is shown, it is not a requirement of this proposal.

